	Pre.0	2019.5.24

Title	5.0”1080*1080 TFT-LCD (LCM)

Buyer	
Model	

Supplier	
Model	ZS050YMM-N41

TITLE/SIGNATURE	DATE
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ITEM	SIGNATURE/DATE
Approved	_____
Reviewed	_____
Reviewed	_____
Prepared	_____
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	Pre.0	2019.5.24

CONTENT LIST

	Pre.0	2019.5.24

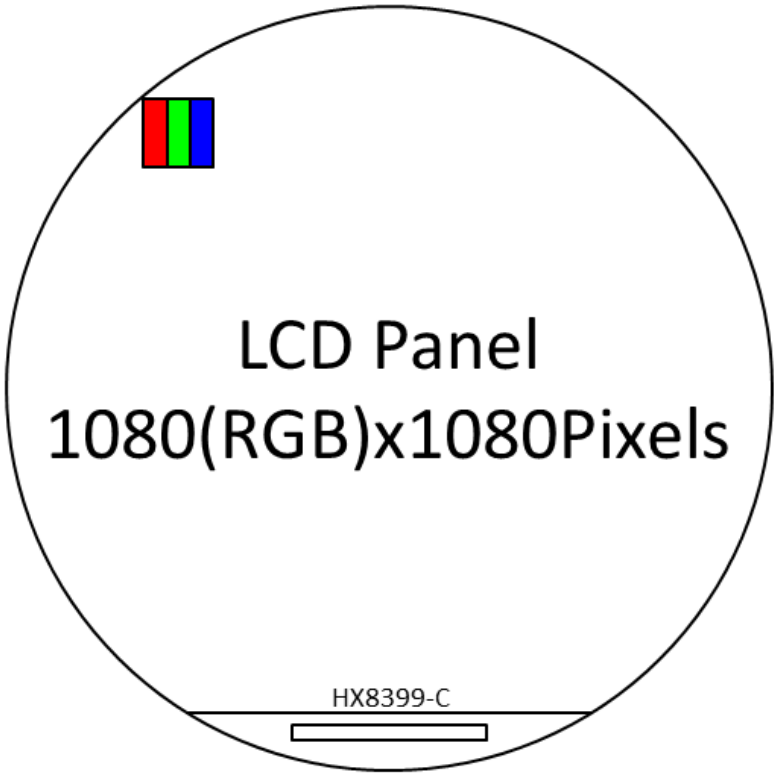
Record of Revisions

Revision	Date	Page	Description	Released by
Pre.0	2019.5.24		Initial Released	Liumin

1.0 GENERAL DESCRIPTION

1.1 Introduction

PL050HDC is a color active matrix TFT-LCD Panel using LTPS TFT's (Thin Film Transistors) as an active switching devices. This model is composed of a TFT-LCD Panel, a driving circuit and a back light system. It is a transmissive type display operating in the normal black. This TFT-LCD has a 5.0 inch diagonally measured active area with FHD resolutions (1080 horizontal by 1080 vertical pixel array). Each pixel is divided into Red, Green, Blue dots which are arranged in 1pixel 2 domain and this panel can display 16.7M colors.



1.2 Features

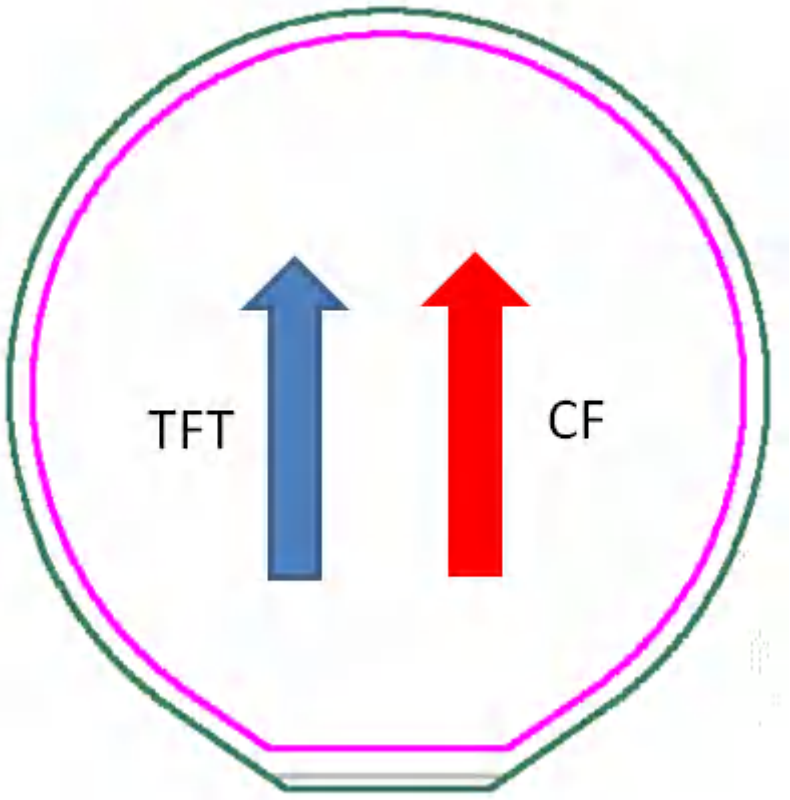
- 0.2t Glass (Single)
- High contrast ratio and wide viewing angle
- Module Design
- RoHS Compliant

1.3 General Specifications (H: horizontal length, V: vertical length)

Parameter	Specification	Unit	Remark
Active Area	127.008 (H) ×127.008 (V)	mm	circle
Number of Pixels	1080(H) RGB × 1080(V)	pixels	
Pixel Pitch	0.1176 (H) ×0.1176 (V)	mm	
Pixel Arrangement	1pixel 2domain		
Display Colors	16.7 M	colors	
Color Gamut	65%(Min.) 70%(typ.)		
Display Mode	Normally Black, Transmissive mode		
Dimensional Outline	136.531x132.208x1.98	mm	
Viewing Direction (Human Eye)	U/D/L/R free viewing direction		Note 1,2

Note:

1. At the U/D/L/R direction, the viewing angle is same;
2. The TFT and CF LC Algin Direction;



2.0 ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are list on table as follows. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Parameter	Symbol	Spec			Unit
		Min.	Typ.	Max.	
Logic Power Supply Voltage	IOVCC	-0.3		+3.6	V
Analog Positive Power Supply	VSP	-0.3		+6.6	V
Analog Negative Power Supply	VSN	0		-6.6	V
Back-light Power Supply Voltage	V_{LED}		37.2	38.4	V
Back-light LED Current	I_{LED}		20		mA
Operating Temperature	T_{OT}	-20		60	℃
Storage Temperature	T_{ST}	-30		75	℃

Note:

If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Module DC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Power Supply Input Voltage	IOVCC	1.65	1.8	3.3	V	-
Analog Positive Power Supply	VSP	4.8	5	6	V	
Analog Negative Power Supply	VSN	-6	-5	-4.8	V	
Low Level Input Voltage	VIL	0		0.3* IOVCC	V	
High Level Input Voltage	V_{IH}	0.7* IOVCC		IOVCC	V	
Power Consumption	P_D	-	-	-	W	Note
	PBL	-	0.744	0.768	W	
	PTotal	-		-	W	

Note:

Frame rate=60HZ, Typ. Pattern White pattern, worst case pattern 1×1 checker 25℃.

3.2 Backlight Driving Conditions

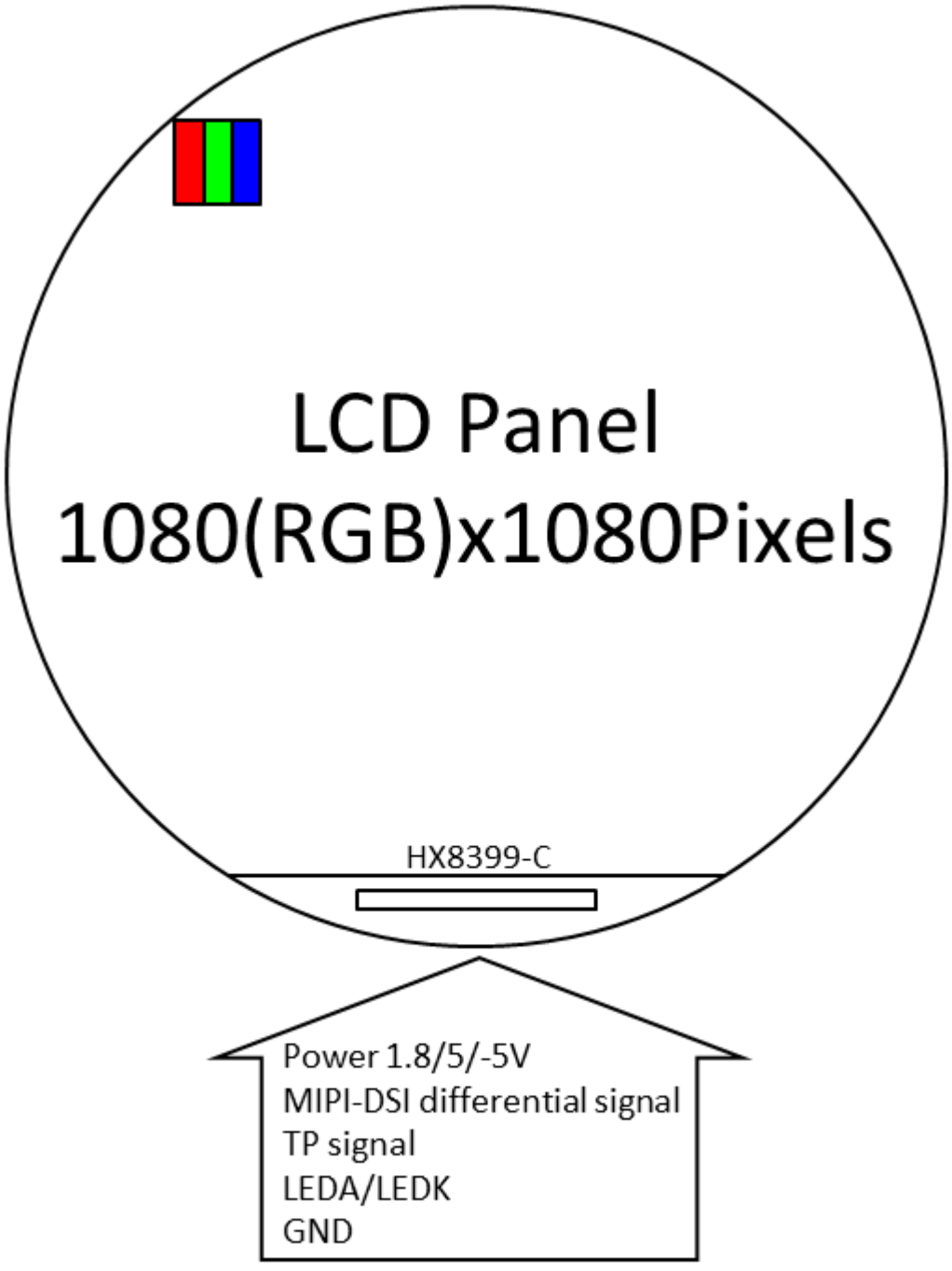
Parameter	Symbol	Min	Typ	Max	Unit	Remark
LED Forward Voltage	V_F		37.2	38.4	V	-
LED Forward Current	I_F		20		mA	-
LED Power Consumption	PLED		0.744	0.768	W	Note 1

Notes:

1. Calculator Value for reference ILED×VLED×LED Quantity = PLED

2. The LED Life-time define as the estimated time to 50% 30000hrs degradation of initial luminous.

3.3 Block Diagram



4.0 INTERFACE CONNECTION

4.1 Connector Part Number

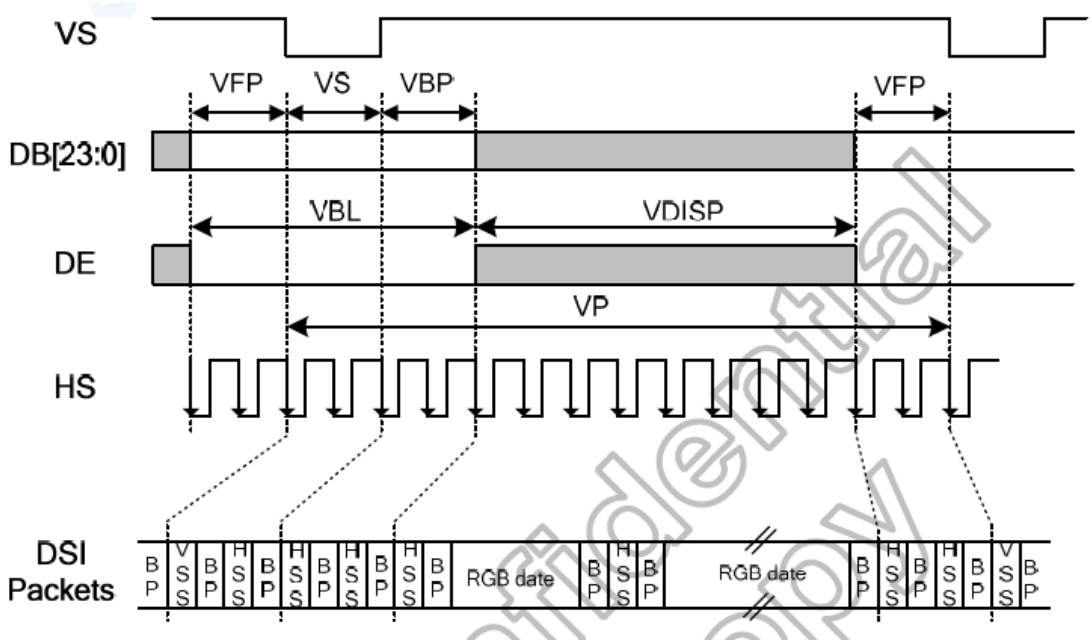
Connector Name / Designation	Signal Connector
Manufacturer	Hirose
Connector Model Number	DF40C-50DP-0.4V

4.2 Electrical Interface Connection

Pin NO.	Pin name	Function	Pin NO.	Pin name	Function
49	GND	Ground	50	GND	Ground
47	GND	Ground	48	RESET	Disp reset
45	NC	NC	46	TE	Disp tearing effect out
43	NC	NC	44	LEDPWM	Backlight pwm output
41	NC	NC	42	GND	Ground
39	NC	NC	40	NC	NC
37	GND	Ground	38	VDD(+5)	Disp +5V analog rail
35	NC	NC	36	VDD(+5)	Disp +5V analog rail
33	NC	NC	34	NC	NC
31	GND	Ground	32	VDD(-5)	Display -5V analog rail
29	LAN3_N	Disp MIPI lane 3-	30	VDD(-5)	Display -5V analog rail
27	LAN3_P	Disp MIPI lane 3+	28	NC	NC
25	GND	Ground	26	GND	Ground
23	LAN0_N	Disp MIPI lane 0-	24	IOVCC	Disp digital power
21	LAN0_P	Disp MIPI lane 0+	22	IOVCC	Disp digital power
19	GND	Ground	20	GND	Ground
17	CLK_N	Disp MIPI CLK -	18	ID_PIN1	ID pd to GND (BOE)
15	CLK_P	Disp MIPI CLK +	16	ID_PIN2	ID pu to 1.8V (BOE)
13	GND	Ground	14	GND	Ground
11	LAN1_N	Disp MIPI lane 1-	12	LEDA	LED Anode
9	LAN1_P	Disp MIPI lane 1+	10	LEDA	LED Anode
7	GND	Ground	8	GND	Ground
5	LAN2_N	Disp MIPI lane 2-	6	LEDK	LED cathode
3	LAN2_P	Disp MIPI lane 2+	4	LEDK	LED cathode
1	GND	Ground	2	GND	Ground

5.0 SIGNAL TIMING SPECIFICATION

Vertical Timing



Vertical Resolution=528+8xNL (VSSA=0V, VDD1=1.8V, VDD3=2.8V, T_A=25°C)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Vertical cycle	VP	-	534+8xNL	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(1)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(1)	Line
Vertical data start point	-	VS+VBP	4	-	Note(1)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	528+8xNL	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSP and GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display.