

Approval Product Specification

Issue date: 2015/03/21

Version: 2.2

Customer		
Approved by Customer		
Approved by CMEL		
PD Division	ENG Division	QA Dept

1. Purpose:

This documentation defines general product specification for OLED module supplied by Samsung. The information described in this technical specification is tentative. Please Contact Samsung's representative while your product is modified.

2. General Description:

- Driving Mode: Active Matrix.
- Color Mode: Full Color (262K color)
- Driver IC: S6E63D6, COG Assembly
- Interface:

1. Serial data transfer interface (SPI)
2. RGB 16-bit bus interface (DOTCLK, VSYNC, HSYNC, DE, DB17-0)

- Application: Cell phone etc..
- RoHS Compatible

3. Mechanical Data:

No.	Items	Specification	Unit
1	Diagonal Size	2.6"	Inch
2	Resolution	240 xRGBx320	
3	Pixel Pitch	0.055 x0.164	mm
4	Active Area	39.60 x52.48	mm
5	Outline Area(Glass)	44.7 x62.2	mm
6	Thickness	1.65 (Typ)	mm
7	Weight	11 (Typ) g	

4. Absolute Maximum ratings:

4.1 Absolute ratings of environment :

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-40	+80	°C	(1)
Operating Ambient Temperature	T _{OP}	-20	+60	°C	(2)

Note (1) The storage duration for both critical temperature (-40 & 80) meet reliability test criteria.

(2) The operating duration for both critical temperature (-20 & 60) meet reliability test criteria.

4.2 Electrical absolute ratings :

Item	Symbol	Unit	Value
Power supply voltage 1	AR_Vdd	V	+4.6V +/- 0.05
Power supply voltage 2	AR_Vss	V	-4.4V +/- 0.1
Power supply voltage 3	VCI	V	+2.5 ~ +3.3
Power supply voltage 4	VDD3 (IOVcc)	V	+1.65 ~ +3.3

5. Electrical Characteristic:

5.1 DC Characteristic

(Ta = -40°C ~ 85°C, VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Driving voltage	VGH	-	3.0	-	8.0	V	
	VGL	-	-8.0	-	-3.0	V	
	VINT	-	-4.0	-	-1.0	V	
Logic Operating Voltage	RVDD	-	1.45	1.5	1.55	V	
Operating frequency	fosc	Frame frequency = 60Hz Display line = 320 line	1161.1	1290.2	1419.3	kHz	
1st booster input voltage	VCI1	-	2.1	-	2.75	V	
1st booster output voltage	VLOUT1	Without load	+4.6	-	+5.5	V	
1st booster output efficiency	VLOUT1	I _{VLOUT1_LOAD} = 2.3mA	90	95	-	%	
2nd booster output voltage	VLOUT2	Without load	-	7.8	-	V	
2nd booster output efficiency	VLOUT2	I _{VLOUT2_LOAD} = 0.1mA	90	93	-	%	
3rd booster output voltage	VLOUT3	Without load	-	-10.6	-	V	
3rd booster output efficiency	VLOUT3	I _{VLOUT3_LOAD} = 0.1mA	90	93	-	%	
Source Output voltage deviation (channel to channel)	-	-	-	±5	-	mV	
Source Output voltage difference (nearest channel)	-	20 Gray Pattern	-	5	-	mV	
Output voltage deviation (Chip to Chip)	-	-	-	±15	-	mV	
Output voltage deviation (Chip to Chip)	-	-	-	±15	-	mV	
Source driver output voltage range	Vso	-	0.3	-	4.2	V	
Driving voltage	dVGH	voltage deviation	-	-	300	mV	
	dVGL	voltage deviation	-	-	300	mV	
Current consumption during normal operation	IVDD3	No load, Ta = 25 °C	-	1.0	5.0	μA	*1
	IVCI		-	3.5	4.0	mA	
Stand by mode current	IVDD3	Ta = 25 °C	-	0.1	5.0	μA	
	IVCI		-	10	20	μA	

Note

1) VDD3=1.8V, VCI=2.8V, fosc=1290.2KHz (320 display line), NL[5:0]="10_1000", SAP[2:0]="101", DC22[2:0]="100", DC12[2:0]="010", BT[1:0]=10, VQ[3:0]="1000", VGH[4:0]="10100", VGL[4:0]="10100", VINT[3:0]="2101"

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Power Supply Voltage	VCI	Operating Voltage	2.5	2.8	3.3	V	
Power Supply Voltage	VDD3	I/O supply Voltage	1.65	1.8	3.3	V	
Logic High level input voltage	V _{IH}		0.7*VDD3		VDD3	V	
Logic Low level input voltage	V _{IL}		0.0		0.3*VDD3	V	
Logic High level output voltage	V _{OH}	I _{OUT} = -1mA	0.8*VDD3		VDD3	V	
Logic Low level output voltage	V _{OL}	I _{OUT} = +1mA	0.0		0.2*VDD3	V	
Analog High level output voltage	EL_ON _{OH}	8uA	1.8		VCI	V	
Analog Low level output voltage	EL_ON _{OL}	8uA	0		0.3	V	

Table 81. DC Characteristics 3

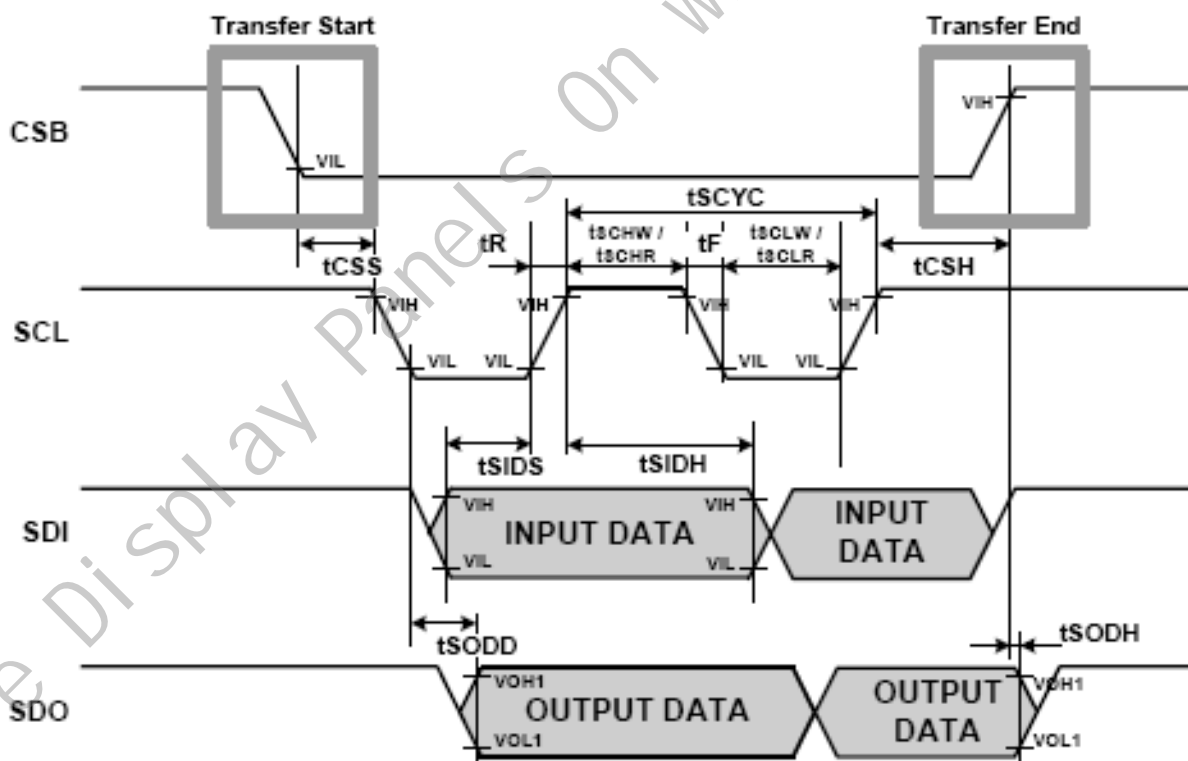
(VDD3 = 1.65-3.3V, VCI = 2.5-3.3V, Ta = 25°C)

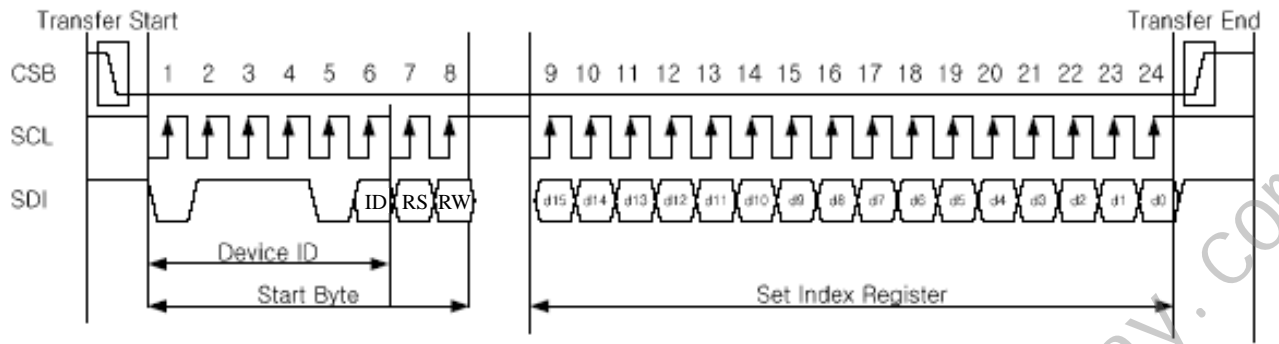
Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
VREG1OUT			4.185	4.2	4.215	V	

5.2.3 SPI

(VDD3 = 1.65 to 3.3V, TA = -40 to +85°C)

Characteristic	Symbol	Specification		Unit
		Min.	Max.	
Serial clock write cycle time	tSCYC	130	-	ns
Serial clock read cycle time	tSCYC	250	-	ns
Serial clock rise / fall time	tR, tF	-	15	ns
Pulse width high for write	tSCHW	50	-	ns
Pulse width high for read	tSCHR	110	-	ns
Pulse width low for write	tSCLW	50	-	ns
Pulse width low for read	tSCLR	110	-	ns
Chip select setup time	tCSS	20	-	ns
Chip select hold time	tCSH	60	-	ns
Serial input data setup time	tSIDS	30	-	ns
Serial input data hold time	tSIDH	30	-	ns
Serial output data delay time	tSODD	-	130	ns
Serial output data hold time	tSODH	5	-	ns





(Note) RS = 0 : Index data
RS = 1 : Parameter data

More Display Panels On www.panoxdi.com

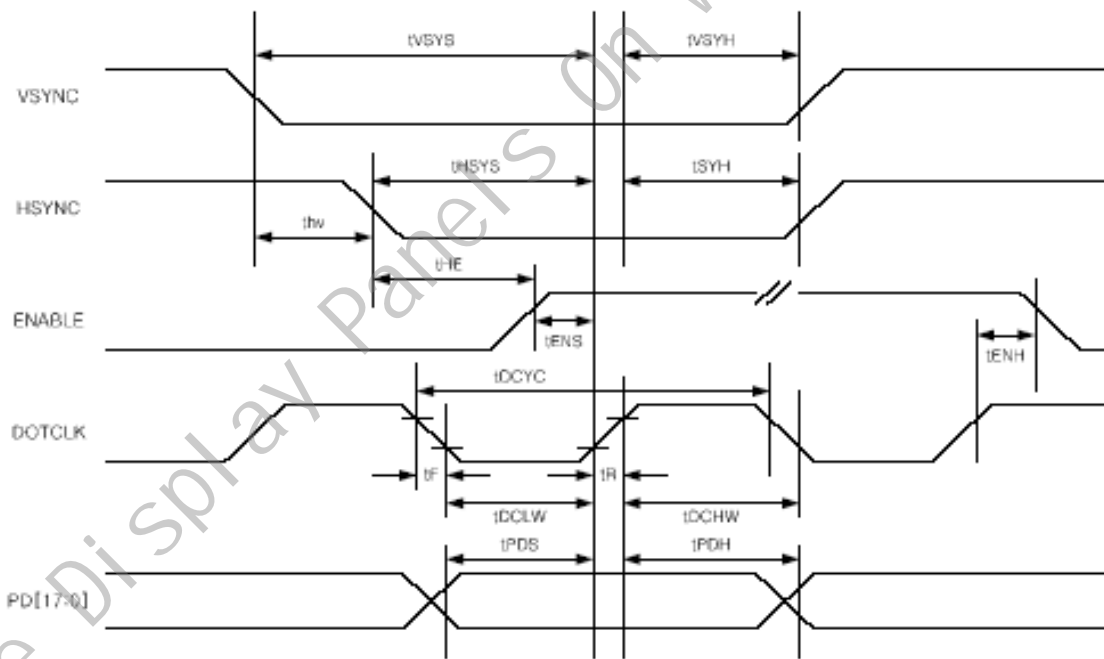
5.2.4 RGB Interface

(VDD3 = 1.65 to 3.3V, TA = -40 to +85°C)

Characteristic	Symbol	Specification		Unit		Unit
		Min.	Max.	Min.	Max.	
DOTCLK cycle time	tDCYC	850	-	-	-	ns
DOTCLK rise / fall time	tR, tF	-	-	-	-	ns
DOTCLK pulse width high	tDCHW	-	-	-	-	ns
DOTCLK pulse width low	tDCLW	-	-	-	-	ns
Vertical sync setup time	tVSYN	30	-	30	-	ns
Vertical sync hold time	tVSYH	30	-	30	-	ns
Horizontal sync setup time	tHSYN	30	-	30	-	ns
Horizontal sync hold time	tHSYH	30	-	30	-	ns
ENABLE setup time	tENS	30	-	30	-	ns
ENABLE hold time	tENH	20	-	20	-	ns
PD data setup time	tPDS	30	-	30	-	ns
PD data hold time	tPDH	20	-	20	-	ns
HSYNC-ENABLE time	tHE	1	HBP	1	HBP	tDCYC
VSYN-HSYN time	tHV	1	175	1	527	tDCYC

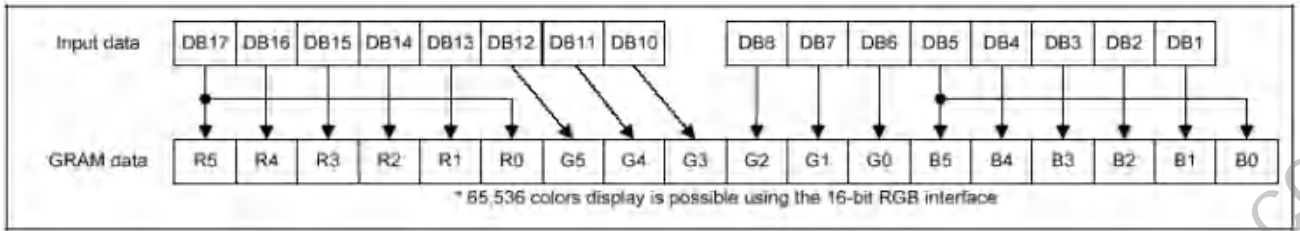
Note

1. HBP is horizontal back-porch.



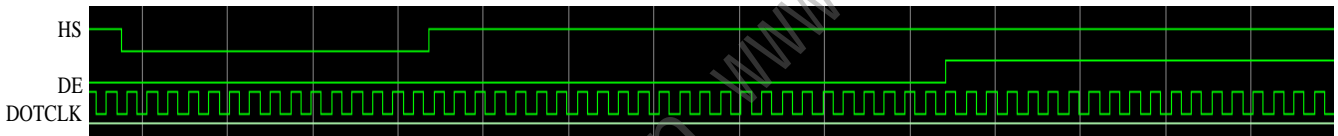
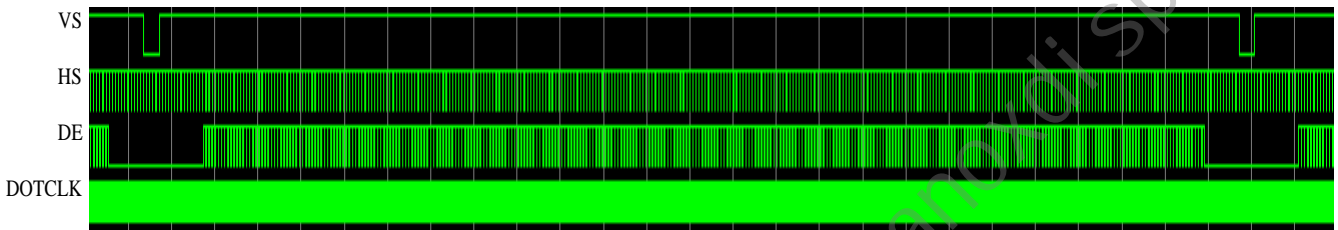
(When VSPL=0, HSPL=0, DPL=0, EPL=1)

Image Data format for 16bit RGB interface (56k color)



Input Oscillogram

一>.输入波形图 (VS/HS/DE/DOTCLK)



DE: 高电平有效

Data: 在 DOTCLK下降沿时把显示数据输出, HIGH8BIT:D17~D10, LOW8BIT: D8~D1

注意: DOTCLK > 940ns

二>.SPI 初始化

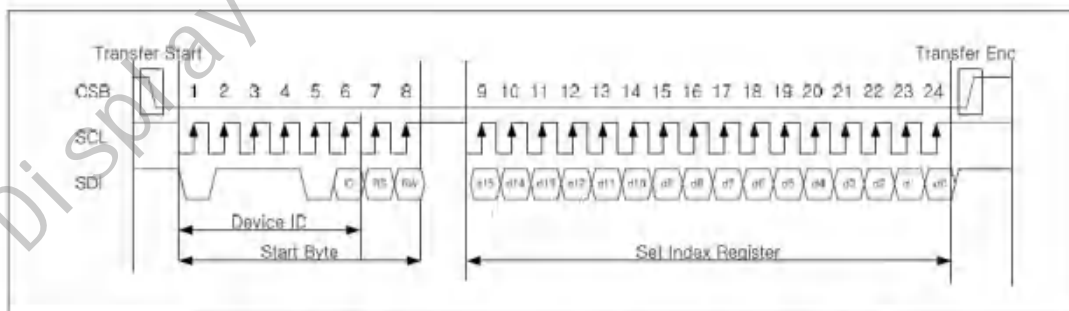


Figure49: Basic Timing Diagram of Register Data Transfer through SPI

Start Byte: 70H----command 72H----para

例如: 700003H 为 command 721020H 为 para

1>.Command:0003h

Para:1020h

2>.Command:0010h

Para:0000h

3>.Command:0005h

Para:0001h

4>.Command:0080h

Para:0001h

5>.Command:0070h

Para:2e80h

6>.Command:0071h

Para:3080h

7>.Command:0072h

Para:3c80h

8>.Command:0073h

Para:1511h

9>.Command:0074h

Para:1c05h

10>.Command:0075h

Para:0076h

11>.Command:0076h

Para:1a14h

12>.Command:0077h

Para:1a15h

13>.Command:0078h

Para:1c18h

14>.Command:0043h

Para:0000h

15>.Command:0005h

Para:0001h

16>.Command:0002h

Para:0193h

17>.Command:0020h

Para:00EFh

18>.Command:0021h

Para:0000h

19>.Command:0022h

More Display Panels On www.panoxdisplay.com

6. Electro-Optical Characteristic:

Items	Symbol	Min	Typ.	Max	Unit	Remark
Operating Luminance	L	170	200	230	Cd/m ²	(1)(5)
Power Consumption	Pon	-	260	300	mW	30% pixels on (1)
Max. Current	Icc	-	-	120	mA	(1)
Response Time	Tres	-	-	50	us	(2)
CIE _x (White)	W _x	0.26	0.31	0.36	-	(5)
CIE _y (White)	W _y	0.28	0.33	0.38	-	(5)
CIE _x (Red)	R _x	0.62	0.66	0.70	-	(5)
CIE _y (Red)	R _y	0.30	0.34	0.38	-	(5)
CIE _x (Green)	G _x	0.25	0.29	0.33	-	(5)
CIE _y (Green)	G _y	0.62	0.66	0.70	-	(5)
CIE _x (Blue)	B _x	0.11	0.15	0.19	-	(5)
CIE _y (Blue)	B _y	0.12	0.16	0.20	-	(5)
Viewing Angle	VA	160	170	-	Degree	(3)
Contrast	CR	5000:1	10000:1	-	-	(4)
Operation Lifetime	LTop	30000	-	-	Hrs	(1)(6)

Note:

Measuring surrounding: dark room

Surrounding temperature: 25°C

IOVCC = 1.65V ~ 3.3V

1. Test condition:

a. AR_VDD= 4.6V +/- 0.03V, AR_VSS= -4.4V +/- 0.03V

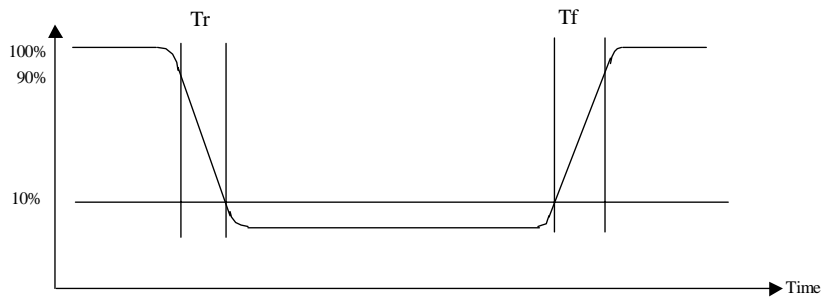
b. IC Initial Register Setting:

R03: 0x0030 // 16bit mode
R10: 0x0000 // IC stand by off
R18: 0x0028 // Frame Rate=80Hz
RF8: 0x000F // VGH=+5V
RF9: 0x0019 // VGL=-7V
R05: 0x0001 // Display On

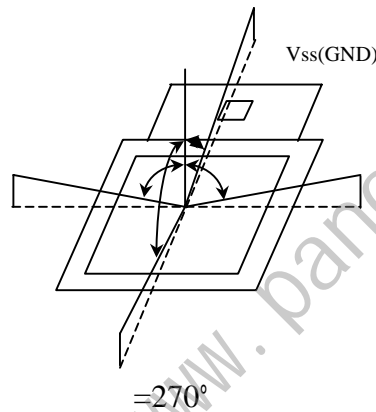
Gamma Register Setting: (Gamma Setting Group : C)

R70h 0x2B00
R71h 0x2C00
R72h 0x3280
R73h 0x2523
R74h 0x2319
R75h 0x2C24
R76h 0x251A
R77h 0x2D2A
R78h 0x281B

2. response Time test condition



3. Viewing angle test condition:



$$\text{Viewing Angle} = \text{CR} > 10$$

4. Contrast

$$\text{CR} = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

5. Optical tester: CA210

6. Brightness of 30% power consumption. Operating Life Time is defined when the luminance has decayed to less than 50% of the initial measured luminance before life test.

8. Pin Assignment:

PIN	Symbol	I/O	Description	Remarks
1	AR_VDD	I	Positive voltage for OLED	
2	AR_VSS	I	Negative voltage for OLED	
3	VCI	I	Power supply for analog circuit(2.5v~3.3v)	
4	NC			
5	GND	I	Ground	
6	NC			
7	NC			
8	NC			
9	NC			
10	NC			
11	NC			
12	NC			
13	NC			
14	NC			
15	NC			
16	NC			
17	NC			
18	NC			
19	VGS	I	A reference level for the grayscale voltage generation circuit. (connect to gnd)	
20	IOVCC	I	I/O power supply	
21	SPB	I	Select the CPU interface mode. (0=parallel interface 1=serial interface)	
22	ID_MIB	I	Select the CPU type (0=intel 80x-system 1=motorola 68x-system)	
23	DB17	I/O	BI-directional data bus.	
24	DB16	I/O	When RGB I/F 18-bit interface : DB 17-0	
25	DB15	I/O	16-bit interface : DB 17-10, DB 8-1	
26	DB14	I/O		
27	DB13	I/O		
28	DB12	I/O		
29	DB11	I/O		
30	DB10	I/O	Fix unused pin to the VSS level	
31	DB9	I/O		
32	DB8	I/O		
33	DB7	I/O		

34	DB6	I/O				
35	DB5	I/O				
36	DB4	I/O				
37	DB3	I/O				
38	DB2	I/O				
39	DB1	I/O				
40	DB0	I/O				
41	VSYNC	I	Frame-synchronizing signal. (VSPL=0 Low active, VSPL=1 High active) FIX this pin at VSS level if the pin is not used			
42	HSYNC	I	Line-synchronizing signal. (HSPL=0 Low active, HSPL=1 High active) FIX this pin at VSS level if the pin is not used			
43	DOTCLK	I	Input pin for clock signal of external interface : dot clock. DPL=0 Display data is fetched at DOTCLK's rising edge DPL=1 Display data is fetched at DOTCLK's falling edge Fix this pin at VSS level if the pin is not used.			
44	ENABLE	I	Data enablesignal pin for RGB interface.			
			EPL	ENABLE	GRAM write	GRAM address
			0	0	Valid	Updated
			0	1	Invalid	Held
			1	0	Invalid	Held
1	1	Valid	Updated			
45	SDI (SDIN)	I	For a serial peripheral interface (SPI), input data is fetched at the rising edge of the SCL signal, Fix SDI pin at VSS level if the pin is not used.			
46	SDO (SDOUT)	O	For a serial peripheral interface (SPI), serves as the serial data output pin (SDO), Successive bits are output at the falling edge of the SCL signal.			
47	CSB (CS/NCS)	I	Chip select signal input pin. 0= driver IC is selected and can be accessed. 1= driver IC is not selected and cannot be accessed.			
48	RW_WRB (SCL)	I	Pin function	CPU type	Pin description	
			RW	68-system	Read/Write operation selection pin 0=write 1=read	
			WRB	80_system	Write strobe signal.(Input pin) Data is fetched at the rising edge.	
SCL	SPI	The synchronous clock signal				
49	RS	I	Register select pin. 0=Index/status, 1=instruction parameter, GRAM data Must be fixed at VDD3 level when not used.			
50	E_RDB	I	Pin Function	CPU type	Pin description	
			E	68-system	Read/Writeoperation enable pin	
			RDB	80_system	Read strobe signal. Read out data at the low level	
When SPI mode is selected, fix this pin at VDD3 levle						

51	RESETB	I	Reset pin initializes the IC when low. Should be reset after power-on.	
52	NC	O	Internal power for RAM. Connect a capacitance to gnd. Connect a capacitance (1u/10v) to gnd.	
53	NC	O	A reference level for the grayscale voltage. Connect a capacitance (1u/10v) to gnd.	
54	VCI	I	Power supply for analog circuit (2.5v~3.3v)	
55	NC	O	The positive voltage used in the gate driver. Connect a capacitance (1u/10v) to gnd.	
56	NC	O	The negative voltage used in the gate driver. Connect a capacitance (1u/10v) to gnd.	
57	GND		Ground	
58	X-			
59	Y-			
60	X+			
61	Y+			

More Display Panels On www.panoxdi.com

9. Reliability Test:

No.	Items	Specification
1	High Temp. Storage	85°C, 240hrs
2	Low Temp. Storage	-40°C, 240hrs
3	High Temp. Operation	60°C, 240hrs
4	Low Temp. Operation	-40°C, 240hrs
5	High Temp / Humidity Storage	85°C, 85%RH, 240hrs
6	High Temp / Humidity Operation	60°C, 90%RH, 240hrs
7	Thermal shock	-40°C ~85°C (-40°C /30min; transit/3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles
8	Vibration	Frequency: 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z
9	Drop	Height: 76cm Sequence : 1 angle, 3 edges and 6 faces Cycles: 1
10	ESD	Air discharge model, ±8kV, 10 times

Test and measurement conditions

- All measurements shall not be started until the specimens attain to temperature stability.
- The degradation of Polarizer is ignored for item 1, 5 & 6.
- The test pattern at operating condition is 30%P.C. alternating pictures.

Evaluation Criteria

- No damage to glass or encapsulation
- No drastic change to display
- Defects / Mura follow product specification
- Luminance: Within +/-50% of initial value
- Current consumption: within +/-50% of initial value

10. Handling:

- 10.1 Do not scratch the surface of the polarizer film as it is easily damaged.
- 10.2 When cleaning the display surface, use soft cloth with solvent (as recommended below) and wipe lightly
 - Ethyl alcohol
 - Isopropyl alcohol
- 10.3 Do not wipe the display surface with dry or hard materials that damage the polarizer surface.
- 10.4 Since this OLED panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.
- 10.5 Do not disassemble the OLED module as it may cause permanent damage.
- 10.6 Hold OLED very carefully when placing OLED module into the system housing. Do not excessive stress or pressure to OLED module.

11. Storage

- 11.1 Storing in a polyethylene bag with the opening sealed.
- 11.2 Placing in a dark place where neither exposure to direct sunlight nor any fluorescent light is permitted and keep at room temperature & room humidity.
- 11.3 Storing with no contact with polarizer surface.

(It is recommended to store them in the inner container which we delivered.)

9. External Dimension:

