Hong Kong Panox Electronics Co.,Ltd

PRDDUCT SPECIFCATION

CUSTOMER		
Approved 核 准	**Checked** 审 核	**Prepared** 确认

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Contents

Document Revision History

Change No.	Date	Subject And Reason	Version No.	Responser
1	2020.10.20	New	00	

1.0General Description

1.1 Introduction

AU080L1280Mis a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel and a driving circuit.This TFT LCD has a 8.0 inch diagonally measured active display area with (800 horizontal by1280 vertical pixe l) resolution.

1.2. Features

8 inch configuration
ROHS design

1.3. General information

Item	Specification	Unit
Outline Dimension	114.6 (H) x 184.1(V) x2.6(D)	mm
Display area	107.64 (H) x 172.224(V)	mm
Number of Pixel	800 RGB (H) x 1280(V)	pixels
Pixel pitch	44.85um (H) x 134.55um (V)s	mm
Pixel arrangement	RGB Vertical stripe	
Display mode	Normally Balck	
Color Filter Array	RGB vertical stripes	
Backlight	White LED	
Weight	TBD	g

2.0 Absolute Maximum Ratings

.2.1 Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Operating Temperature	Topa	-10	60	℃	
Storage Temperature	Tstg	-20	70	℃	

2.2 Back-light Unit:

PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
LED Current	IF	–	140	–	mA	–	–
LED Voltage	VF	9	9.9	10.5	V	–	–
Life Time		–	20000	–	Hr.	I≦140mA	–
Color	White						

Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions.

(2)Ta=25±2℃

(3)Test condition: LED Current 140mA

3.0 Optical Characteristics

3.1 Optical specification

Item	Symbol	Condition	Values			Unit	Remark
			Min.	Typ.	Max.		
Viewing angle (CR≥ 10)	θ_L	Φ=180°(9 o'clock)	70	80	-	degree	Note 1
	θ_R	Φ=0°(3 o'clock)	70	80	-		
	θ_T	Φ=90°(12 o'clock)	70	80	-		
	θ_B	Φ=270°(6 o'clock)	70	80	-		
Response time	T_{ON}	Normal θ=Φ=0°	-	10	20	msec	Note 3
	T_{OFF}		-	15	30	msec	Note 3
Contrast ratio	CR			500	-	-	Note 4
Color chromaticity	W_X		0.26	0.31	0.36	-	Note 2 Note 5 Note 6
	W_Y		0.28	0.33	0.38	-	
Luminance	L		200	250	-	cd/m²	Note 6
Luminance uniformity	Y_U		70	75	-	%	Note 7

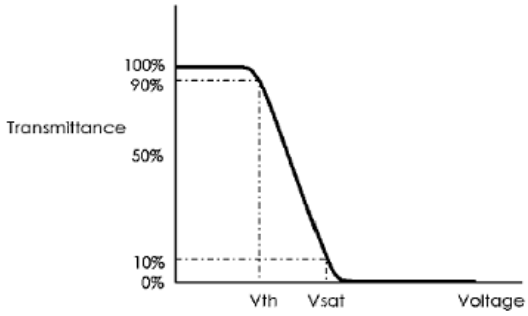
3.2 Measuring Condition

- ■ Measuring surrounding : dark room
- ■ Ambient temperature : 25±2℃
- ■ 30min. warm-up time.

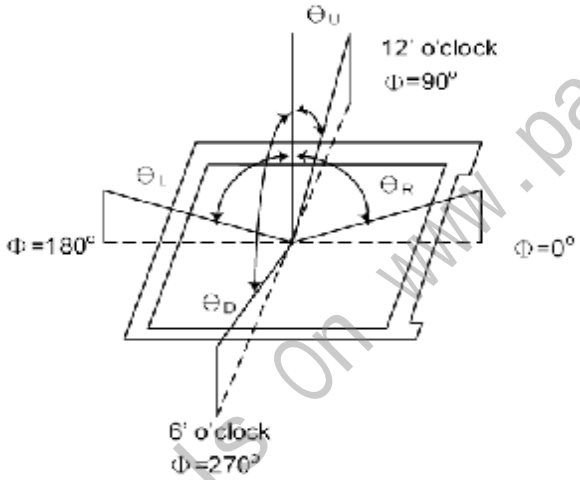
3.3 Measuring Equipment

- ■ TOPCON BM-7
- ■ Measuring spot size : field 2°

Note (1) Definition of Vsat and Vth (at 20℃)



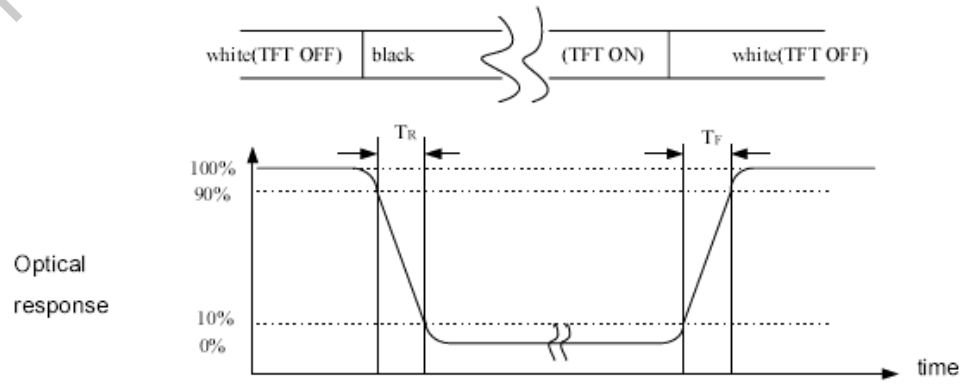
Note (2) Definition of Viewing Angle :



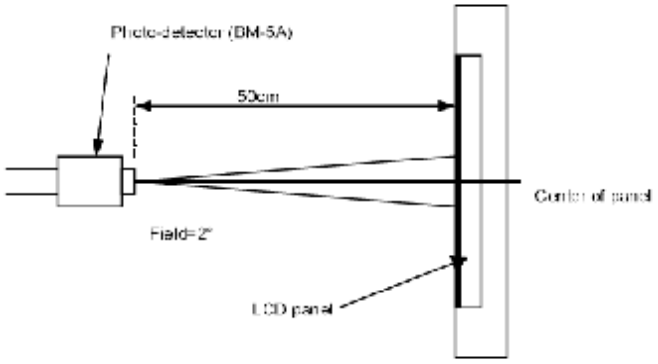
Note (3) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

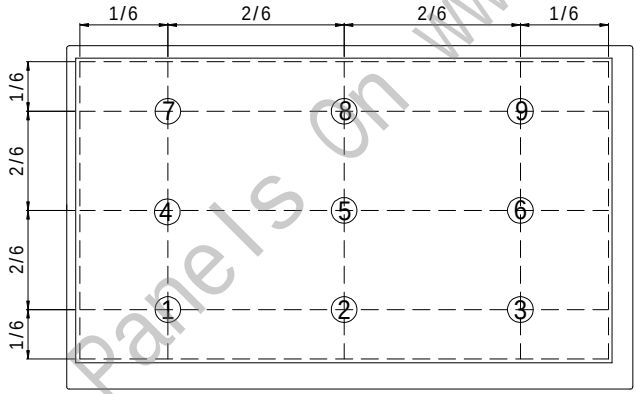
Note (4) Definition of Response Time : Sum of T_R and T_F



Note (5) Definition of optical measurement setup



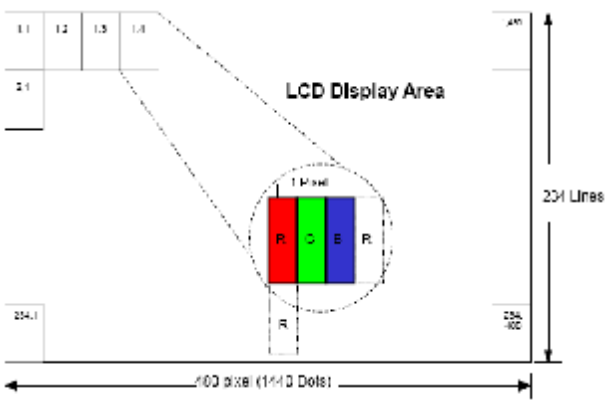
Note (6) Definition of brightness uniformity



Note (7) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.

4.0 Block Diagram

4.1 TFT-LCD Module



5.0 Interface Pin Connection

PIN NO	SYMBOL	DESCRIPTION
1	LEDA	Power for LED backlight(Anode)
2	LEDA	Power for LED backlight(Anode)
3	LEDA	Power for LED backlight(Anode)
4	NC	No connect
5	LEDK	Power for LED backlight(Cathode)
6	LEDK	Power for LED backlight(Cathode)
7	LEDK	Power for LED backlight(Cathode)
8	LEDK	Power for LED backlight(Cathode)
9	GND	Ground
10	GND	Ground
11	MIPI_D2+	HSSI_D2_Pare differential small amplitude signals
12	MIPI_D2-	HSSI_D2_Nare differential small amplitude signals
13	GND	Ground
14	MIPI_D1+	HSSI_D1_Pare differential small amplitude signals
15	MIPI_D1-	HSSI_D1_Nare differential small amplitude signals
16	GND	Ground
17	MIPI_CLK+	HSSI_CLK_Pare differential small amplitude signals
18	MIPI_CLK-	HSSI_CLK_Nare differential small amplitude signals
19	GND	Ground
20	MIPI_D0+	HSSI_D0_Pare differential small amplitude signals
21	MIPI_D0-	HSSI_D0_Nare differential small amplitude signals
22	GND	Ground
23	MIPI_D3+	HSSI_D3_Pare differential small amplitude signals
24	MIPI_D3-	HSSI_D3_Nare differential small amplitude signals
25	GND	Ground
26	NC	
27	RESET	Reset signal
28	NC	
29	VDD1V8	I/O power supply
30	VDD3V3	Power supply 3.0-3.6V
31	VDD3V3	Power supply 3.0-3.6V

6. Electrical Characteristics

6.1 TFT LCD Module

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	VDD1V8	1.7	1.8	2.0	V	
	VDD3V3	3.0	3.3	3.6	V	
Input signal voltage	V_{IH}	0.7DV_{DD}	-	DV_{DD}	V	
	V_{IL}	0	-	0.3DV_{DD}	V	
Power Current	I_{VDD3V3}	-	135	--	mA	

6.2Power on/off sequence

VCI, VCIP and IOVCC can be applied in any order. VCI, VCIP and IOVCC can be powered down in any order.

During power off, if the display module is in the SLPOUT mode, VCI, VCIP and IOVCC must be powered down minimum 120msec after RESX has been released.

During power off, if the display module is in the SLPIN mode, VCI, VCIP and IOVCC can be powered down minimum 0msec after RESX has been released.

There will be no damage to the display module if the power sequences are not met.

There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

There will be no abnormal visible effects on t he display panel between end of Power On Sequence and before receiving SLPOUT co mmand. Also between receiving SLPOUT command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence as defined in

Sections 9.5.2, then it will be necessary to apply a Hardware Reset (RESX) after Host

Power On Sequence is complete to ensure correct operation. Other wise function is not guaranteed.

There is not a limit for Rise/Fall time on VCI, VCIP and IOVCC.

6.3 **MIPI Signal Timing Characteristics**

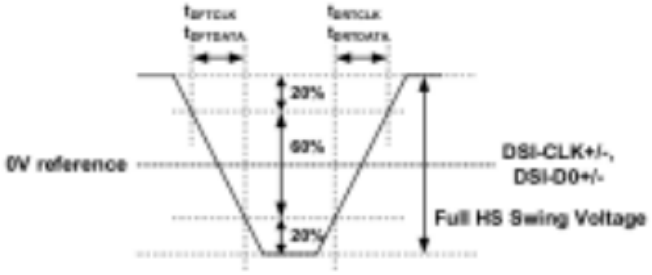
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs (UI = UIINSTA = UIINSTB)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	tDS	Data to clock setup time	0.15x UI	-	-	ps	
DSI-Dn+/-	tDH	Data to clock hold time	0.15x UI	-	-	ps	
DSI-CLK+/-	tDRTCLK	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDRTDATA	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	tDFTCLK	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	tDFTDATA	Differential fall time for data	150	-	0.3xUI	ps	

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.

DSI clock channel timing



Rising and fall time on clock and data channel

7.0 Reliability test items

NO	Item	Conditions	Remark
1	High Temperature Storage	Ta=+70℃,24hrs	
2	Low Temperature Storage	Ta=-20℃,24hrs	
3	High Temperature Operation	Ta=+60℃,24hrs	
4	Low Temperature Operation	Ta=-10℃,24hrs	
5	High Temperature and High Humidity (operation)	Ta=+40℃,90%RH,24hrs	
6	Thermal Cycling Test (non operation)	-20℃(0.5hr)→+70℃(0.5hr),200cycles	
7	Electrostatic Discharge	150pf/330Ω/±8KV air & contact test 200pf/0Ω/±4KV contact test	

Note: All tests above are practiced at module type.

There is no display function NG issue occurred, All the cosmetic specification is judged before the reliability stress.

8.0 Outline dimension