1.39”Smartwatch
Product Specification
Rev. P7

Customer Name	:	
Product Name	:	1.39” Smartwatch
Model Name	:	BOE139F454SM
Description	:	1.39” (454x454) Smartwatch AMOLED

Proposed by			Customer’s Approval
Designed	Checked	Approved	

Revision History

Rev.	ECN No.	Description of Change	Date	Prepared
P0	-	Initial issue	Mar.16.2016	
P1		1. Modify 2D draw 2. Modify Pin assignment	Mar.19.2016	
P2		1. Add SPI description 2. Add Idle mode power consumption 3. Add Code information 4. Add RT4723 PWR IC information 5. Add Package information	May.9.2016	
P3		1. Delete SPI description 2. Delete Main FPCB Drawing 3. Modify Pin assignment 4. Modify 2D draw	Jun.15.2016	
P4		1. Modify COF name 2. Modify Pin assignment 3. Modify Total Information 4. Add Main FPCB Drawing 5. Add TSL2584TSV information 6. Modify Packing Information	Sept.13.2016	
P5		1. Modify Pin assignment	Dec.27.2016	
P6		1. Modify Initial Code and Idle Code 2. Modify Electro-optical Characteristics 3. Modify Total outline	Mar.09.2017	
P7		1. Modify Initial Code and Idle Code 2. Modify Idle mode power consumption	Apri.11.2017	

Content

1. General Description

1-1. Introduction

BOE 1.39inch 454x454 is a color active matrix AMOLED module using Low Temperature Poly-silicon TFT's (Thin Film Transistors) as active switching devices. This module has a 1.39inch diagonally measured active area with 454x454 resolutions (454horizontal by 454 vertical pixel arrays). Each pixel is divided into RED, GREEN, BLUE dots and this module can display 16.7M colors.

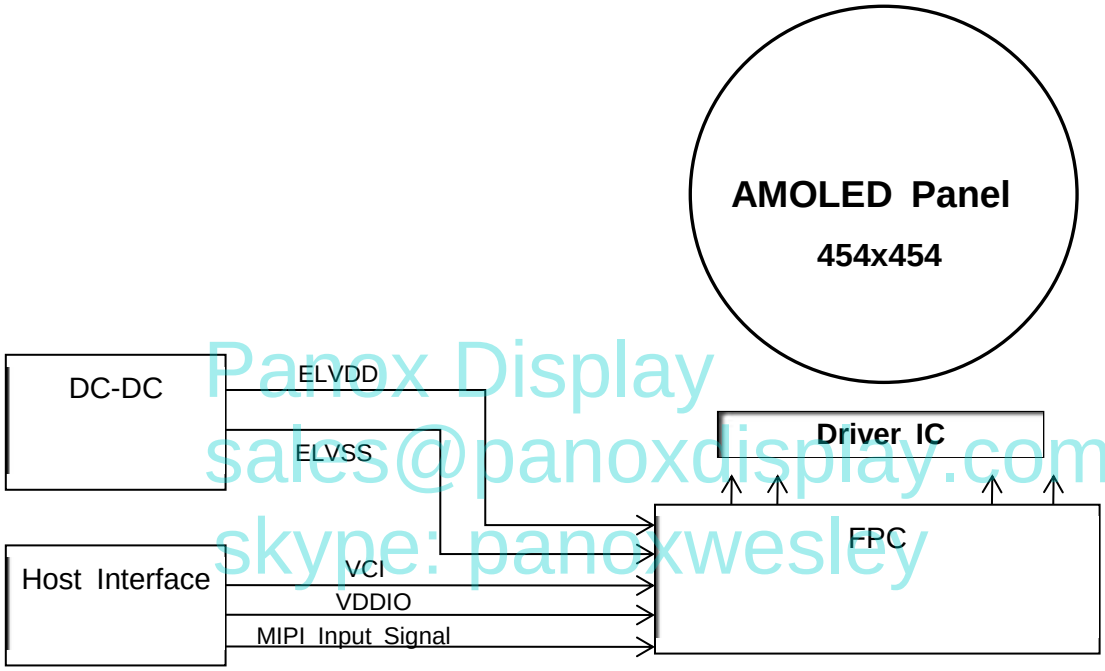


Figure 1

1-2. Features

1) Display Colors : 16.7M
2) Display Format : 1.39" OLED 454x454
3) MUX: source 1：6
4)Interface : MIPI1-lane
5) Driver IC :RM67162FI
6) Polarizer : Circular Type Polarizer

1-3. Application

- Smartwatch

2. Mechanical Specification

Table 1

Item		Specifications	Unit	Remark
Glass outline		38.212(W)x39.372(H)x0.5(T)	mm	
Number of dots		454(W)RGB×454(H)	Dots	
Active area		35.412(W)×35.412(H)	mm	
Diagonal Inch		1.39	inch	
Pixel pitch		78(W)×78(H)	um	
Pixel Arrangement		Real RGB		
Module Size	Display Panel(POL+Glass+Tape)	38.212(W)x39.372(H)×0.893(T)	mm	
Weight		2.65	g	

3. Absolute Maximum Ratings

Table 2

Item	Symbol	Min.	Max.	Unit	Note
I/O Voltage	VDDIO	-0.3	5.5	V	
Operation Voltage	VCI	-0.3	5.5	V	
EL Driving Voltage	ELVDD	4.5	4.7	V	
	ELVSS	-0.4	-4.0	V	
Operating temperature	Topr	-20	70	℃	-
Storage temperature	Tstg	-40	85	℃	-

4. Electrical Characteristics

Test Condition: Temp=25±2℃

Table 3

Item		Symbol		Condition	Symbol	Min.	Typ.	Max.	Uni	Remark
ELVDD		ELVDD		-	-	4.55	4.6	4.65	V	Fixed 4.6V
ELVSS		ELVSS		-	-	-0.6	-2.4	-4	V	100mV Step
VCI		VCI		-	-	2.7	3.0	3.6	V	
VDDIO		VDDIO		-	-	1.65	1.8	3.3	V	
Power Consumption	Display on mode	IC	VCI	100% Pixel On,350nits, 60Hz	Ivci	4	5	6	mA	
					Pvc	12	15	18	mW	
			VDDIO		Ivddio	2	3	6	mA	
					Pvddio	3.6	5.4	10.8	mW	
		Panel	EL		Inl	21	23	25	mA	
					Pnl	147	161	175	mW	
	Idle mode	IC	VC	10% Pixel On,50nits, 30Hz	Ivci	3	4.5	7	mA	
					Pvci	9	13.5	21	mW	
			VDDIO		Ivddio	1.1	1.5	2.5	mA	
					Pvddio	1.98	2.7	4.5	mW	
	Sleep mode	-	VCI	-	Ivci	20	30	40	uA	
					Pvci	0.06	0.09	0.12	mW	
			VDDIO		Ivddio	20	30	40	uA	
					Pvddio	0.036	0.054	0.072	mW	
	F_{frm}					59	60	61	Hz	

5. Electro-optical Characteristics

Table 4

Item		Symbol	Temp	Condition	Min.	Typ.	Max.	Unit	Note
Brightness			25℃	Normal (White pattern)	300	350	-	cd/m^2	Center brightness
Uniformity			25℃	Normal (White pattern)	75	85	-	%	(1)
Contrast ratio		K	25℃	Φ=0°,θ=0°	10,000	20,000	-	-	(2)
Color of CIE coordinate	White	u’	25℃	Φ=0°,θ=0° CIE1976	0.181	0.196	0.211	-	(3)
		v’			0.441	0.456	0.471	-	
	Red	u’			0.439	0.471	0.500	-	
		v’			0.514	0.529	0.539	-	
	Green	u’			0.061	0.081	0.101	-	
		v’			0.569	0.579	0.589	-	
	Blue	u’			0.134	0.164	0.188	-	
		v’			0.116	0.146	0.210	-	
Color Gamut			25℃	NTSC ，CIE1976	98	105	-	%	(3)
Viewing Angle			25℃	Up/Down/Right/Left CR ratio ≥10	75	80	-	°	(3)
Color temp			25℃	-	6500	7500	8500	K	
Crosstalk			25℃	Background: gray128	-	-	3	%	(4)
Luminance decrease ratio			25℃	30°	-	-	45	%	(5)
Color Shift(White)			25℃	30°	-	-	7	JNCD	(6)
Life Time			25℃	LT94	150	-	-	hrs	
Response time			25℃	-	-	-	3	ms	(7)
Gamma			25℃	-	1.9	2.2	2.5	-	
Long time Image Sticking			25℃	Light on for 150hrs	Luminance≥94			%	(8)
Short time Image Sticking			25℃	Light on a Black &White 350nit for 10 sec and then Change to 128 Gray	-	-	20	sec	(9)

Notes :

(1) Uniformity Measuring Point

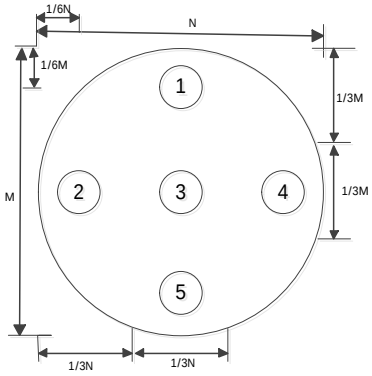


Figure 2

Uniformity=Lmin/Lmax *100%

(2) Definition of contrast ratio(K)

$$\mathrm{CR} = \frac{\text{Luminance When Display panel is at “White” state}}{\text{Luminance When Display panel is at “Black” state}}$$

(3) Optical &viewing angle measuring system

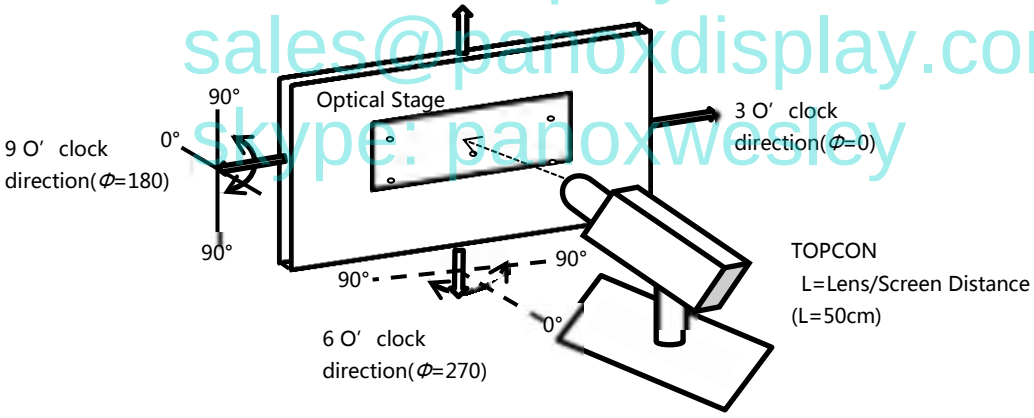


Figure 3

Definition of Color of CIE Coordinate and NTSC Ratio

$$S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} * 100\%$$

(4) The point should be marked is, the background of Cross-talk Test Pattern-“gray “ are defined as middle gray scale . For example, RGB 24bit “gray” defined as below:

$$\mathrm{Vx} = \mathrm{Max}\{\frac{\mathrm{A1}-\mathrm{A1}'}{\mathrm{A1}'}, \frac{\mathrm{A2}-\mathrm{A2}'}{\mathrm{A2}'}, \frac{\mathrm{B1}-\mathrm{B1}'}{\mathrm{B1}'}, \frac{\mathrm{B2}-\mathrm{B2}'}{\mathrm{B2}'}\}$$

$$\mathrm{Hx} = \mathrm{Max}\{\frac{\mathrm{A3}-\mathrm{A3}'}{\mathrm{A3}'}, \frac{\mathrm{A4}-\mathrm{A4}'}{\mathrm{A4}'}, \frac{\mathrm{B3}-\mathrm{B3}'}{\mathrm{B3}'}, \frac{\mathrm{B4}-\mathrm{B4}'}{\mathrm{B4}'}\}$$

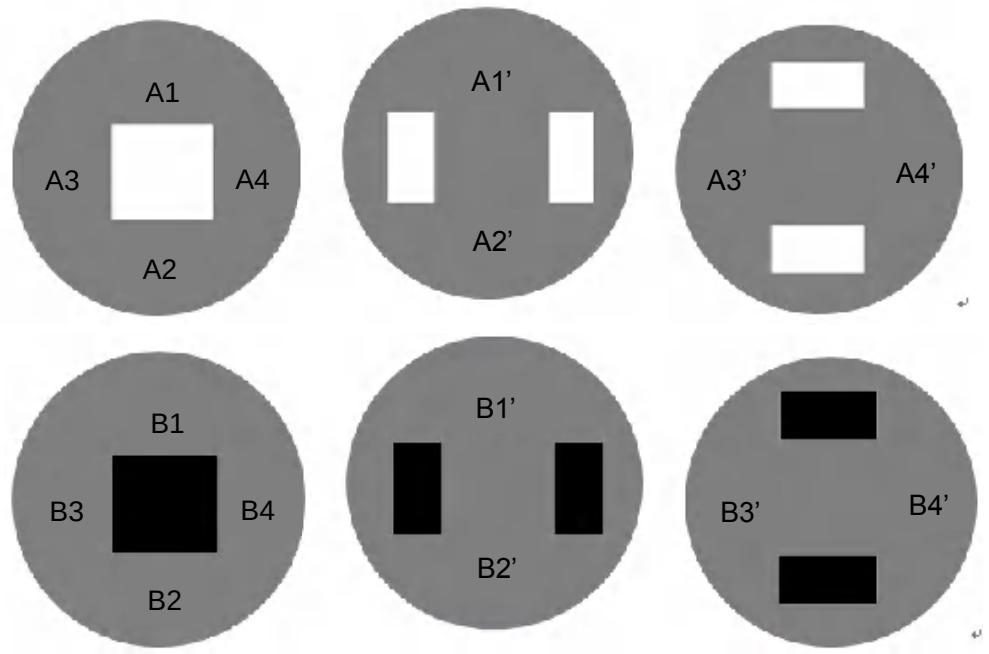


Figure 4. crosstalk measuring pattern

(5) Definition of Luminance decrease ratio

Test pattern : Full White

The luminance decrease ratio is calculated by using following formula:

$$\text{Luminance decrease ration} = 1 - \frac{\text{Luminance test at left, right, top, bottom} = 30°}{\text{Luminance test at left, right, top, bottom} = 0°}$$

(6) Color Shift JNCD

For JNCD measure:

Fix on one pattern like white pattern,

On the condition θ=0 Ø=0 °, we can get the color coordinate (u1', v1') and on 30 °we can get another color coordinate (u2', v2')

Delta = Square Root((u2' - u1')^2 + (v2' - v1')^2)

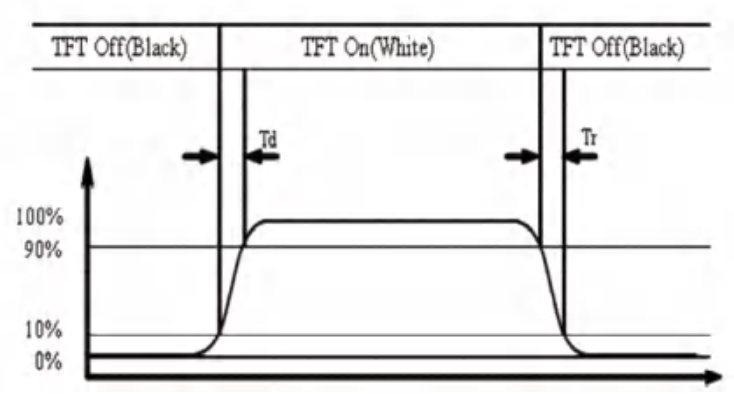
JNCD stands for "Just Noticeable Color Difference"

For the (u', v') color space JNCD=0.0040.

2JNCD means Delta u'v'<0.0080

For color shift we need to measure white/red/green/blue pattern

(7) The output signals of photo detector are measured when the input signals are changed from “black” to “white”(Voltage falling time) and from “white” to “black”(Voltage rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



(8)OLED Long time image sticking

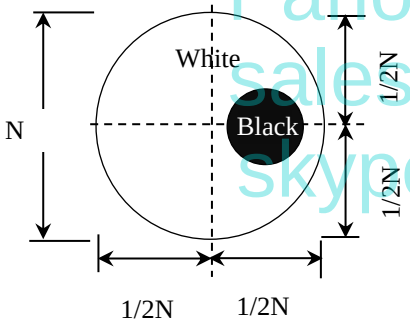
Test samples 30pcs;

1)At room temperature(25℃), light the module with 255 gray pattern which display a white pattern, but with a black dot, the dot size based on the test equipment's detector.

2)Keep Lighting150 hours;

3)Then change to an full white pattern, measure the brightness data of White area and Black area;

The test data must pass the specification.



Pattern: white pattern with black dot

Circular center lines up with horizontal center line of AA
Based on the test detector

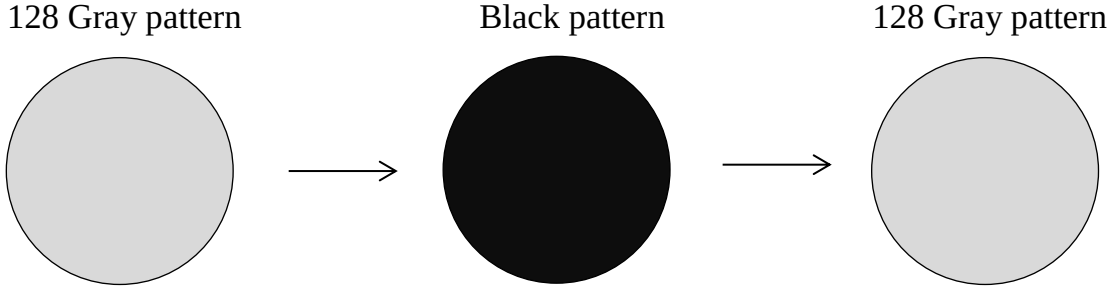
(9)OLED Short time image sticking

Test samples 5pcs;

1)Light on a 128 gray pattern for 10s;

Change to a Black pattern, and light on this pattern for 10 seconds;

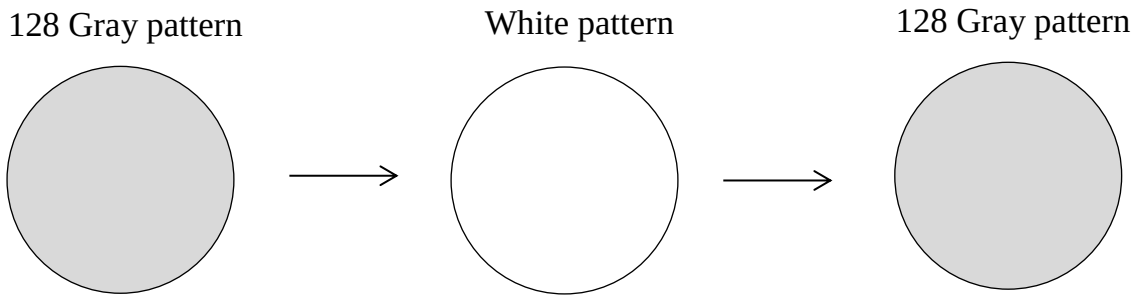
Then change the pattern back to 128 gray, See Figure below.



2)Light on a 128 gray pattern for 10s;

Change to a White pattern, and light on this pattern for 10 seconds;

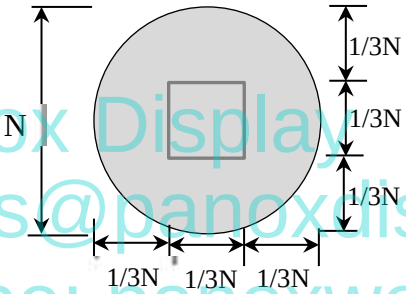
Then change the pattern back to 128 gray, See Figure below.



When change the pattern back to 128 gray, at same time start to use CCD measure the luminance, the CCD exposure time is 0.3sec;

Measure 60 times and each interval step 1sec;

Capture the useful luminance data as below pattern;



Calculate the contrast as below method:

$$x = \frac{\text{Imax} - \text{Imin}}{\text{Imax} + \text{Imin}}$$

Record the time which satisfy the x value less than 0.005(JND);

This time value must within the module spec.

6. FPC Pin Assignment

Main FPC assignment- AMOLED Panel Input/output Signal Interface.

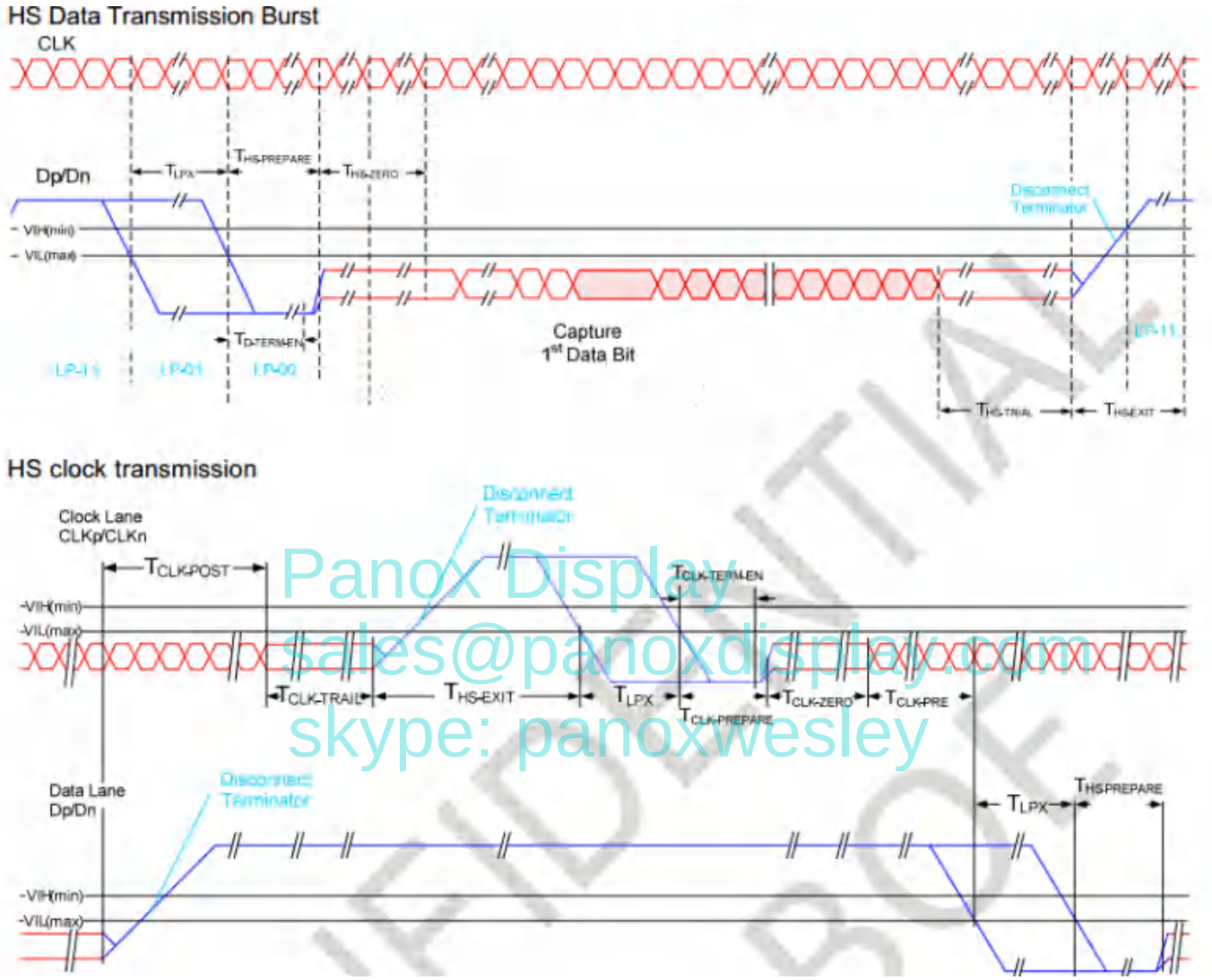
Connector type: AXG220144

Table 5

Pin number	Pin name	I/O	Description
1	ELVSS	P	AMOLED negative power supply
2	ELVSS	P	AMOLED negative power supply
3	ELVSS	P	AMOLED negative power supply
4	VCI	P	Driver analog power supply
5	VDDIO	P	Power supply for interface system
6	GND	P	Ground
7	TE	O	Tearing effect output pin to synchronize MCU to frame writing
8	MTP	P	MTP programming power supply pin (7.5V typical)
9	RESX	I	Device reset signal (0 : Enable1: Disable)
10	SWIRE	O	SWIRE signal for PWR IC control
11	GND	P	Ground
12	CLKP	I	MIPI positive clock signal
13	CLKN	I	MIPI negative clock signal
14	GND	P	Ground
15	D0P	I/O	MIPI positive data signal
16	D0N	I/O	MIPI negative data signal
17	GND	P	Ground
18	ELVDD	P	AMOLED positive power supply
19	ELVDD	P	AMOLED positive power supply
20	ELVDD	P	AMOLED positive power supply

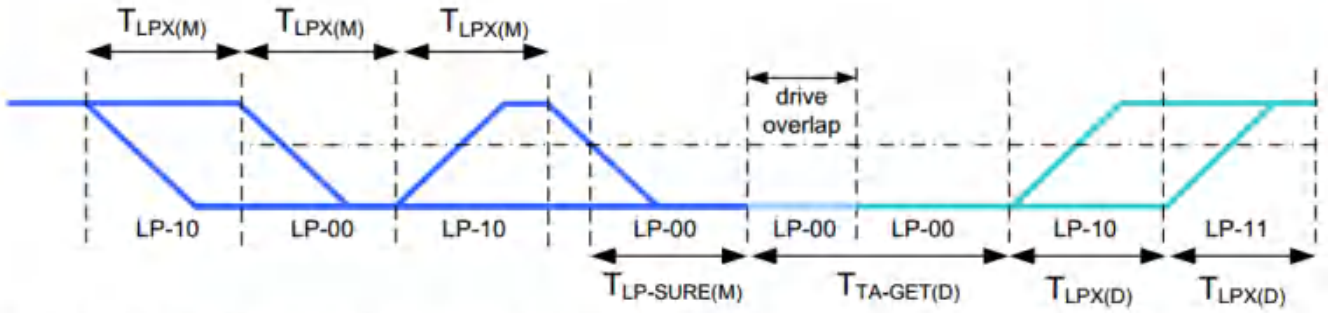
7. AC Characteristics

7-1.MIPI DSI Timing Characteristics

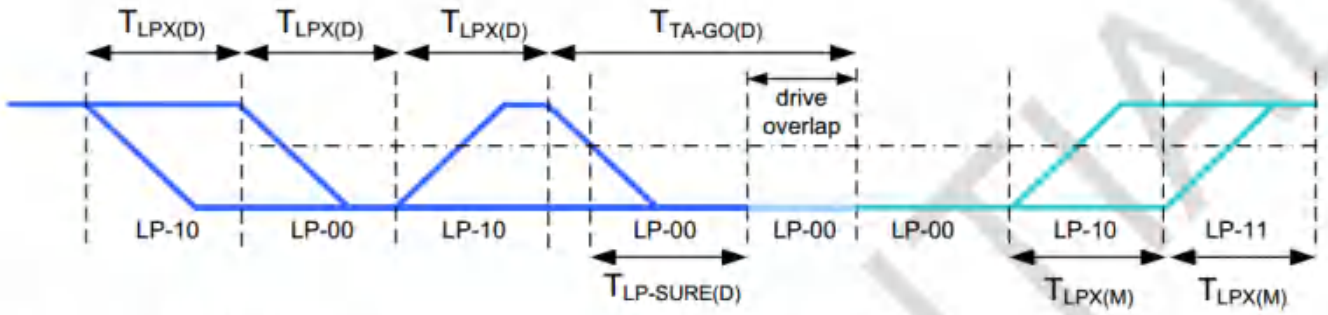


Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	**300**			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	**$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.**	**145ns + 10*UI**			**ns**
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

Low Power Mode :

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns	2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns	2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns	2

NOTE:
1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

8. Recommended Operating Sequence

8-1. Display Power on/off Sequence

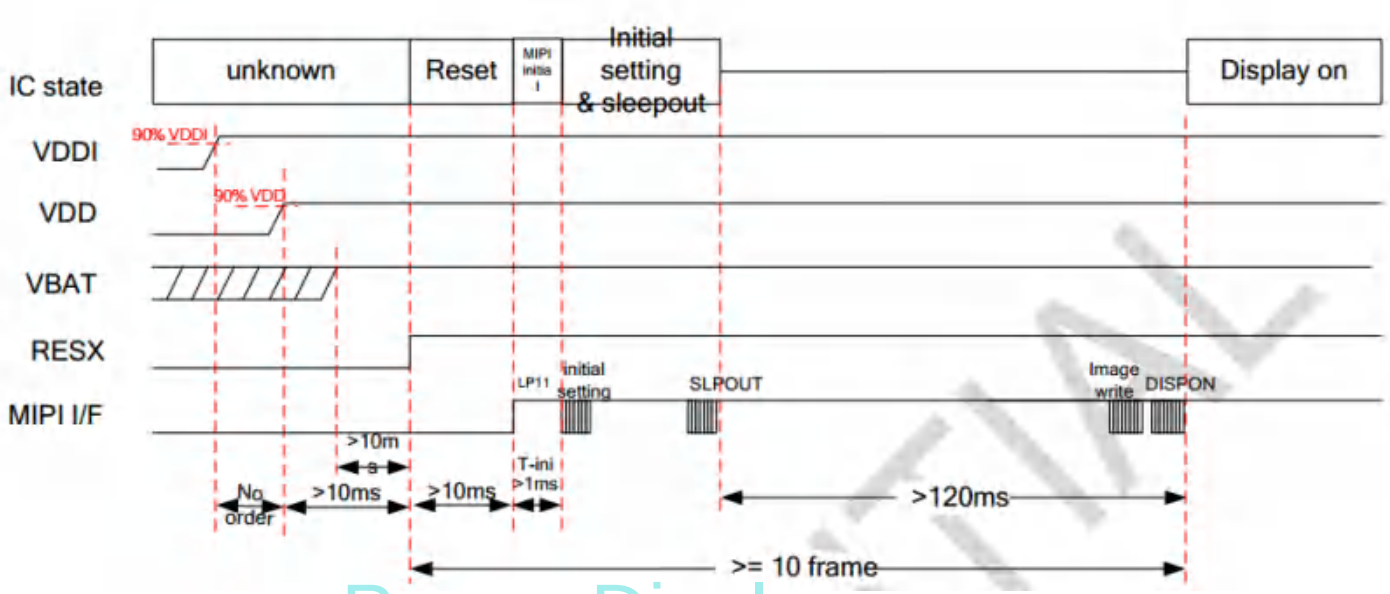


Figure 5 Power On to Display On Sequence

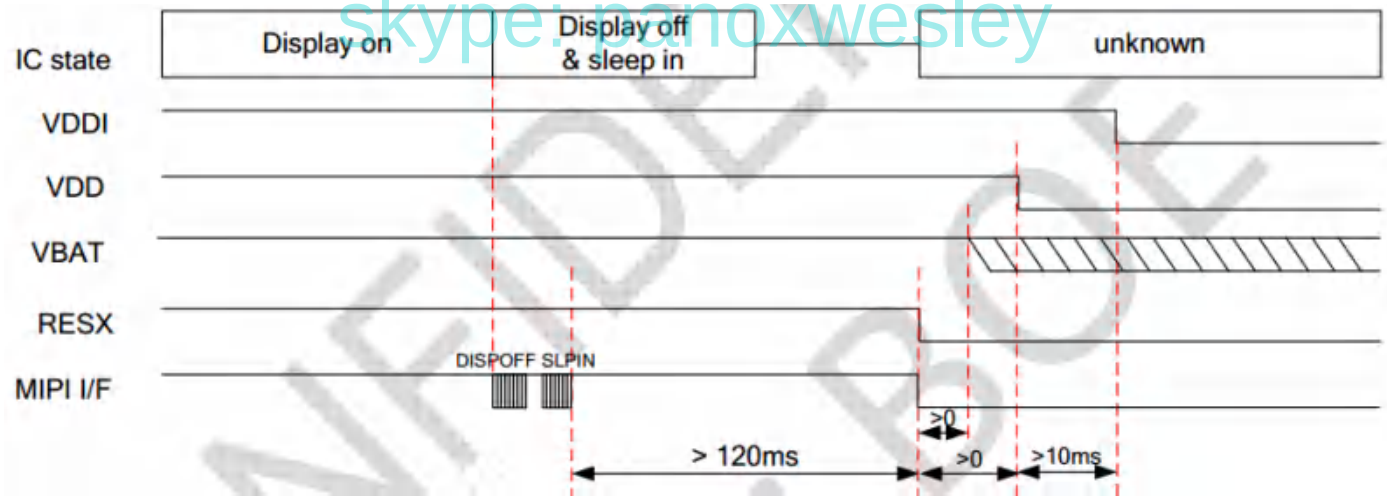


Figure 6 Display Off to Power Off Sequence

9. Code Information

9-1. Initial code

Power on;
wait 20ms;
Reset;
wait 20ms;
mipi 0x23 0xFE 0x01;
mipi 0x23 0x70 0x55;
mipi 0x23 0xFE 0x0A;
mipi 0x23 0x29 0x10;
mipi 0x23 0xFE 0x05;
mipi 0x23 0x05 0x01;
mipi 0x23 0xFE 0x00;
mipi 0x23 0x35 0x00;

mipi 0x39 0x2A 0x00 0x0C 0x01 0xD1;
mipi 0x39 0x2B 0x00 0x00 0x01 0XC5;
mipi 0x13 0x11;
wait 120ms;
mipi 0x13 0x29

wait 20ms;

9-2. Idle mode code

Into idle mode code:

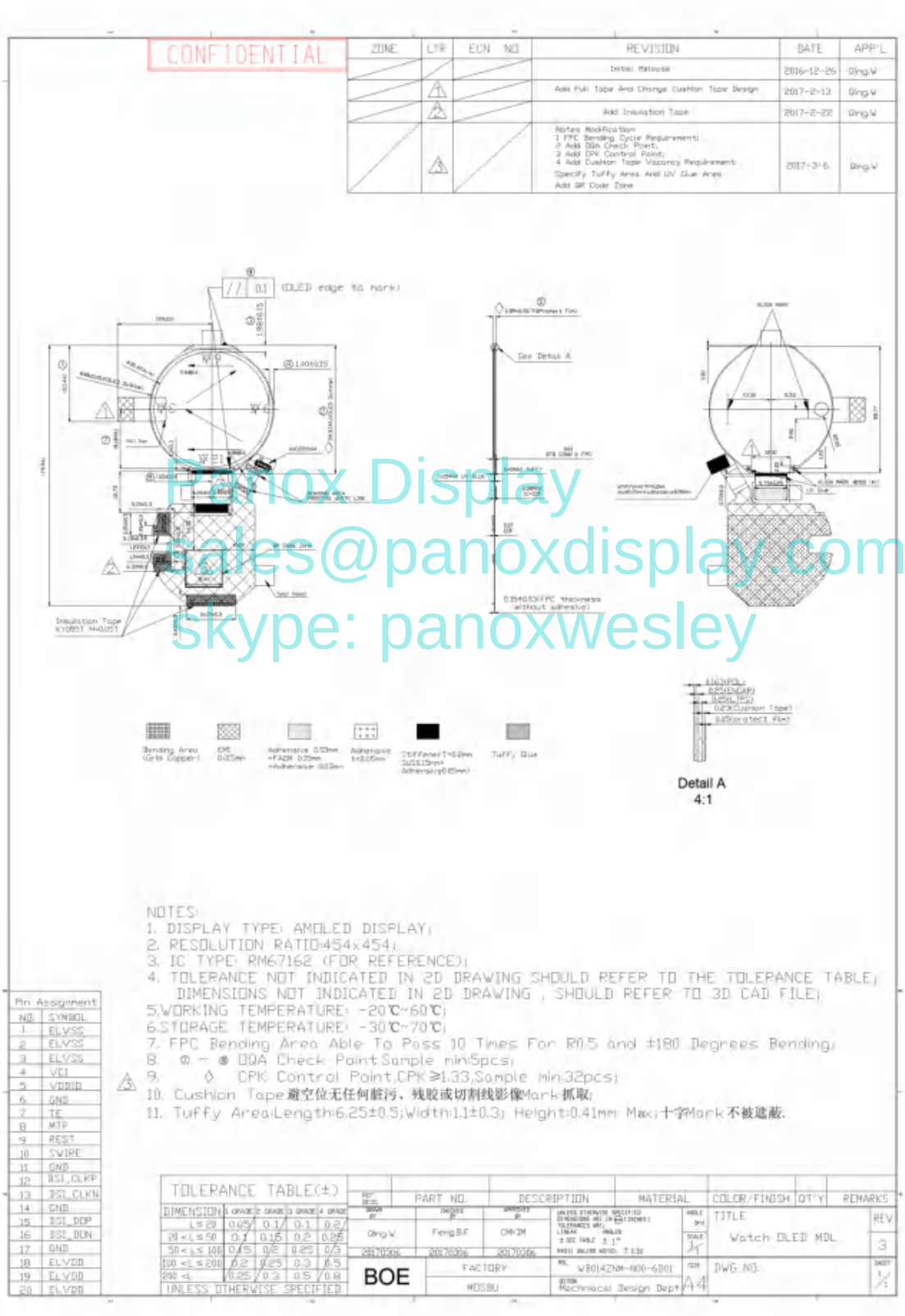
mipi 0x23 0xFE 0x01;
mipi 0x23 0x36 0x00;
mipi 0x23 0x14 0xA0;
mipi 0x23 0xFE 0x04;
mipi 0x23 0x1B 0x8D;
mipi 0x23 0xFE 0x02;
mipi 0x23 0x00 0x03;
mipi 0x23 0x01 0xff;
mipi 0x23 0x34 0x03;
mipi 0x23 0x35 0xff;
mipi 0x23 0x69 0x03;
mipi 0x23 0x6a 0xff;
mipi 0x23 0xFE 0x05;
mipi 0x23 0x05 0x01;
mipi 0x23 0xFE 0x00;
mipi 0x13 0x39;

Out idle mode code:

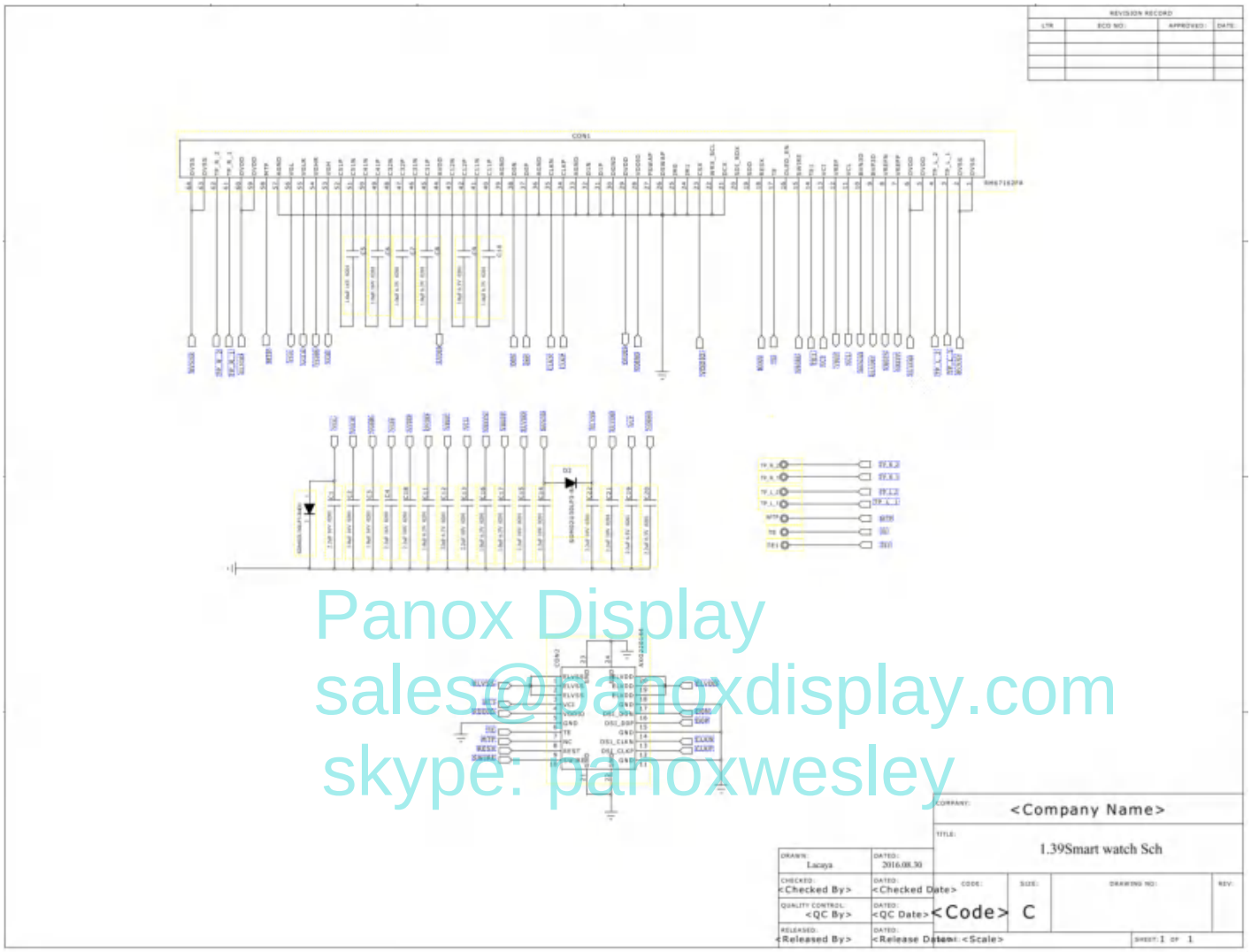
mipi 0x23 0xFE 0x01;
mipi 0x23 0x36 0x22;
mipi 0x23 0xFE 0x00;
mipi 0x13 0x38;

10. Outline Information

10-1. Total Outline

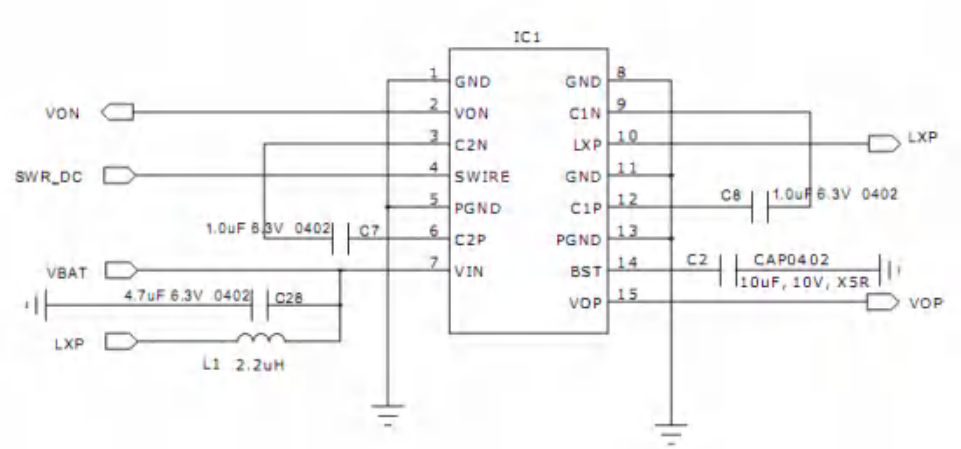


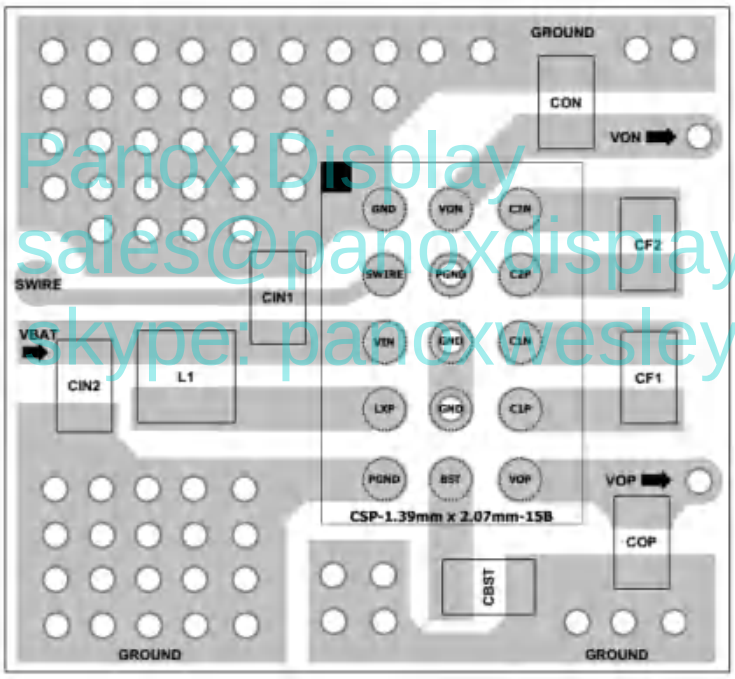
10-2. Main FPCB Drawing



11. IC informatiom

11-1. RT4723 PWR IC information





12. Reliability Test

No.	Item			Condition
1	High Temperature Storage test(HTS)			70℃,240hr
2	Low Temperature Storage test(LTS)			-30℃,240hr
3	High Temperature Operating test(HTO)			60℃,240hr
4	Low Temperature Operating test(LTO)			-20℃,240hr
5	Thermal Humidity Operating test(THO)			60℃/90%RH,240hr
6	Thermal Cycle Storage test(TST)			-40℃~80℃, 30cycles,2h/cycle
7	Electrical Static Discharge	Power off	Contact	+2KV/150pF + 330 ohm
			Air	+4KV/150pF + 330 ohm
		Power on	Contact	+6KV/150pF + 330 ohm
			Air	+8KV/150pF + 330 ohm

Judgment criteria: no functional failures

13. Packing Information