SONY

1.3 cm (Type 0.5) Active Matrix Color OLED Panel

ECX331DB-6

Description

The ECX331DB-6 is a 1.3 cm (type 0.5) diagonal, 1024 × 768 dots active matrix color OLED panel module using single crystal silicon transistors. This panel incorporates panel driver and logic driver, and realizes small size, light weight and high definition. It enables full color display in NTSC/PAL progressive system.

(Applications: View finders, head mounted displays, very small monitors etc.)

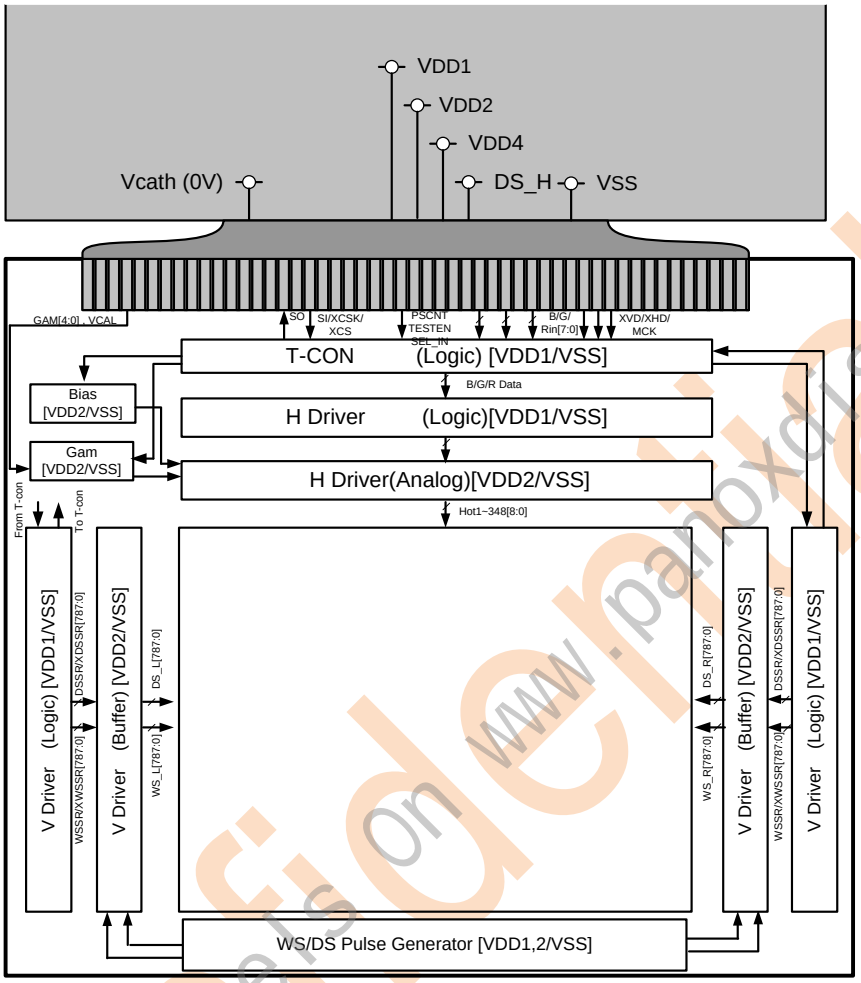
Features

- Small size high definition type 0.5 display dots: 1024 (RGB)×768 = 2.36 M dots
- High contrast
- Wide color reproduction range
- High-speed response
- Thin type and light weight
- Power saving function
- Up/down and/or right/left inverse display function
- Orbit supported

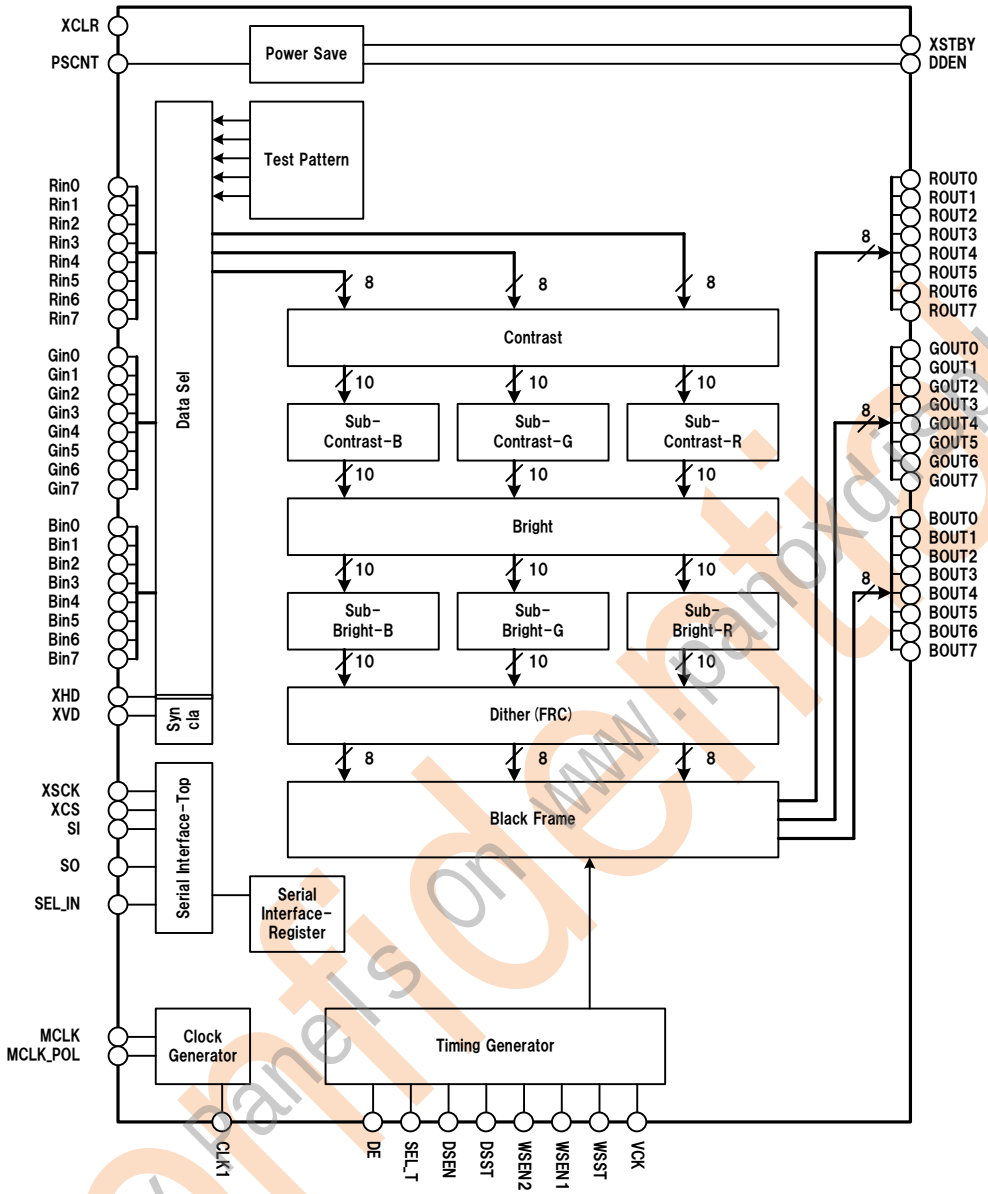
Element Structure

Active matrix color OLED display element with on-chip driver using single crystal silicon transistors

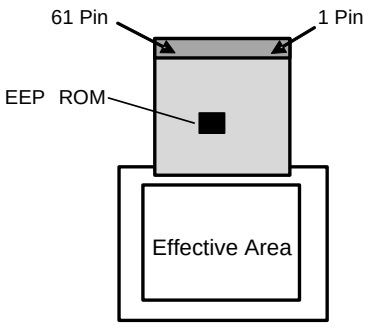
Block Diagram



T-CON Block Diagram



Pin Assignment



EEP ROM

This panel has an EEP ROM on the flexible connector.

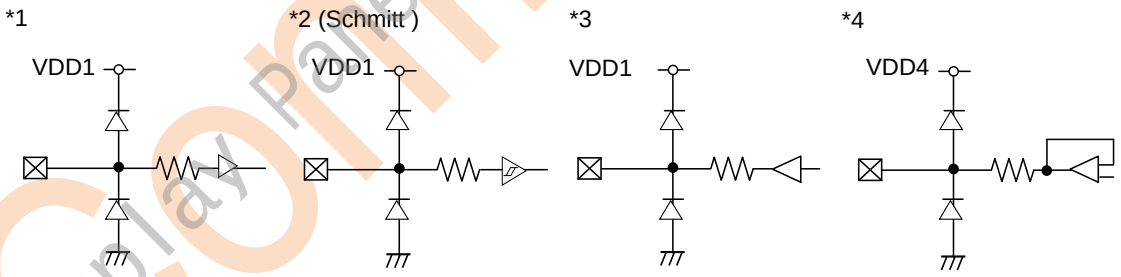
This EEP ROM stores the register setting values used to adjust the luminance and white chromaticity.

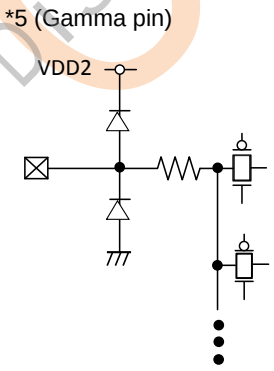
Pin Description

Pin No. (FPC side)	Symbol	Type	Description	Equivalent circuit
1	VSS	Power supply	GND	
2	VDD4	Power supply	10V power supply	
3	DS_H	Power supply	DS-High power supply	
4	VDD2	Power supply	DAC input stage, Data input level shifter DAC selector, Output selector Gamma generation, V driver Amplifier output stage power supply	
5				
6	Vcath	Power supply	EL cathode power supply	
7	VSS	Power supply	GND	
8	VDD 1	Power supply	3 V power supply	
9	MCLK	Input	Clock	*1
10	XHD	Input	Horizontal sync signal	*1
11	XVD	Input	Vertical sync signal	*1
12	XCLR	Input	System reset	*2
13	Rin7	Input	Digital R signal	*1
14	Rin6	Input	Digital R signal	*1
15	Rin5	Input	Digital R signal	*1
16	Rin4	Input	Digital R signal	*1
17	Rin3	Input	Digital R signal	*1
18	Rin2	Input	Digital R signal	*1
19	Rin1	Input	Digital R signal	*1
20	Rin0	Input	Digital R signal	*1
21	Gin7	Input	Digital G signal	*1
22	Gin6	Input	Digital G signal	*1
23	Gin5	Input	Digital G signal	*1
24	Gin4	Input	Digital G signal	*1
25	Gin3	Input	Digital G signal	*1
26	Gin2	Input	Digital G signal	*1
27	Gin1	Input	Digital G signal	*1
28	Gin0	Input	Digital G signal	*1
29	VDD 1	Power supply	3 V power supply	
30	VSS	Power supply	GND	
31	Bin7	Input	Digital B signal	*1
32	Bin6	Input	Digital B signal	*1
33	Bin5	Input	Digital B signal	*1
34	Bin4	Input	Digital B signal	*1
35	Bin3	Input	Digital B signal	*1
36	Bin2	Input	Digital B signal	*1
37	Bin1	Input	Digital B signal	*1
38	Bin0	Input	Digital B signal	*1
39	XSCAN_MODE	Input	Serial communication mode Low: MSB First High: LSB First	*2
40	E2PROM_XCS	Input	Serial communication chip select for EEP ROM	*2
41	E2PROM_WP	Input	Serial communication data write control signal for EEP ROM	*2
42	XCS	Input	Serial communication Chip select	*2
43	XSCK	Input	Serial communication Serial clock (shared with EEP ROM XSCK)	*2

Pin No. (FPC side)	Symbol	Type	Description	Equivalent circuit
44	SI	Input	Serial communication Input data (shared with EEP ROM SI)	*2
45	E2PROM_SO	Output	SO for EEP ROM Serial communication Output data	*3
46	SO	Output	Panel SO Serial communication Output data	*3
47	VDD 1	Power supply	3 V power supply	
48	VSS	Power supply	GND	
49	VCAL	Output	Correction voltage output in temperature compensation circuit	*4
50	VGAM 4	Output	Gamma top reference voltage (255)	*5
51	VGAM 3	Output	Gamma reference voltage (128)	*5
52	VGAM 2	Output	Gamma reference voltage (32)	*5
53	VGAM1	Output	Gamma bottom reference voltage (1)	*5
54	VGAM0	Output	Vofs voltage (0)	*5
55	VSS	Power supply	GND	
56	Vcath	Power supply	EL cathode power supply	
57	VDD 2	Power supply	DAC input stage, Data input level shifter DAC selector, Output selector Gamma generation, V driver Amplifier output stage power supply	
58				
59	DS_H	Power supply	DS-High power supply	
60	VDD4	Power supply	10V power supply	
61	VSS	Power supply	GND	

Equivalent Circuit





Absolute Maximum Ratings

Item	Symbol	Min.	Maximum Ratings	Unit
3 V power supply	VDD1	-0.3	4.0	V
12.5 V power supply	VDD2	-0.3	18.5	V
10 V power supply	VDD4	-0.3	10.3	V
DS-High power supply	DS_H	-0.3	VDD2	V
EL cathode voltage	Vcath	-0.3	VDD2	V
Logic input voltage	Vi	-0.3	VDD1+（0.3）	V
Storage temperature	Tpnl	-30	+80	°C

Recommended Operating Conditions

Item	Symbol	Min.	Typ.	Max.	Unit
3 V power supply	VDD1	2.7	3.0	3.3	V
12.5 V power supply	VDD2	12.0	12.5	13.0	V
10 V power supply	VDD4	9.7	10.0	10.3	V
DS-High power supply	DS_H	12.0	12.5	13.0	V
EL cathode voltage	Vcath	-0.3	0	0.3	V
Clock frequency	fCLK		54.0	54.5	MHz
Operating temperature range	Tpnl	-10		70	°C

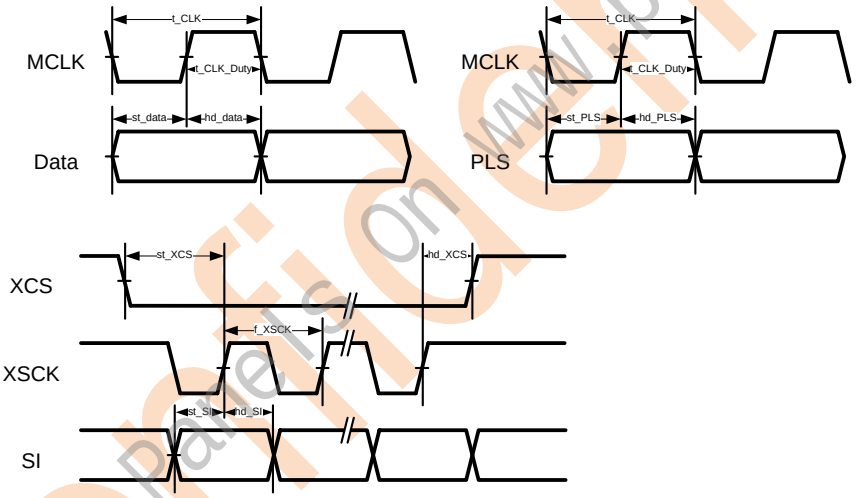
Electrical Characteristics

1. DC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-level input voltage	VIH		0.7VDD1		VDD1	V
Low-level input voltage	VIL		0		0.3VDD1	V
High-level input voltage	Vt+	Schmitt input	0.7VDD1		VDD1	V
Low-level input voltage	Vt-	Schmitt input	0		0.3VDD1	V
Vt+ - Vt-	Vhys	Schmitt input		0.50		V
Logic High -level Output voltage	VOH		VDD1-0.4			V
Logic Low -level Output voltage	VOL				0.4	V

2. AC Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock pulse cycle	t_CLK		15.3	18.5		ns
Clock duty	t_CLK_duty	All mode (54 MHz/40.5 MHz/32.4 MHz) common	40	50	60	%
Data setup time	st_Data	Vi = 2.7 to 3.6 V	2.5			ns
Data hold time	hd_Data	Vi = 2.7 to 3.6 V	1.8			ns
Control pulse setup time	st_PLS	Vi = 2.7 to 3.6 V	2.5			ns
Control pulse hold time	hd_PLS	Vi = 2.7 to 3.6 V	1.8			ns
XSCK frequency	f_SCLK			0.8	2.5	MHz
XCS setup time	st_XCS		0.4			µs
XCS hold time	hd_XCS		0.2			µs
SI setup time	st_SI		0.2			µs
SI hold time	hd_SI		0.2			µs



3. Power Consumption

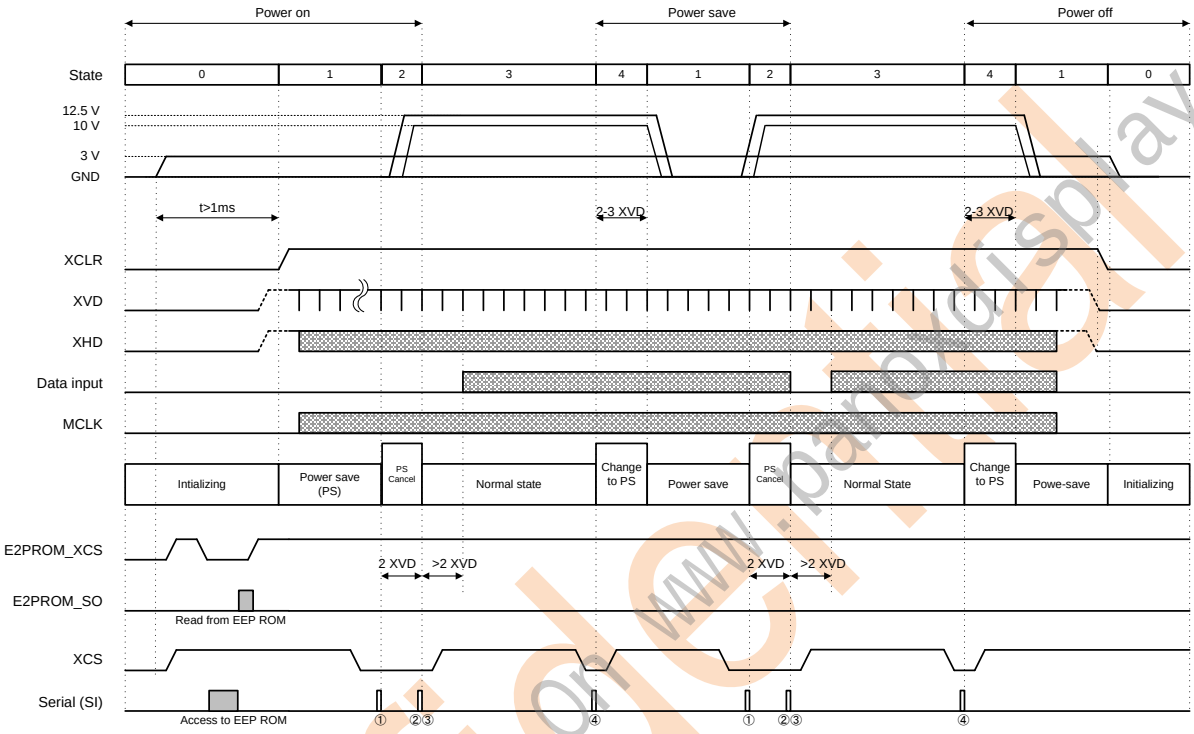
Item	Symbol	Condition	Typ. (*)					Unit
			500	300	200	120	Standby	cd/m^2
VDD1 power consumption	PDD1	Tpnl = 40℃	43				0	mW
VDD2 power consumption	PDD2		107				3.3	mW
VDD4 power consumption	PDD4		0				0	mW
DS-High power consumption	PDS_H		330	195	130	75	0	mW
Total	PTTL		480	345	280	225	3.3	mW

*All white raster, Frame rate=60Hz, Clock=54MHz

Power Supply Sequence

To avoid panel breakdown caused by excessive current flow into the internal circuit, power supply sequence written below should be kept.

1. Sequence Diagram



Serial setting ①	
Address	Data(Hex)
0x00	0E
0x01	(※)
0x02	2A
0x03～2C	(※)
0x34	06
0x00	0F

Serial setting ②	
Address	Data(Hex)
0x00	
0x01	
0x02	
0x03～2C	
0x34	00

Serial setting③	
Address	Data(Hex)
0x00	
0x01	
0x02	28
0x03～2C	
0x34	

Serial setting ④	
Address	Data(Hex)
0x00	0E
0x01	
0x02	
0x03～2C	
0x34	

(※) Setting values are separately presented.

2. Power-On Sequence

1. Set XCLR to low and turn on 3V power supply. Then the panel initializing is perfoemed.
2. After completion of 3V power supply rising, set E2PROM_XCS and XCS to high.
3. Read the register settings from EEP ROM according to 1.2.EEP ROM read timing.
4. Set XCLR to high at an interval of > 1msec after the completion of 3V power supply rising, then the panel changes to power saving (PS) mode.
5. Perform PS off by serial setting ①.

6. Turn on 12.5V power supply, then turn on 10V power supply.
7. Perform the serial setting ② and ③ > 2XVD after the serial setting ① completion.

*Input pulse of XVD, XHD and MCLK should be stable.

*12.5 V power supply should be kept higher voltage than 10V power supply when turning on.

3. Power-Off Sequence

1. Perform PS on by serial setting ④.
2. After power saving mode starts, turn off 10V and 12.5V power supply.
3. Set XCLR to low and turn off 3V power supply.

*12.5 V power supply should be kept higher voltage than 10V power supply, when turning off.

*12.5V and 10V power supply should be under 0.3V when setting XCLR to low and turning 3V power supply off.

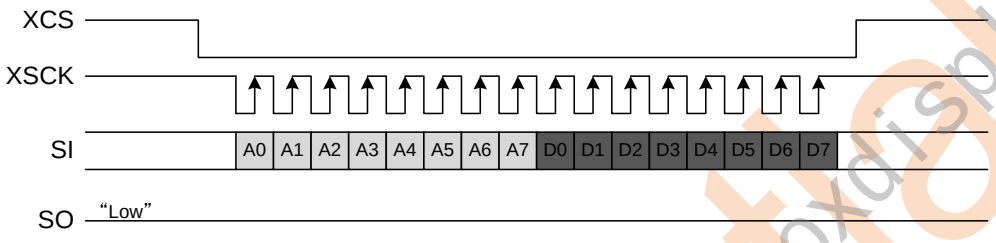
Description of Function

1. T-CON Block

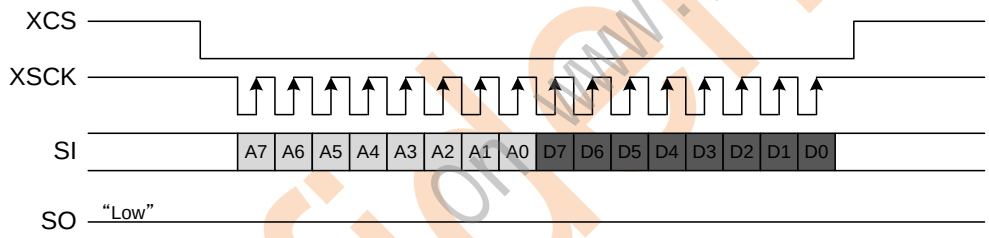
1.1. Serial I/F Transfer Timing

◆ Write

Write operation should be designed to be able to support serial communication.
Switching of the serial communication mode (MSB First / LSB first) is performed by SEL_IN (input pin #39).
Timing of each mode is shown below.



Write access normal transfer (when XSCAN_MODE = High; LSB First)



Write access normal transfer (when XSCAN_MODE = Low; MSB First)

◆ Read

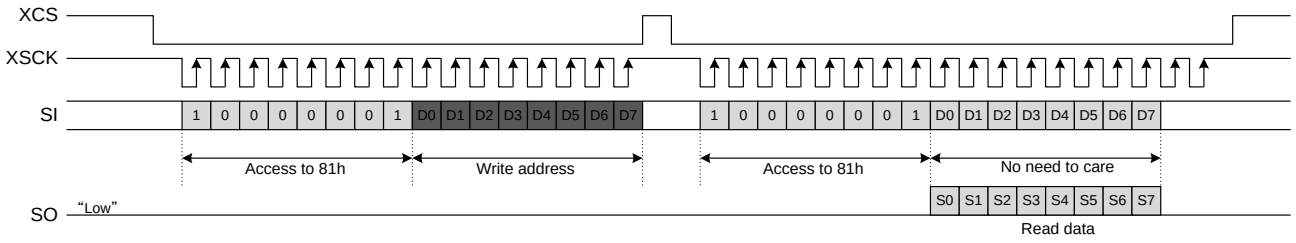
Read operation should be designed to be able to support serial communication (normal transfer, LSB/MSB First).

Read access procedure

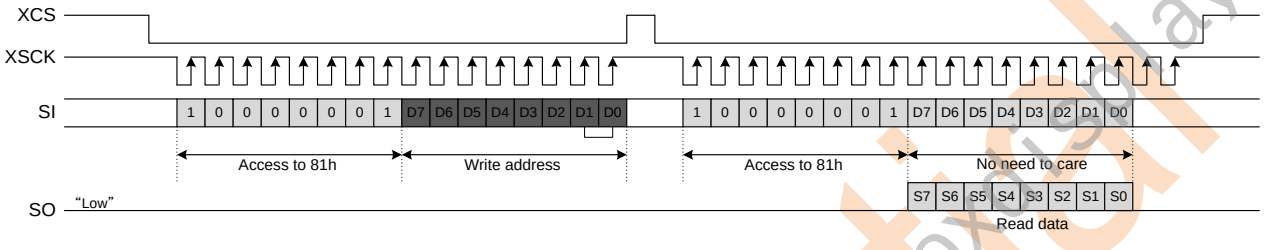
1. Set the RD_REGEN register(0x02h DATA2) to1
2. Set the RD_ON register (0x80h DATA0) to 1.
3. Write the address of reading data to 0x81h.
4. Read the data from SO (pin #46).

Switching of the serial communication mode (MSB / LSB first) is performed by XSCAN_MODE (input pin#39).

The timing of each mode is shown below.



Read access normal transfer (XSCAN_MODE =High; LSB first)



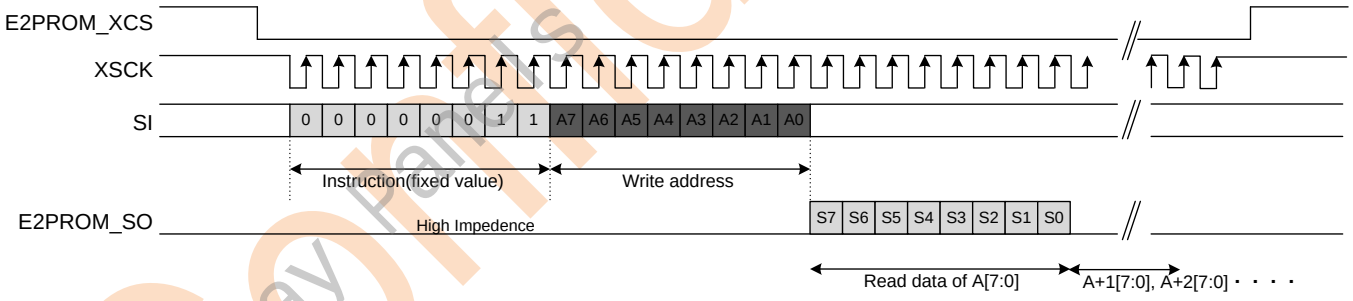
Read access normal transfer (XSCAN_MODE = Low; MSB first)

1.2. EEP ROM Read Timing

◆Read

Read operation should be designed to be able to support serial communication (normal transfer, MSB First).

The EEP ROM data should be read at the timing shown below.



1.3. Register Map

	Addr.	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
0	+0x00	VD_POL	HD_POL	VD_Filter	HD_Filter	DWN	RGT	MCLKPOL	PS0
1	+0x01	GAMSL[1:0]		DITHERON		FORMAT[3:0]			
2	+0x02			GCONEN	GBRTEN	TIM_REGEN	RD_REGEN		
3	+0x03					AMPBIAS[1:0]		TMPEN[1:0]	
4	+0x04	T_SLOPE	CALSEL[1:0]		CALDAC[4:0]				
5	+0x05	CONT[7:0]							
6	+0x06	CONT[8]	RCONT[6:0]						
7	+0x07		GCONT[6:0]						
8	+0x08		BCONT[6:0]						
9	+0x09	BRT[7:0]							
10	+0x0A		RBRT[6:0]						
11	+0x0B		GBRT[6:0]						
12	+0x0C		BBRT[6:0]						
13	+0x0D	H_ACT_U[7:0]							
14	+0x0E			V_ACT_D[9:8]			H_ACT_D[10:8]		
15	+0x0F	H_ACT_D[7:0]							
16	+0x10	V_ACT_U[7:0]							
17	+0x11	V_ACT_D[7:0]							
18	+0x12	S_BLK[7:0]							
19	+0x13						H_TOTAL[10:8]		
20	+0x14	H_TOTAL[7:0]							
21	+0x15		DE_D[10:8]				DE_U[10:8]		
22	+0x16	DE_U[7:0]							
23	+0x17	DE_D[7:0]							
24	+0x18			DSST_D[9:8]		DSST_U[9:8]		V_TOTAL[9:8]	
25	+0x19	V_TOTAL[7:0]							
26	+0x1A	DSST_U[7:0]							
27	+0x1B	DSST_D[7:0]							
28	+0x1C								
29	+0x1D								
30	+0x1E	WSEN1_U[7:0]							
31	+0x1F	WSEN1_W[7:0]							
32	+0x20					WSEN2_T[3:0]			
33	+0x21	DSEN_U[7:0]							
34	+0x22	VCK_U[3:0]				DSEN_W[3:0]			
35	+0x23	VCK_D[7:0]							
36	+0x24		SIGSELOFS_W[10:8]				SEL_OFS_W[10:8]		
37	+0x25					SIGSELOFS_U[3:0]			
38	+0x26	SIGSELOFS_W[7:0]							
39	+0x27			SELOFS_U[5:0]					
40	+0x28	SELOFS_W[7:0]							
41	+0x29		SIGSEL_W[10:8]				SEL_W[10:8]		
42	+0x2A	SIGSEL_W[7:0]							
43	+0x2B			SEL_U[5:0]					
44	+0x2C	SEL_W[7:0]							
...	...								
128	+0x80								RD_ON
129	+0x81	RD_ADDR[7:0]							

1.4. Description of Register

Register name	Bit width	V sync	Function
PS0	1		Power saving mode 0: Power saving on 1: Power saving off
MCLKPOL	1		MCLK polarity switching 0: Negative polarity 1: Positive polarity
RGT	1	Yes	0: Left scan 1: Right scan
DWN	1	Yes	0: Upper scan 1: Lower scan
HD_Filter	1		0: 1 MCLK 1: 3 MCLK
VD_Filter	1		0: 1 MCLK 1: 3 MCLK
HD_POL	1		0: Negative polarity 1: Positive polarity
VD_POL	1		0: Negative polarity 1: Positive polarity
FORMAT	4		Signal format selection 0000: XGA 59.94Hz (54 MHz) 1010: XGA 50Hz (54 MHz)
DITHERON	1	Yes	Dithering On/Off 0: Dithering Off 1: Dithering On
GAMSL	2		Gamma table selection 00: Internal gamma ($\gamma \fallingdotseq 3.5$, CALDAC 37.5mV/step) 01: Internal gamma ($\gamma \fallingdotseq 3.5$, CALDAC 62.5mV/step) 11: Internal gamma ($\gamma \fallingdotseq 2.4$, CALDAC 62.5mV/step) 11: Not used
GBRTEN	1		G Sub-Bright setting 0: Invalid 1: Valid
GCONEN	1		G Sub-Contrast setting 0: Invalid 1: Valid
TIM_REGEN	1		Timing setting 0: Invalid 1: Valid
RD_REGEN	1		Register read setting 0: Invalid 1: Valid
TMPEN	2		Temperature compensation On/Off 00: On(fixed) 01: On(same as 00) 10/11: Off
AMPBIAS	2		AMP Bias current selection 00: 100 % (fixed)
CALDAC	5		Luminance Adjustment Default: 01000
CALSEL	2		Vcal output selection 00: Not used 01: V1 output 10: V2 output 11: VOUT attenuate output (VGAM4 x 0.25[V])
T_SLOPE	1		Temperature gain selection 0: -6.3 mV/℃ (fixed)
CONT	9	Yes	Contrast adjustment

Register name	Bit width	V sync	Function
RCONT	7	Yes	R sub-contrast adjustment
GCONT	7	Yes	G sub-contrast adjustment
BCONT	7	Yes	B sub-contrast adjustment
BRT	8	Yes	Brightness adjustment
RBRT	7	Yes	R sub-brightness adjustment
GBRT	7	Yes	G sub-brightness adjustment
BBRT	7	Yes	B sub-brightness adjustment
H_ACT_U	8		Input signal rise position (horizontal)
H_ACT_D	11		Input signal fall position (horizontal)
V_ACT_U	8		Input signal rise position (vertical)
V_ACT_D	10		Input signal fall position (vertical)
S_BLK	8		Input signal exchange level
H_TOTAL	11		Horizontal total
DE_U	11	Yes	Display start position (horizontal)
DE_D	11	Yes	Display end position (horizontal)
V_TOTAL	10		Vertical total
DSST_U	10	Yes	Display start position (vertical)
DSST_D	10		Display end position (vertical)
WSEN1_U	8		Timing setting register
WSEN1_W	8		Timing setting register
WSEN2_T	4		Timing setting register
DSEN_U	8		Timing setting register
DSEN_W	4		Timing setting register
VCK_U	4		Timing setting register
VCK_D	8		Timing setting register
SIGSELOFS_U	4		Timing setting register
SIGSELOFS_W	11		Timing setting register
SELOFS_U	6		Timing setting register
SELOFS_W	11		Timing setting register
SIGSEL_W	11		Timing setting register
SEL_U	6		Timing setting register
SEL_W	11		Timing setting register
RD_ON	1		Register read on/off 0: Off 1: On
RD_ADDR	8		Register address for reading

2. Input supported Format

Panel driving timing should be set according to the input signal format.

To validate automatic timing setting, set the TIM_REGEN resistor to 0: invalid and select the signal format by the FORMAT resistor.

In case of the format which is not supported in the FORMAT, set the TIM_REGEN 1: valid and set each panel timing manually.

◆Register description

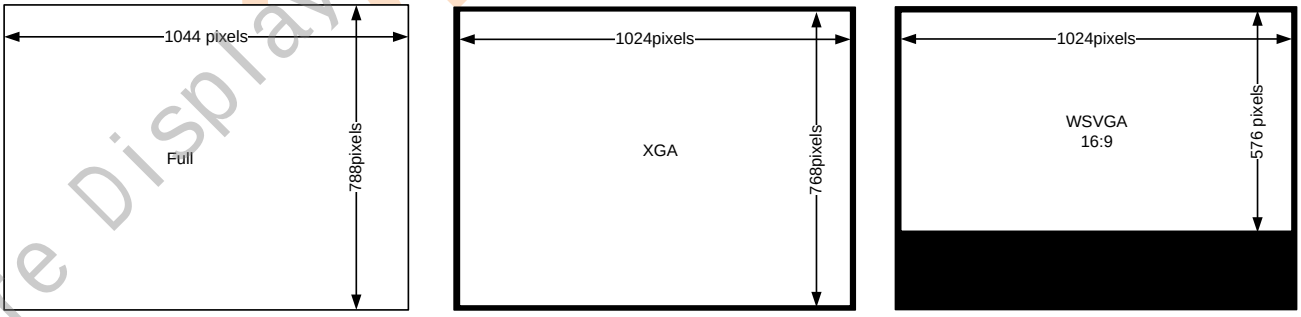
Address	Register	Number of bits	Setting Value
0x02	TIM_REGEN	1	Timing setting 0: Invalid 1: Valid
0x01	FORMAT[3:0]	4	Signal format selection 0000: XGA-59.94Hz (54MHz) 1010: XGA-50Hz (54MHz)

Input signal format	FORMAT [3:0]	Active		Total		FP		SYNC		BP		BP+Sync		fv	Th	Clock
		Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical	Horizontal	Time (µs)	Hz	µs	MHz
XGA-59.94Hz	0000	1024	768	1092	825	20	19	16	6	32	32	48	0.89	59.94	20.2	54
WSVGA-59.94Hz	-	1024	576	1092	825	20	211	16	6	32	32	48	0.89	59.94	20.2	54
XGA-50Hz	1010	1024	768	1200	900	128	94	16	6	32	32	48	0.89	50	22.2	54
WSVGA-50Hz	-	1024	576	1200	900	128	286	16	6	32	32	48	0.89	50	22.2	54

3. Display Area

The display area is 1044 ×784 pixels including all the orbit margin of 10 pixels on the right, left, upper and lower side from XGA active area.

The black frame should be displayed by masking the blanking period of XGA / WSVGA (16:9) signal.



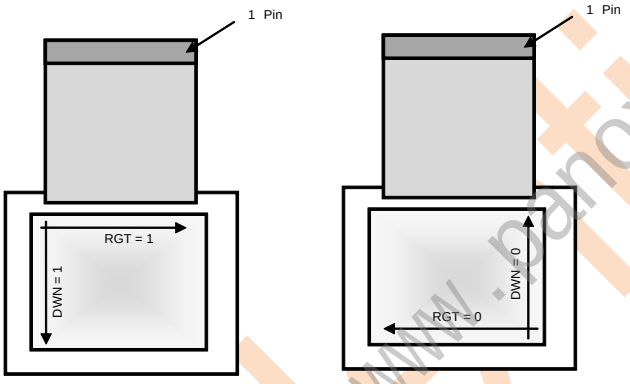
4. Up/down and/or right/left inverse display

The RGT register determines the direction of horizontal scan while the DWN register determines the direction of vertical scan.

Each setting mode is shown below.

◆Register description

Address	Register	Number of bits	Setting Value
0x00	RGT	1	0: Left scan 1: Right scan
0x00	DWN	1	0: Up scan 1: Down scan



5. Internal gamma function

Panel has internal gamma table. Gamma mode is selected by the GAMSEL resistor.

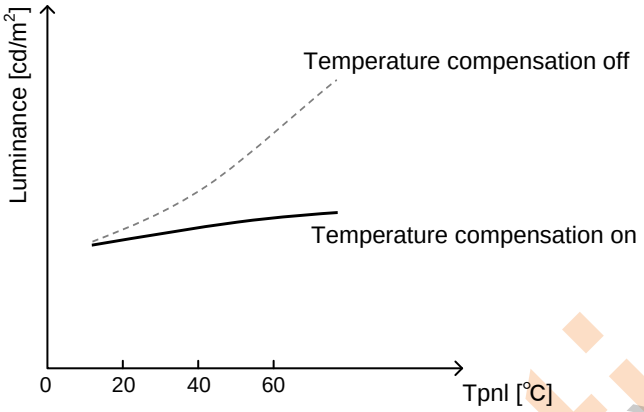
◆Register description

Address	Register	Number of bits	Setting Value
0x01	GAMSL	2	Gamma table selection 00: Internal gamma (γ≒3.5, CALDAC 37.5mV/step) 01: Internal gamma (γ≒3.5, CALDAC 62.5mV/step) 11: Internal gamma (γ≒2.4, CALDAC 62.5mV/step) 11: Not used

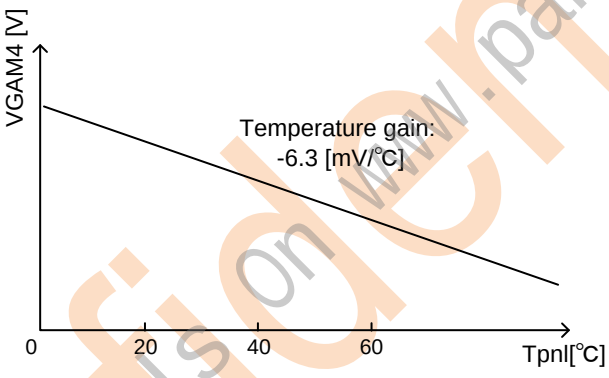
6. Luminance Adjustment Function (temperature compensation)

OLED panel has the characteristics of luminance dependence on temperature.

Luminance adjustment is performed by the temperature compensation function.



Temperature compensation is realized by sensing the temperature using internal sensor and calibrating the VGAM4 voltage according to temperature gain written below.



◆Register description

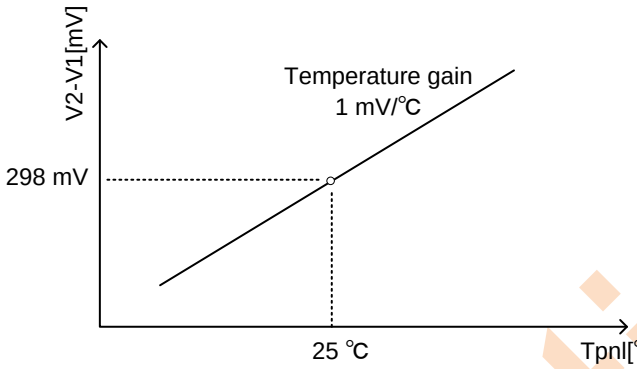
Address	Register	Number of bits	Setting Value
0x03	TEMPEN[1:0]	2	Temperature compensation On/Off Temperature compensation On/Off 00: On(fixed) 01: On(same as 00) 10/11: Off
0x04	T_SLOPE	1	Temperature gain selection 0: -6.3 mV/°C (fixed)
0x04	CALSEL	2	Vcal output selection 00: Not used 01: V1 output 10: V2 output 11: VOUT attenuate output (VGAM4 x 0.25[V])

◆Panel temperature sensing function

Panel has internal temperature sensor and its output voltage can be read by tne Vcal pin (pin #49).

By setting the CALSEL register to the value written above, the output voltage V1/V2 is selected.

Calculation of V2-V1 is converted into the panel temperature by temperature gain.



7. Luminance adjustment function

To adjust the panel luminance, set the VGAM4 voltage according to the CALDAC register value.

◆Register description

Address	Register	Number of bits	Setting Value
0x04	CALDAC[4:0]	5	Luminance adjustment(gamma top reference voltage variable) Default: 01000 37.5mV/step (when GAMSEL=00) 62.5mV/step (when GAMSEL=01/10)

◆CALDAC register setting value and adjustment voltage (GAMSEL=00)

CALDAC	Decimal	0	…	7	8(Default)	9		31
	Binary	00000	…	00111	01000	01001		
VGAM4 adjustment voltage [mV]		-300		-37.5	0	+37.5		+862.5

◆CALDAC register setting value and adjustment voltage (GAMSEL=01/10)

CALDAC	Decimal	0	…	7	8(Default)	9		31
	Binary	00000	…	00111	01000	01001		
VGAM4 adjustment voltage [mV]		-500		-62.5	0	+62.5		+1437.5

8. White balance adjustment function

8.1. Contrast / Sub Contrast

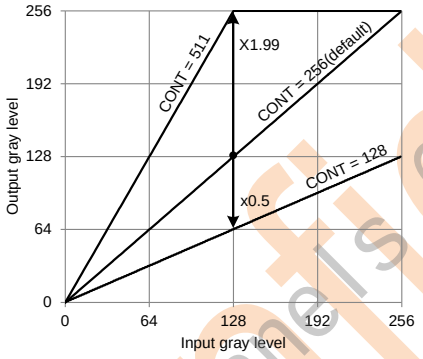
Register CONT determines all the RGB contrast (gain) to input signal, while RCONT/GCONT/BCONT determines R/G/B gain to output of CONT separately.

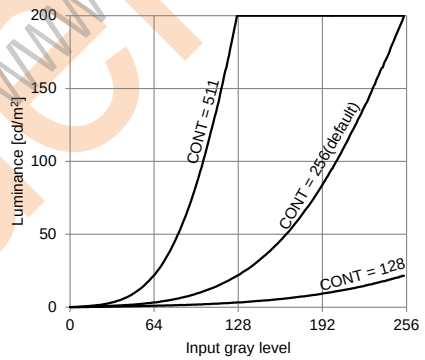
◆Register description

Address	Register	Number of bits	Function
0x02	GCONEN	1	G Sub-Contrast setting 0: Invalid 1: Valid
0x05,0x06	CONT	9	RGB gain to input signal: x0 ⋯ x1 (default) ⋯ x1.99
0x06	RCONT	7	R gain to CONT: x0.75 ⋯ x1.0 (default) ⋯ x1.24
0x07	GCONT	7	G gain to CONT: x0.75 ⋯ x1.0 (default) ⋯ x1.24
0x08	BCONT	7	B gain to CONT: x0.75 ⋯ x1.0 (default) ⋯ x1.24

◆Contrast adjustment

CONT	0	…	128	…	256(Default)	…	384	…	511
RGB gain to input	×0	…	×0.5	…	×1	…	×1.5	…	×1.99

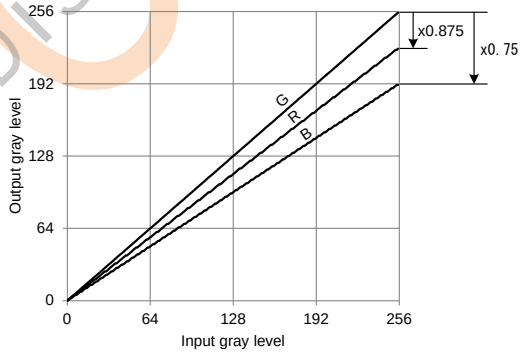




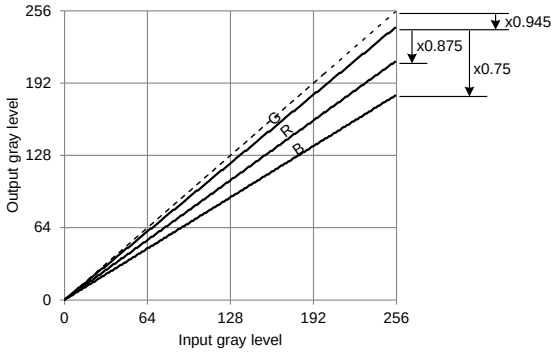
◆Sub contrast adjustment

R/G/BCONT	0	…	32	…	64(Default)	…	96	…	127
R/G/B gain to CONT	×0.75	…	×0.875	…	×1	…	×1.125	…	×1.24

Example 1
CONT = 256 (x1)
RCONT = 32 (x0.875)
GCONT = 64 (x1)
BCONT = 0 (x0.75)



Example 2
CONT = 242 (x0.945)
RCONT = 32 (x0.875)
GCONT = 64 (x1)
BCONT = 0 (x0.75)



8.2. Bright / Sub Bright

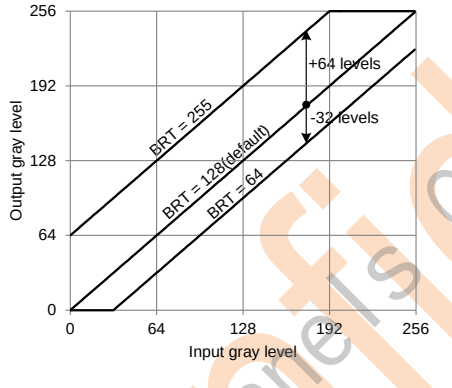
Register BRT determines all the RGB brightness (bias) to input signal, while RBRT/GBRT/BBRT determines R/G/B bias to output of BRT separately.

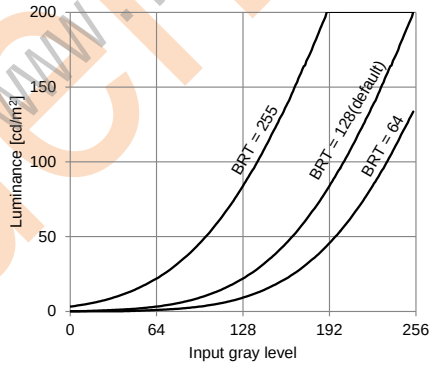
◆Register description

Address	Register	Number of bits	Function
0x02	GBRTEN	1	G Sub-Bright setting 0: Invalid 1: Valid
0x09	BRT	8	RGB bias to input signal: -64 ⋯ 0 (default) ⋯ +63 levels
0x0A	RBRT	7	R bias to BRT: -32 ⋯ 0 (default) ⋯ +31 levels
0x0B	GBRT	7	G bias to BRT: -32 ⋯ 0 (default) ⋯ +31 levels
0x0C	BBRT	7	B bias to BRT: -32 ⋯ 0 (default) ⋯ +31 levels

◆Bright adjustment

BRT	0	…	64	…	128(Default)	…	192	…	255
Output gray level (to input)	-64	…	-32	…	0	…	+32	…	+63

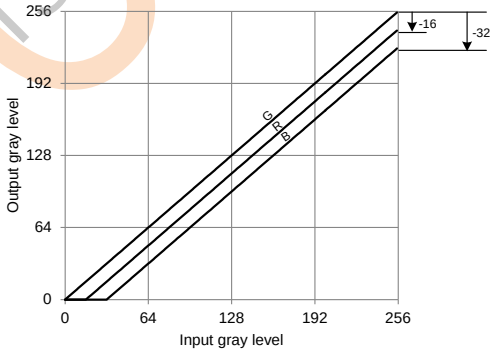




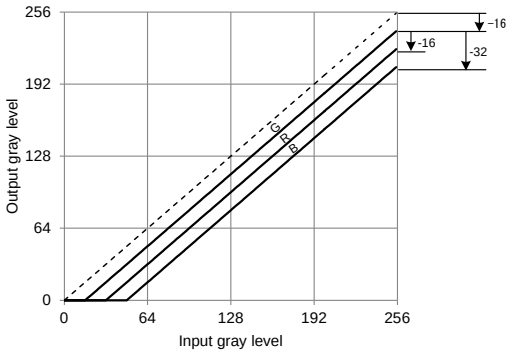
◆Sub bright adjustment

R/G/BBRT	0	…	32	…	64(Default)	…	96	…	127
Output gray level (to BRT)	-32	…	-16	…	0	…	+15	…	+31

Example 3
BRT = 128 (0)
RBRT = 32 (-16 levels)
GBRT = 64 (0)
BBRT = 0 (-32 levels)



Example 4
BRT = 96 (-16 levels)
RBRT = 32 (-16 levels)
GBRT = 64 (0)
BBRT = 0 (-32 levels)



9. Dithering Function

This function increases the number of gray scale levels simulately making use of FRC, and performs the compensation for the dereased gray scay levels after white balance adjusutment (contrast / bright).

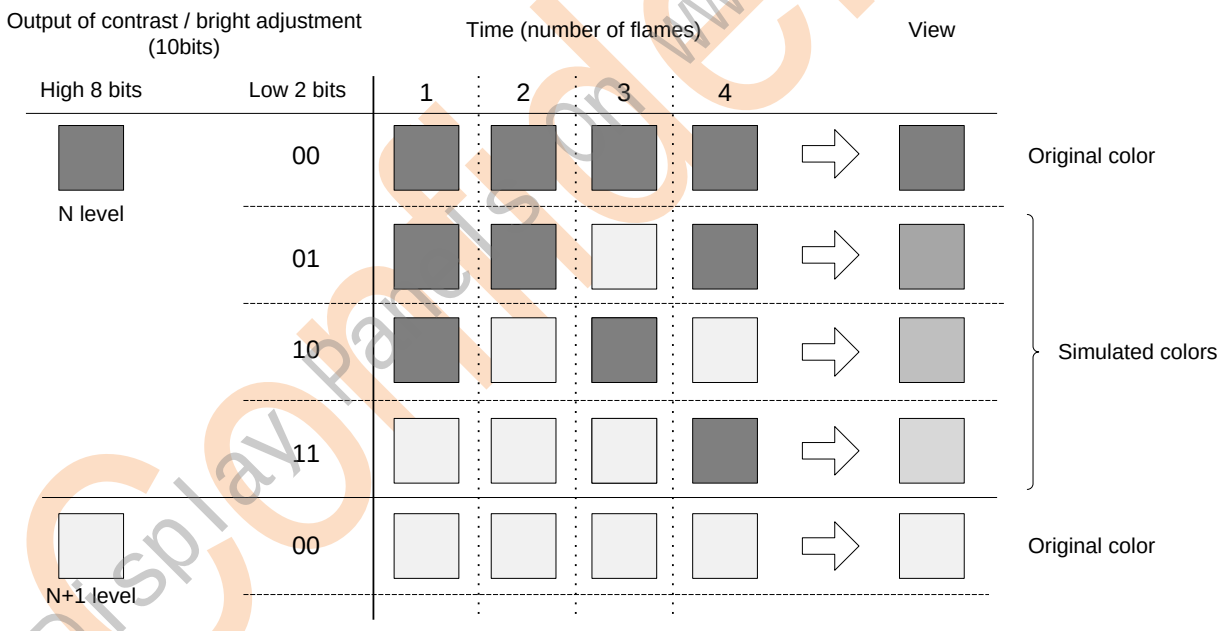
◆Register description

Address	Register	Number of bits	Setting Value
0x01	DITHERON	1	Dithering On/Off 0: Dithering Off 1: Dithering On

9.1. FRC (Frame Rate Control)

Simulated colors are expressed making use of frame rate and image lag effect of human eyes. When two colors are switching alternately in high-speed, it looks an intermediate color for human eyes. Three simulated colors can be added to original colors by changing data in 4-frame cycle making use of this property (2 bit FRC).

FRC simulated color image when noticing arbitral one pixel is shown below.



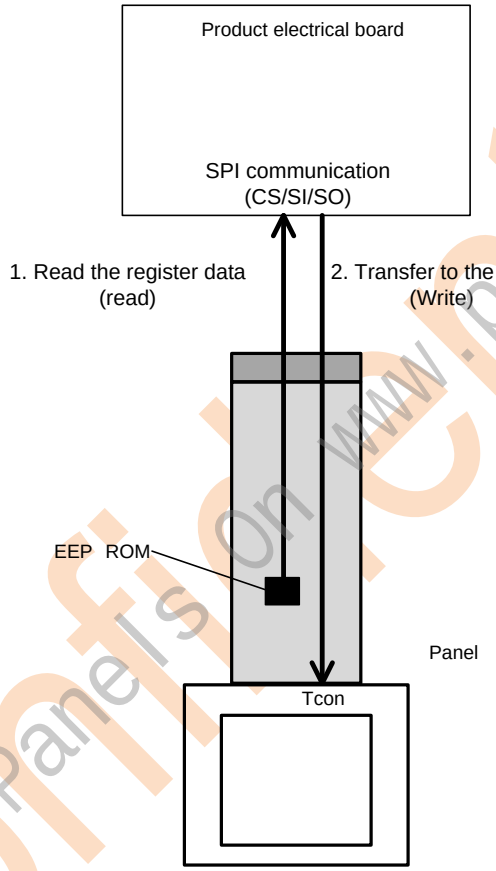
10. Luminance and white balance adjustment

Luminance and white balance adjustment is done by 7.Luminance Adjustment Function and 8.White Balance Adjustment Function. Alternate method of luminance and white balance adjustment is to make use of the recommended register settings stored in the EEP ROM.

10.1 Procedure for reading register setting and transfer to the panel.

1. Read the register data stored in the EEP ROM according to the sequence written in Description of Function 1.2 EEP ROM read timing (read).

2. Transfer the register data to the panel (write).

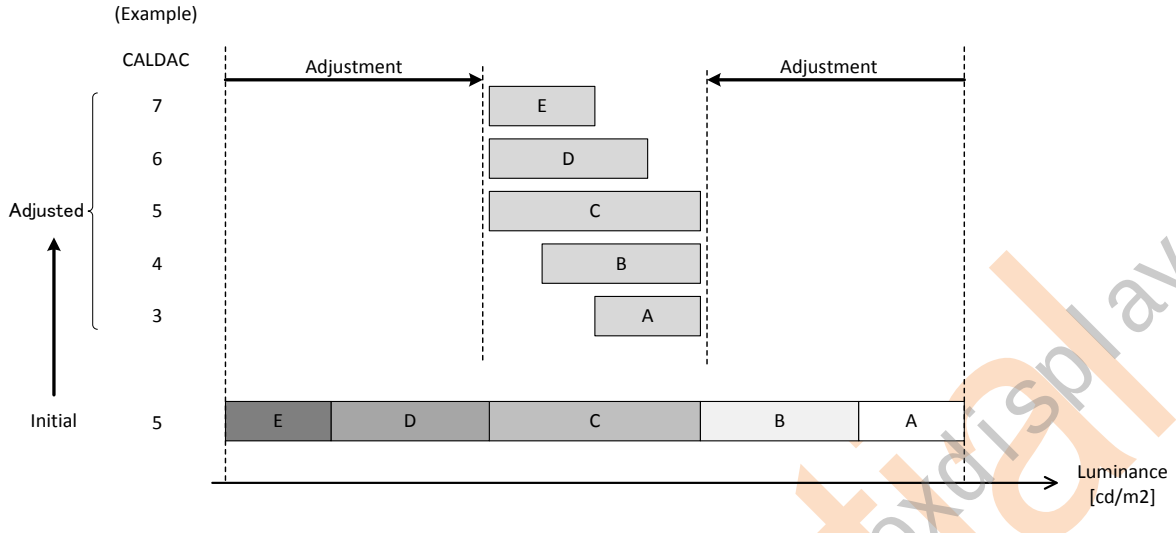


10.2 Register Map of EEP ROM

	Addr.	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
Mode 0	+0x00	GAMSEL[1:0]			CALDAC[4:0]				
	+0x01	CONT[7:0]							
	+0x02	CONT[8]	RCONT[6:0]						
	+0x03		GCONT[6:0]						
	+0x04		BCONT[6:0]						
	+0x05	BRT[7:0]							
	+0x06		RBRT[7:0]						
	+0x07		GBRT[7:0]						
	+0x08		BBRT[7:0]						
	+0x09					Ver.[3:0]			
		~							
Mode 2	+0x20	GAMSEL[1:0]			CALDAC[4:0]				
	+0x21	CONT[7:0]							
	+0x22	CONT[8]	RCONT[6:0]						
	+0x23		GCONT[6:0]						
	+0x24		BCONT[6:0]						
	+0x25	BRT[7:0]							
	+0x26		RBRT[7:0]						
	+0x27		GBRT[7:0]						
	+0x28		BBRT[7:0]						
	+0x29					Ver.[3:0]			
Mode 3	+0x30	GAMSEL[1:0]			CALDAC[4:0]				
	+0x31	CONT[7:0]							
	+0x32	CONT[8]	RCONT[6:0]						
	+0x33		GCONT[6:0]						
	+0x34		BCONT[6:0]						
	+0x35	BRT[7:0]							
	+0x36		RBRT[7:0]						
	+0x37		GBRT[7:0]						
	+0x38		BBRT[7:0]						
	+0x39					Ver.[3:0]			
Mode 4	+0x40	GAMSEL[1:0]			CALDAC[4:0]				
	+0x41	CONT[7:0]							
	+0x42	CONT[8]	RCONT[6:0]						
	+0x43		GCONT[6:0]						
	+0x44		BCONT[6:0]						
	+0x45	BRT[7:0]							
	+0x46		RBRT[7:0]						
	+0x47		GBRT[7:0]						
	+0x48		BBRT[7:0]						
	+0x49					Ver.[3:0]			

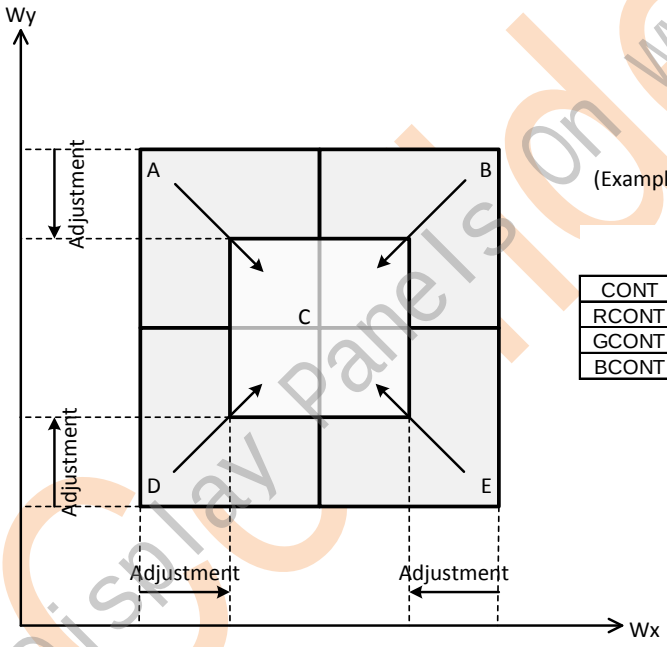
10.3 Luminance Adjustment

Luminance adjustment is done by CALDAC register.



10.4 White Balance Adjustment

White balance adjustment is done by CONT, RCONT, GCONT and BCONT registers.

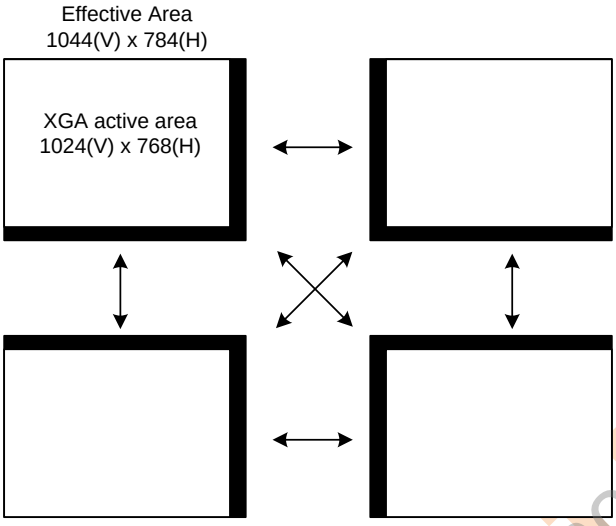


(Example)

	Standard				
	A	B	C	D	E
CONT	242	242	242	242	242
RCONT			64		
GCONT			64		
BCONT			64		

11. Orbit function

This function changes the display start position and alleviates the image sticking view due to locally concentrated luminance.



◆Register description

Address	Register	Number of bits	Function
0x15 0x16	DE_U	11	Display start position (horizontal)
0x18 0x1A	DSST_U	10	Display start position (vertical)
0x18 0x1B	DSST_D	10	Display end position (vertical)

11.1. The horizontal display position shift

The display start position is determined by register DE_U.
The variable range is ± 10 pixels.

◆Register setting

When RGT = 1 (right and left inversed when RGT = 0) in decimal notation

XGA-59.94Hz	DE-U	41	…	32	31(Default)	30	…	21
	Pixel shift	Left 10	…	Left 1	Center	Right 1	…	Right 10

XGA-50Hz	DE-U	41	…	32	31(Default)	30	…	21
	Pixel shift	Left 10	…	Left 1	Center	Right 1	…	Right 10

*Notes on rightward shift

Setting DE_U = 0 is prohibited.
When DE_U＜0, set the value of HTOTAL-1, HTOTAL-2, HTOTAL-3 and so on.

11.2. Vertical display position shift

The display start / end position is determined by register DSST_U / DSST_D.
The variable range is ± 10 pixels.

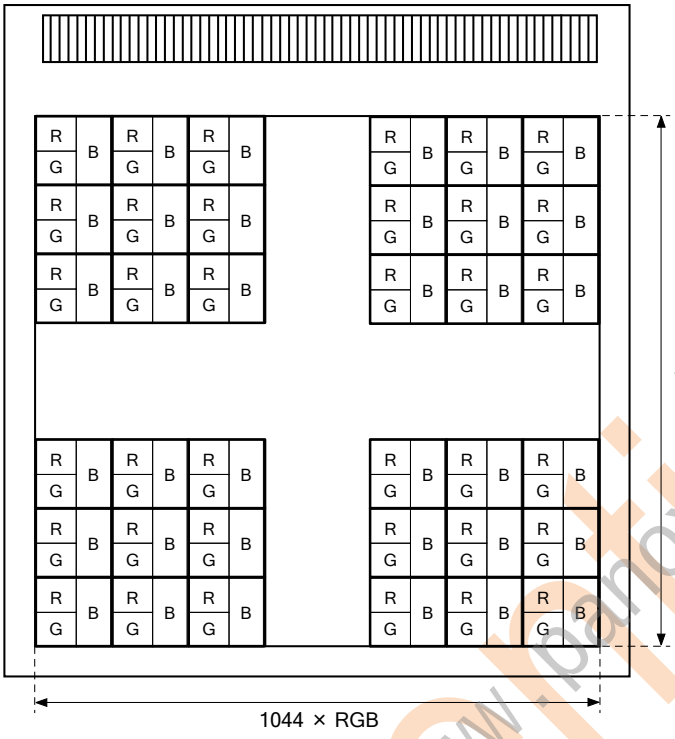
◆Register setting

When DWN = 1 (up and down inversed when DWN = 0) in decimal notation

XGA-59.94Hz	DSST_U	39	…	30	29(Default)	28	…	19
	DSST_D	781	…	772	771(Default)	770	…	761
	Pixel shift	Upward 10	…	Upward 1	Center	Downward 1	…	Downward 10

XGA-50Hz	DSST_U	39	…	30	29(Default)	28	…	19
	DSST_D	849	…	840	839(Default)	838	…	829
	Pixel shift	Upward 10	…	Upward 1	Center	Downward 1	…	Downward 10

Pixel Alignment



Optical Characteristics

1. Optical Characteristics

Item		Symbol	System	Min.	Typ.	Max.	Unit
Luminance	Mode 2	L2	1	102	120	138	Cd/m^2
	Mode 0	L0	1	170	200	230	Cd/m^2
	Mode 3	L3	1	255	300	345	Cd/m^2
	Mode 4	L4	1	400	500	600	Cd/m^2
Contrast		CR	1	5,000	—	—	
Chromaticity	W (Mode 0,2&3)	x	1	0.298	0.310	0.322	CIE
		y	1	0.298	0.310	0.322	CIE
	W (Mode 4)	x	1	0.295	0.310	0.325	CIE
		y	1	0.295	0.310	0.325	CIE
	R	x	1	0.635	0.655	0.675	CIE
		y	1	0.310	0.330	0.350	CIE
	G	x	1	0.255	0.275	0.295	CIE
		y	1	0.625	0.645	0.665	CIE
	B	x	1	0.127	0.147	0.167	CIE
		y	1	0.045	0.065	0.085	CIE

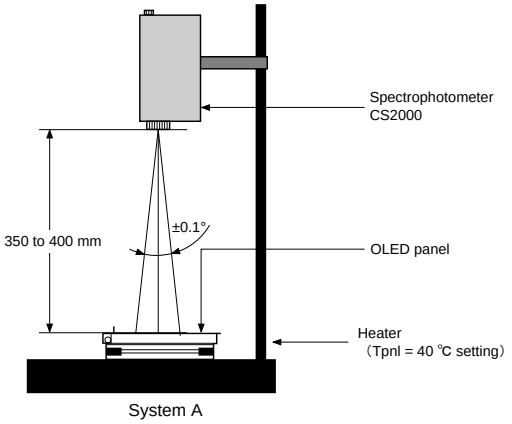
Drive conditions : EEP-ROM register setting
Measurement temperature : Tpnl = 40 ˚C
Measurement point : One point on the screen center

2. Measurement method and system 1

All white display : All RGB signal data is set to High.
All black display : All RGB signal data is set to Low.

◆Luminance, color temperature and Chromaticity:
Measured in Measurement System A.

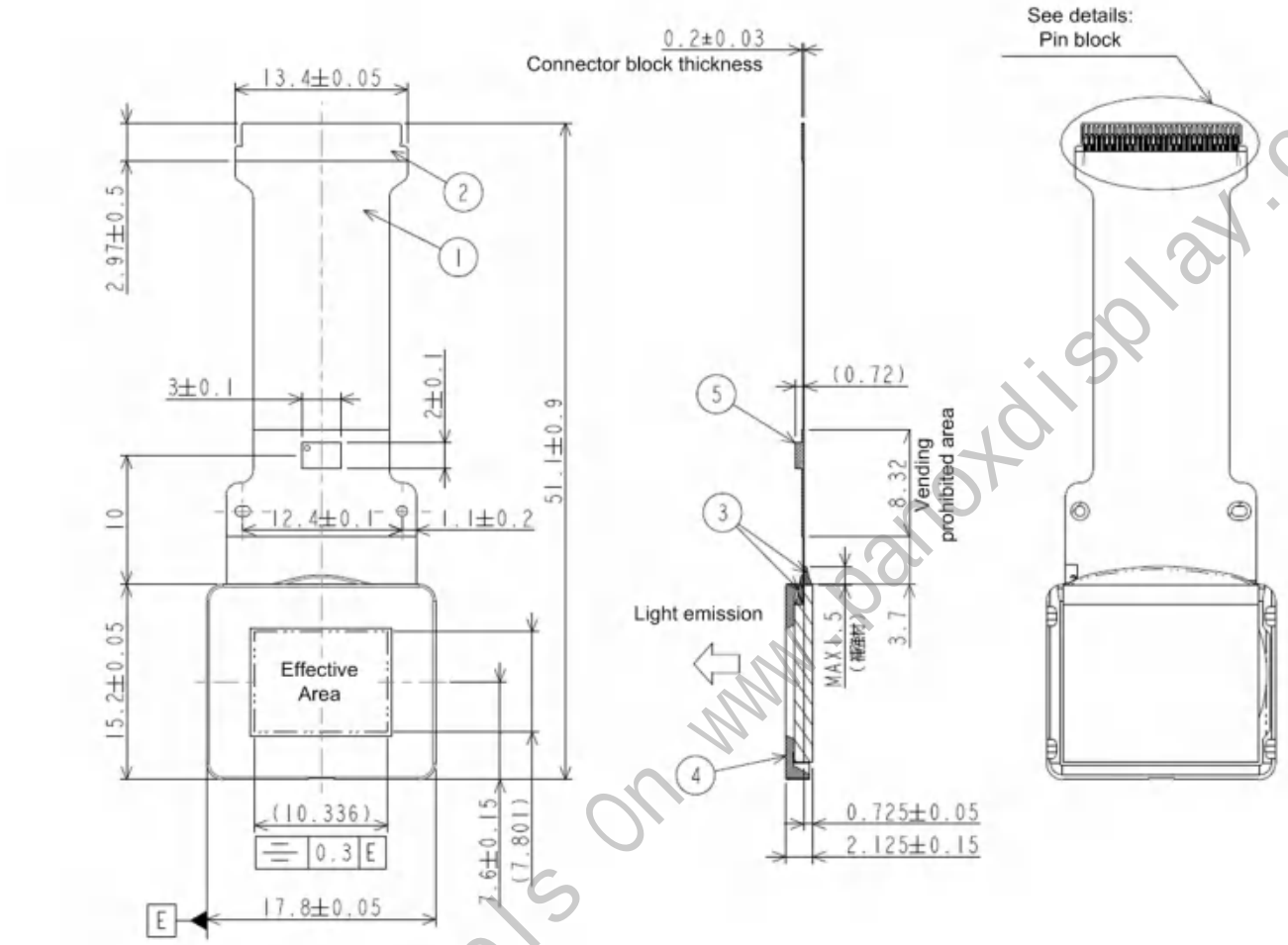
◆Contrast:
Measure the luminance of the panel in Measurement System A and substitute them in the formula below.
Contrast = Luminance in all white display / Luminance in all black display

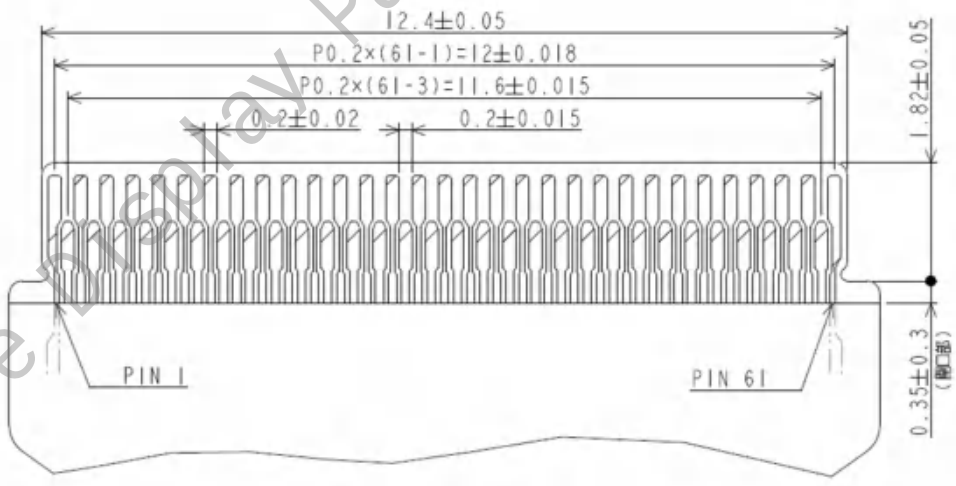


System A

Package Outline

(Unit : mm)





Details of pin block

No	Items
1	FPC
2	Reinforcing Plate
3	Stiffener
4	Frame
5	ROM

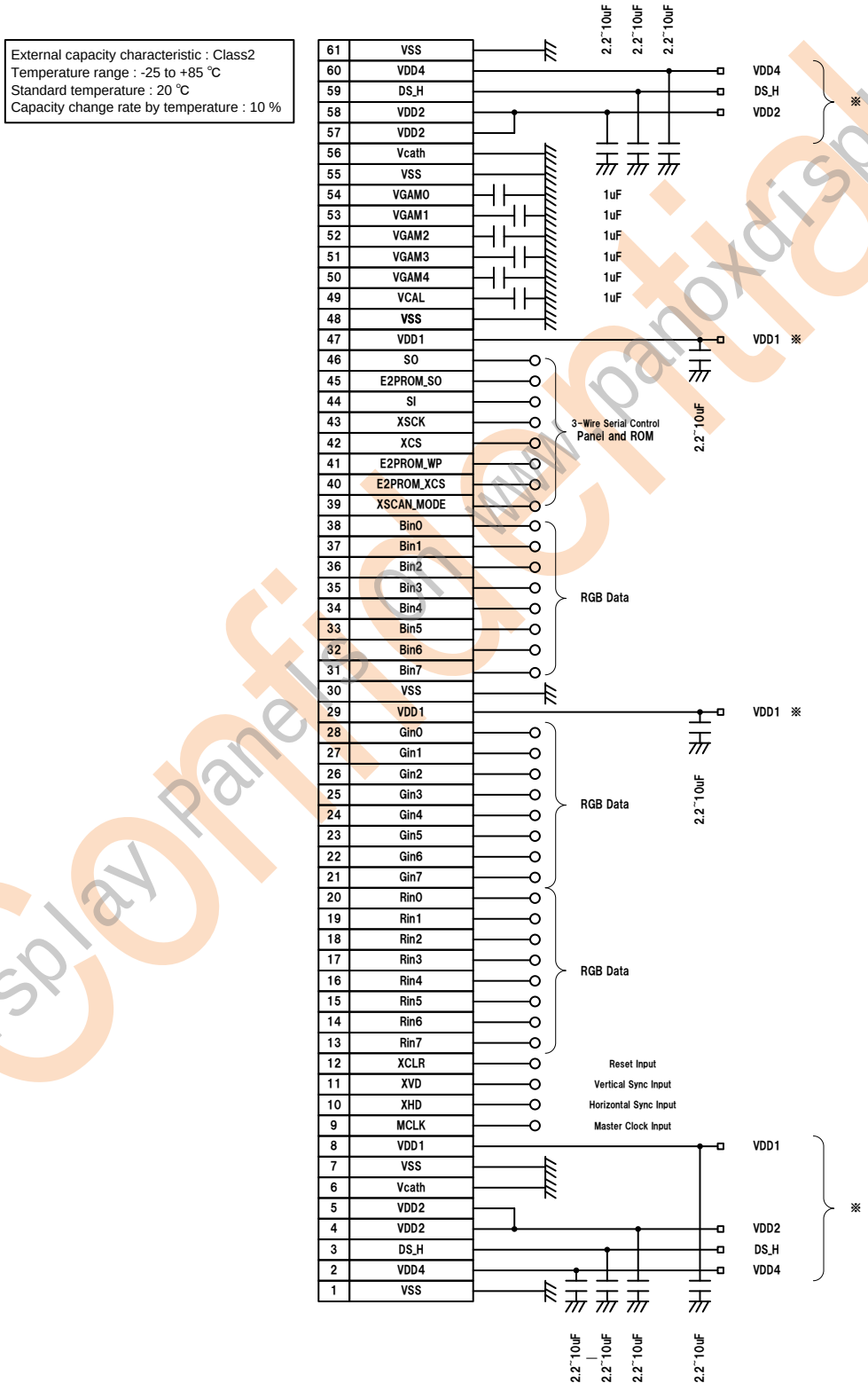
Weight: 1.0g

Recommendation

1. Peripheral circuits

Reccommended periheral circuits of panel pin is as follows.

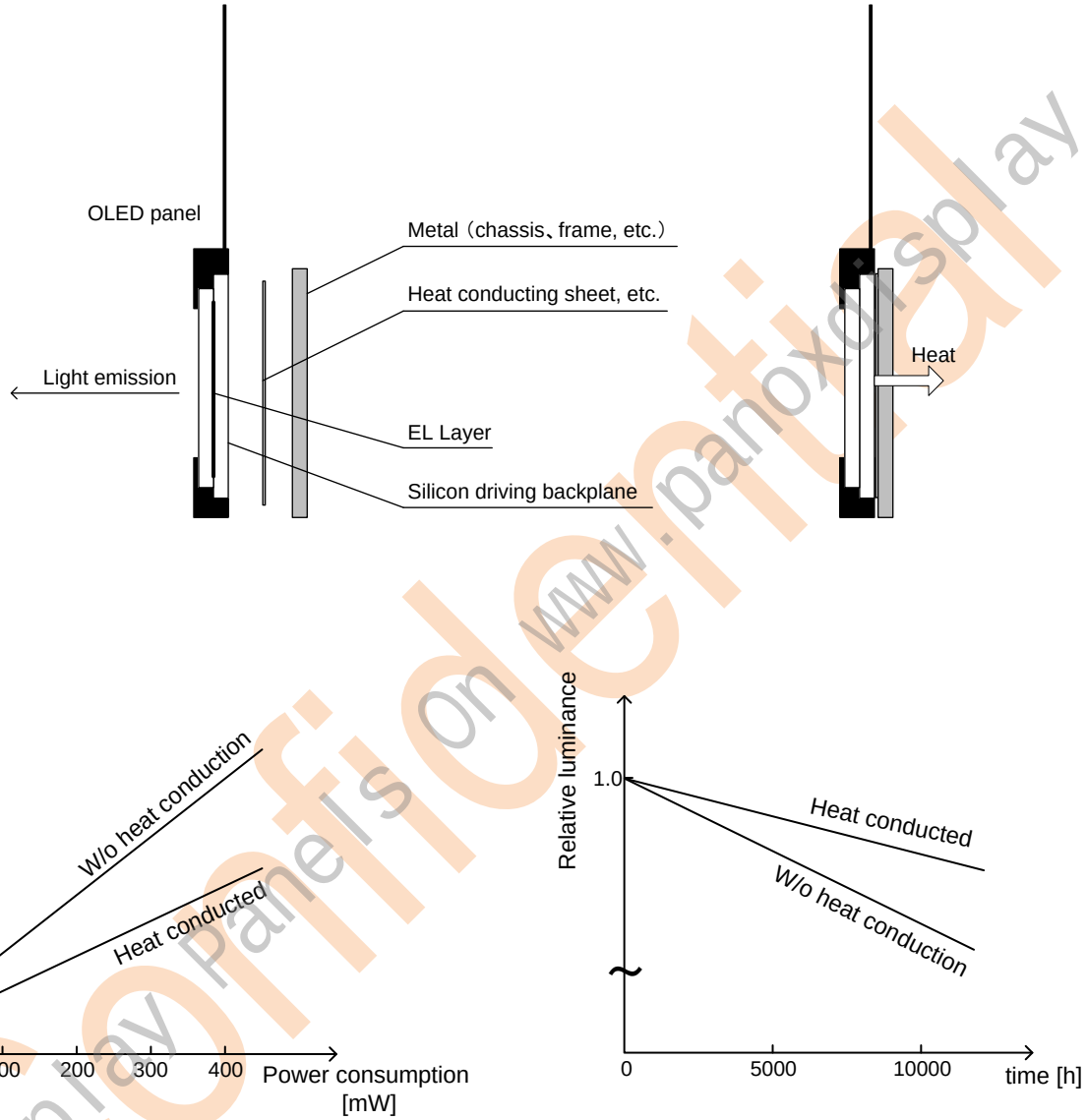
*2.2μF to 10μF capacitor needs to be mounted for each power supply (※). Short capacitance may affect the picture quality.



2. Panel Temperature Control by Heat Condcution

The tempareture of OLED panel rises dut to power consumption of EL layer and silicon driving backplane. Higher panel temperature may affects the luminance degradation in the long span.

To control the panel temperature , heat conduction between panel back side(silicon bakplane) and metal (chassis, frame,etc.) is recommended.



Notes on Handling

1. Static charge prevention

   Be sure to take the following protective measures. OLED panels (modules) are easily damaged by static charges.

   (1) Use non-chargeable gloves, use bare hands.
   (2) Use a wrist strap when handling.
   (3) Do not touch any electrodes of the panel.
   (4) Wear non-chargeable clothes and conductive shoes.
   (5) Install grounded conductive mats on the working floor and working table.
   (6) Keep the panel (module) away from any charged materials.

2. Protection from dust and dirt

   (1) Operate in a clean environment.
   (2) Do not touch the panel (module) surface. The surface is easily scratched.
   When cleaning, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
   (3) Apply ionized air blow or air blow to the panel when dust and dirt fall on the panel surface.

3. Others

   (1) Do not hold the flexible board or twist or bend it because the flexible board connection block is easily affected by twist.
   (2) The minimum fold radius of the flexible board is 1 mm.
   (3) Do not drop the panel.
   (4) Do not twist or bend the panel.
   (5) Keep the panel away from heat sources.
   (6) Do not dampen the panel with water or other solvents.
   (7) Do not store or use of the panel at high temperatures or high humidity, as this may affect the characteristics.
   (8) When disposing this panel, handle it as an industrial waste complying with related regulations.
   (9) Do not store or use the panel in reactive chemical substances (including alcohol) environment, as this may affect the performance.
   (10) This panel is delivered with packed in the degassed aluminum laminated bag.
   When storing this panel after unsealing bags, put it into the aluminum laminated bag again and seal it with tapes with the opening folded after entering desiccants.