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CUSTOMER APPROVAL SHEET

Company Name

MODEL H163QLN01.1

CUSTOMER **Title :**

APPROVED **Name :**

☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)**

☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)**

☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.____)**

☐ **CUSTOMER REMARK :**

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Product Specification

1.63" COLOR AMOLED MODULE

MODEL NAME: H163QLN01

AUO Product P/N: 95.01H72.101

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	Mar. 5, 2014		First Draft
1.0	Mar.18,2014	17 21 22 23	Revise H. Specifications_Optical characteristics Add I. Reliability test items_Vibration test Add J.packing Revise K.2D/3D drawing;
2.0	Apr.16,2014	7 11 14, 15 16 24	Add Idle power consumption & revise panel power Revise TE description Revise Initial Code for display optimization B500=0x05 -> 0x03; B501=0x05 -> 0x03; B502=0x05 -> 0x03 BA00=0x13 -> 0x03; BA01=0x13 -> 0x03; BA02=0x13 -> 0x03 BE00=0x22 -> 0x32 Revise CF description Revise K. 2D drawing
3.0	July.3,2014	24	Revise K. 2D drawing
4.0	July.17,2014	24	Revie 2D drawing for foam tape modified.
5.0	Aug.7,2014	25	Add Precaution
6.0	Oct. 6,2014	 13 14 15 24	Revise Initial Code for display optimization BD00~BD04 =0x03 20 14 4B 00 BE00~BE04 =0x03 20 14 4B 01 BF00~BF04 =0x03 20 14 4B 00 EB00=0x02 E900~E902 = 0x00 36 38 B600=0x53 -> 0x55; B601=0x53 -> 0x55; B602=0x53 -> 0x55 B700=0x33 -> 0x36; B701=0x33 -> 0x36; B702=0x33 -> 0x36 CF03=0xEF -> 0XE8 Revie 2D drawing for foam tape modified.

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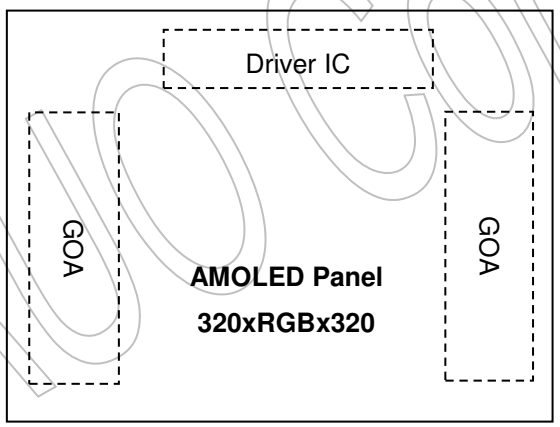
A. General Specification

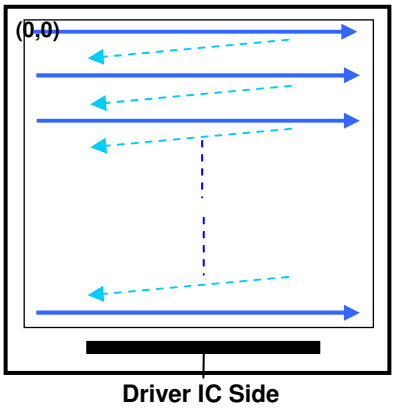
1. Physical Specifications

	Item	Description	Remark
1	Screen Size (inch)	1.63”	
2	Display Mode	AMOLED	
3	Display Resolution (dot)	320xRGBx320	
4	Active Area (mm*mm)	29.28 (H)×29.28(V)	
5	Pixel Configuration	Hyper R.G.B	
6	Display Color (M)	16.7	
7	Brightness (nits)	300	
8	Interface	MIPI DSI	
9	Outline Dimension (mm*mm*mm)	32.08 (H) × 36.48(V) × 0.7(T)	cell+foam

2. Module Block Diagram



3. Panel Scan direction



B. Electrical Specifications

1. Main FPC Pin assignment — AMOLED Panel Input/Output Signal Interface

Recommended connector: AXE520127 (Panasonic)

FPC	Pin_name	I/O	Description
1	**ELVSS**	P	AMOLED power Negative
2	**ELVSS**	P	AMOLED power Negative
3	**ELVSS**	P	AMOLED power Negative
4	**VDD**	P	Power supply for analog
5	**IOVDD**	P	Power supply for Interface system excep MIPI interface
6	**GND**	P	GND
7	**TE**	O	Vsync(vertical sync)signal output from panel to avoid tearing effect
8	**MTP**	I	MTP(need to indicate to connect GND or NC)
9	**RESX**	I	Device reset signal (0 : Enable ; 1: Disable)
10	**SWIRE**	O	SWIRE signal for PWR IC control
11	**ELVDD**	P	AMOLED power positive
12	**ELVDD**	P	AMOLED power positive
13	**ELVDD**	P	AMOLED power positive
14	**GND**	P	GND
15	**DSI_D0N**	I/O	MIPI data negative signal
16	**DSI_D0P**	I/O	MIPI data positive signal
17	**GND**	P	GND
18	**DSI_CLKN**	I	MIPI strobe negative signal
19	**DSI_CLKP**	I	MIPI strobe postive signal
20	**GND**	P	GND

Note: I = input ; O = output ; P = Power ; I/O = input / Output

2. Absolute maximum ratings

Item	Symbol	Min.	Max.	Unit	Remark
Digital Power supply	IOVDD	-0.3	5.5	V	
Analog Power supply	VDD	-0.3	5.5	V	
ELVDD power supply	ELVDD	-	5.0	V	
ELVSS power supply	ELVSS	-5.0	-	V	

Note : If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

C. Electrical Characteristics

1. DC Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Digital Power supply		IOVDD	1.65	1.8	1.95	V	Note1
Analog Power supply		VDD	2.8	3.0	3.1	V	Note1
ELVDD power supply		ELVDD	4.57	4.60	4.63	V	Note1,2
ELVSS power supply		ELVSS	-3.35	-3.40	-3.45	V	Note1
Input Signal Voltage	H Level	V_{IH}	0.8*IOVDD	-	IOVDD	V	Note1
	L Level	V_{IL}	0	-	0.2*IOVDD	V	
Output Signal Voltage	H Level	V_{OH}	0.8*IOVDD	-	IOVDD	V	Note1
	L Level	V_{OL}	0	-	0.2*IOVDD	V	Note1

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

Note 2 : TPS65631W Positive output voltage = 4.6V ± 0.8% at -40℃ ≦ Ta ≦ +85 ℃

2. Display Current Consumption

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Panel Power		P_{NL}	ELVDD:4.6V ELVSS:-3.4V	--	--	138.4	mW	Note1,2,
		I_{NL}		--	--	17.3	mA	Note1,2,
IC	**Normal**	P_{VDD}	VDD : 3.0V	--	25.2	39.3	mW	Note2,
		I_{VDD}		--	8.4	13.1	mA	Note2,
		P_{IOVDD}	IOVDD :1.8V	--	18.0	19.8	uW	Note2,
		I_{IOVDD}		--	10.0	11.0	uA	Note2,
	Idle	P_{VDD}	VDD : 3.0V	--	12.0	15.3	mW	Note3,
		I_{VDD}		--	4.0	5.1	mA	Note3,
		P_{IOVDD}	IOVDD :1.8V	--	18.0	19.8	uW	Note3,
		I_{IOVDD}		--	10.0	11.0	uA	Note3,

Note 1: Based on L255 (300nits) full white pattern

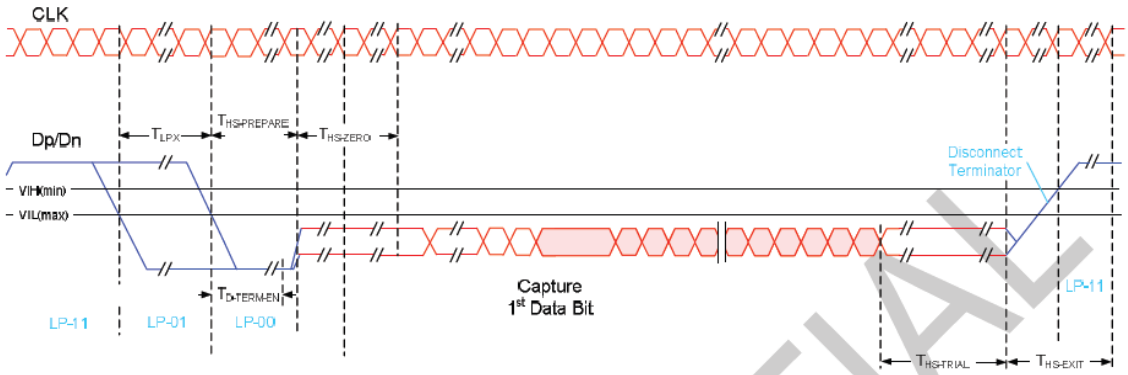
Note 2: Testing in MIPI-DSI frame rate 60Hz CMD mode.

Note 3: Testing in MIPI-DSI frame rate 30Hz CMD mode.

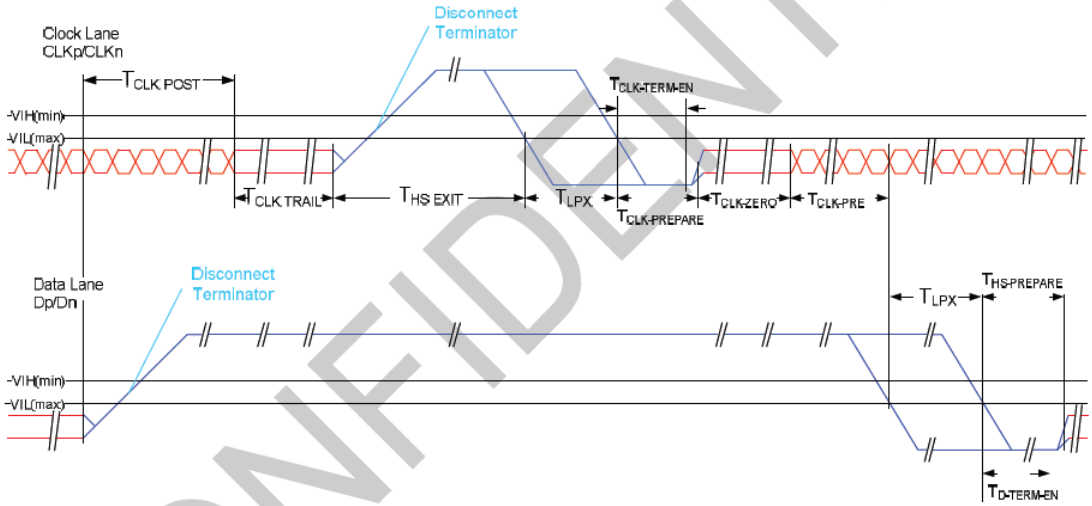
D. AC Characteristics

1. MIPI Interface Characteristics

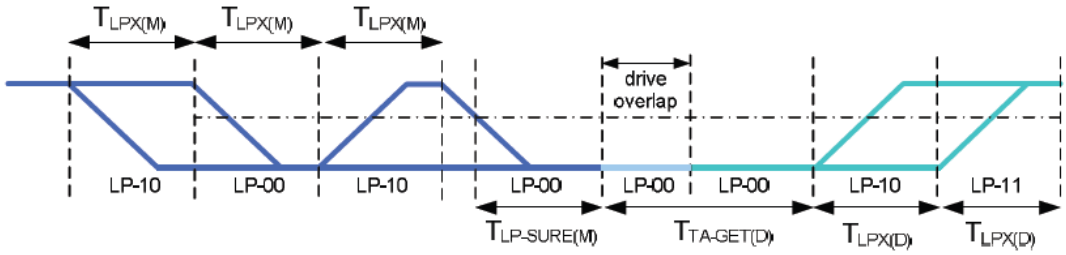
HS Data Transmission Burst



HS clock transmission



Turnaround Procedure



Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to Reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		60 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	96*UI			ns
$T_{LPX(M)}$	Transmitted length of any Low-Power state	100		150	ns