CUSTOMER APPROVAL SHEET

Company Name	
MODEL	**H245QBN02.0**
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☐ **CUSTOMER REMARK :**

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Product Specification

2.45" COLOR TFT-LCD MODULE

MODEL NAME: H245QBN02.0

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2012/08/06		First Draft.

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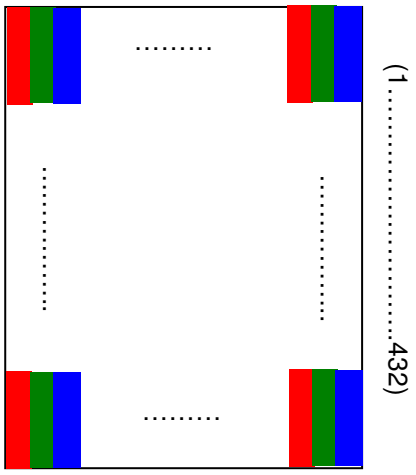
1. General Information

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	2.45(Diagonal)	
2	Display Resolution	dot	240RGB(H)×432(V)	
3	Overall Dimension	mm	31.82(H) × 33.72(V) × 1.242(T)	Note 1
4	Active Area	mm	30.24(H)×54.432(V)	
5	Pixel Pitch	mm	0.042(H)×0.126(V)	
6	Color Configuration	--	R. G. B. Stripe	Note 2
7	Color Depth	--	262k Colors	
8	NTSC Ratio	%	50	
9	Display Mode	--	ECB Normally white	
10	Weight	g	2.4g	
11	Interface		1-Lane MIPI I/F	
12	Viewing angle		CR>10:1 at 50 degree	

Note 1: Not include FPCs extrude stucture.

Note 2: Below figure shows dot stripe arrangement.

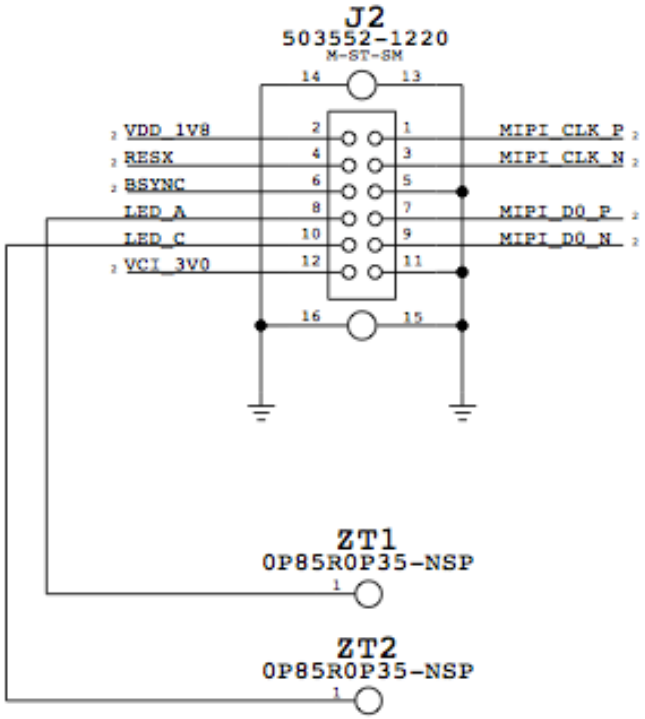


2. Electrical Specifications

1 Pin Assignment

TFT LCD Panel Pin Assignment:

No.	Pin Name	I/O	Description	Remarks
1	DISP_CLK_P	I/O	MIPI Clock	
2	1V8	-	1.8 V Power Supply	
3	DISP_CLK_N	I/O	MIPI Clock	
4	DISP_RESET_L	I	Reset	Active Low
5	GND	-	MIPI Data Guard	
6	DISP_BSYNC	O	Synchronization Pulse Signal	
7	DISP_D0_P	I/O	MIPI Data	
8	LCD_BL_CA	O	LCD Backlight Anode	
9	DISP_D0_N	I/O	MIPI Data	
10	LCD_BL_CC	O	LDC Backlight Cathode	
11	GND	-	MIPI Data Guard	
12	DISP_3V0	-	3.0 V Power Supply	



2 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Notes
Analog Power Supply Voltage	DISP_3V0	-0.3 ~ +5.0	V	
Logic I/O Voltage	1V8	-0.3 ~ +5.0	V	
Logic Input Voltage	VIN	-0.3 ~ (1.8+0.5)	V	1
LED Current	ILED	25	mA	2
Operating Temperature	TOP	-20 ~ +70	℃	3
Storage Temperature	TSTG	-30 ~ +80	℃	3
Humidity	H	5% ~ 95%	RH	3

(1)Applies to DISP_D0_N, DISP_D0_P, DISP_CLK_N, DISP_CLK_P, DISP_SYNC, DISP_RESET_L

(2) Applies for each LED individually

(3) See Section 7 for specific temperature and humidity test conditions.

3 Electrical DC Characteristics

a. Typical Operation Condition (GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Logic I/O Voltage	VDD3-VSS	1.71	1.8	1.89	V	
1.8V Input Current	IVDD3NM	-	-		mA	1
	IVDD3KEYNOTE					1
	IVDD3SLEEP					1
Analog Power Supply	VCI-VSS	2.85	3	3.15	V	
3.0V Input Current	IVCINM		-		mA	1
	IVCIKEYNOTE					1
	IVCISLEEP					1
LED Input Current	ILED		16	20	mA	
“H” Level Input Voltage	VIH	0.7VDD3	-	VDD3	V	1,2

“L” Level Input Voltage	VIL	0	-	0.3VDD3	V	1,2
“H” Level Output Voltage	VOH	0.8VDD3	-	VDD3	V	Iout = -1mA
“L” Level Output Voltage	VOL	0	-	0.2VDD3	V	Iout = +1mA
“H” Level Input Current	IIH	-	-	10	uA	
“L” Level Input Current	IIL	-10	-	-	uA	
Power, MIPI full refresh	PMIPI	-	-	40	mW	1
MIPI Operating Frequency	fMIPI	-	124	300	MHz	
Power, Normal mode. MIPI ULPS	PULPS	-	-	32	mW	5
Power Consumption, Backlight	PB	-		252	mW	3
Power Consumption, Suspend	PS	-	84	-	uW	4

(1) The specified current and power consumption are under the conditions at VCI = V_{DD} = 3.0V, VDD3 = V_{EE} = 1.8V, T = 25℃, and f_v = 60 Hz, large black/white checker pattern (20-pixel blocks), 240 Mbps MIPI refresh at 30 fps.

(2) Input mode of DISP_RESET_L, MTP, HIFA, DISP_SYNC

(3) LED Backlight assumptions: 3.2 V_f, 15.8 mA, 5 LED’s.

(4) VDD3 and VCI present, MIPI lane ULPS, Deep Sleep In mode

(5) The specified power consumption is under the conditions at VCI = V_{DD} = 3.0V, VDD3 = V_{EE} = 1.8V, T = 25℃, and f_v = 60 Hz, large black/white checker pattern (20-pixel blocks), MIPI in ULPS (LP11 for both CKL and D0)

4 Electrical Timing Characteristics

4.1. MIPI DC Characteristics

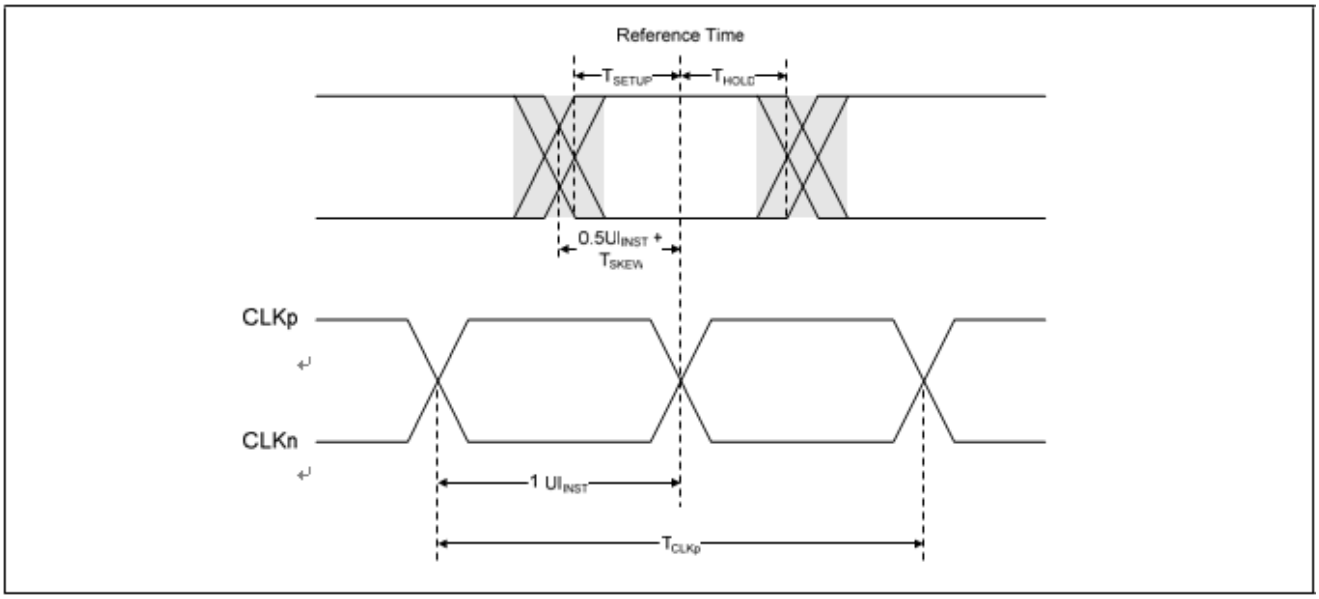
Items		Parameter	Min.	Typ.	Max.	Unit	Note
LP_TX	Thevenin output high level	VOH	1.1	1.2	1.3	V	
	Thevenin output low level	VOL	–50		50	mV	
	Output impedance of LP transmitter	ZOLP	110			Ω	1
HS_RX	Common-mode voltage HS receive mode	VCMRX (DC)	70		330	mV	2, 3
	Differential input high threshold	VIDTH			70	mV	
	Differential input low threshold	VIDTL	–70			mV	
	Single-ended input high voltage	VIHHS			460	mV	2
	Single-ended input low voltage	VILHS	–40			mV	2
	Single-ended threshold for HS termination enable	VTERM-EN			450	mV	
	Differential input impedance	ZID	80	100	125	Ω	
LP_RX	Logic 1 input voltage	VIH	880			mV	
	Logic 0 input voltage, not in ULP State	VIL			550	mV	
	Input hysteresis	VHYST	25			mV	
LP_CD	Logic 1 contention threshold	VIHCD	450			mV	
	Logic 0 contention threshold	VILCD			200	mV	

Note1. Even though a maximum value for ZOLP is not specified, the output impedance of the LP transmitter ensures that the TRLP/TFLP specification is met

Note2. Excluding additional RF interference of 100mV peak sine wave beyond 450MHz

Note3. This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz.

4.2. High Speed Data-Clock Timing



Host sends a differential clock signal to the S6D04D2 to be used for data sampling. This signal is a DDR (half- rate) clock and has one transition per data bit time. The timing relationship of the DDR Clock differential signal
to the Data differential signal is shown in Figure 1

Figure 1. MIPI data to clock timing definitions

MIPI pin characteristic specifications

Clock Parameter	Symbol	# of d-lane	Min	Typ	Max	Units	Notes
UI instantaneous	UIINST	1	2		12.5	ns	1,2

Note1. This value corresponds to a minimum 80 Mbps data rate.

Note2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

MIPI data-clock timing specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data to Clock Setup Time [receiver]	$T_{SETUP[RX]}$	0.15			UI_{INST}	2
Clock to Data Hold Time [receiver]	$T_{HOLD[RX]}$	0.15			UI_{INST}	2

Note1. Total silicon and package delay budget of 0.3* UI_{INST}

Note2. Total setup and hold window for receiver of 0.3* UI_{INST}