Version: 4.0

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CUSTOMER APPROVAL SHEET

Company Name	**eRay**
MODEL	**H381DLN01.0**
CUSTOMER	**Title :**
APPROVED	**Name :**

- ☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.____)**
- ☐ **CUSTOMER REMARK :**

1 Li-Hsin Rd. 2. Science-Based Industrial Park
Hsinchu 300, Taiwan, R.O.C.
Tel: +886-3-500-8800
Fax: +886-3-565-1840

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Total pages :	26
Date :	2016/01/18

Product Specification

3.81" COLOR AMOLED MODULE

MODEL NAME: H381DLN01.0

Trial-run sample P/N: 95.03H70.000

MP product P/N: (TBD)

< ◆ >Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
1.0	2015-11-09	1~26	First Draft
2.0	2015-11-09	9 17	Add Power IC pin note. Initial Setting Modify, change OVSS setting, RAM bypass.
3.0	2016-01-04	9	Recommend Power IC description.
4.0	2016-01-18	4 26	Physical spec. Outline Dimension(w IQE) Module outline (w IQE)

Contents

A. General Specification

1. Physical Specifications

NO	Item	unit	Specification	Remark
1	Screen Size	inch	3.81”	Diagonal
2	Display Resolution	--	1080(H) X 1200(V)	
3	Outline Dimension	mm	67.60 (H) x 78.95 (V) × 1.14(T)	
4	Active Area	mm	64.80 (H) x 72.0 (V)	
5	Pixel Pitch	um	60	
6	Color Configuration	--	R, G, B	
7	Color Depth	--	16.7M	8-bit x RGB
8	NTSC Ratio	%	100	CIE 1931
9	Display Mode	--	AMOLED	
10	Interface	--	MIPI DSI – Video Mode	
11	Driver IC		Raydium	RM69071

2. Pin Assignment

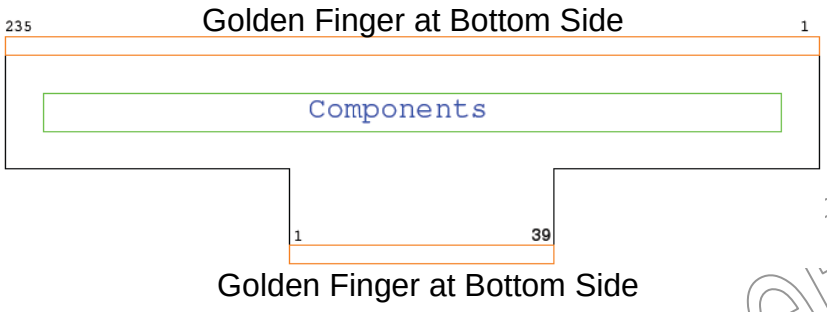
AMOLED Main FPC Pin assignment

#	Pin_name	I/O/P	Description
1	OVSS	P	OLED Power
2	OVSS	P	OLED Power
3	OVSS	P	OLED Power
4	OVDD	P	OLED Power
5	OVDD	P	OLED Power
6	OVDD	P	OLED Power
7	GND	G	Ground
8	D2N	I	MIPI DSI data
9	D2P	I	MIPI DSI data
10	GND	G	Ground
11	D0N	I/O	MIPI DSI data
12	D0P	I/O	MIPI DSI data
13	GND	G	Ground
14	CLKN	I	MIPI DSI clock
15	CLKP	I	MIPI DSI clock
16	GND	G	Ground
17	D1N	I	MIPI DSI data
18	D1P	I	MIPI DSI data
19	GND	G	Ground
20	D3N	I	MIPI DSI data
21	D3P	I	MIPI DSI data
22	GND	G	Ground
23	IOVCC	P	Display Driver Digital Power
24	IOVCC	P	Display Driver Digital Power
25	VCI	P	Display Driver Analog Power
26	VCI	P	Display Driver Analog Power
27	RESX	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
28	SWIRE	O	DC/DC power IC control signal, please connect to power IC CTRL pin
29	AVDD_EN	O	DC/DC power IC control signal, please connect to power IC EN pin
30	MTP	P	Leave this pin OPEN
31	GND	G	Ground
32	AVDD	P	Display Driver IC Source Analog Power
33	AVDD	P	Display Driver IC Source Analog Power
34	OVDD	P	OLED Power
35	OVDD	P	OLED Power
36	OVDD	P	OLED Power
37	OVSS	P	OLED Power

38	OVSS	P	OLED Power
39	OVSS	P	OLED Power

Recommended connector: Hirose FH35C-39S-0.3HW(50)

FPC Outline



3. Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Remark
OLED Power supply	OVDD	-	4.6	V	
OLED Power supply	OVSS	-	-2.9	V	
Driver IC Source power supply	AVDD	-	5.8	V	
Digital Power supply	IOVCC	-0.3	+1.95	V	
Analog Power supply	VCI	-0.3	+3.2	V	
Operating temperature (Ambient)	Topr	-20	+70	℃	
Storage temperature (Ambient)	Tstg	-40	+80	℃	

Note : If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operates with the absolute maximum ratings for a long time, the reliability may drop.

B. DC Characteristics

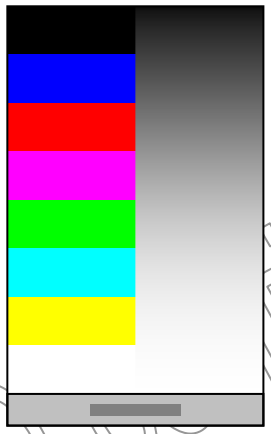
1. Typical Operating Conditions

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
OLED Power supply		OVDD	-	4.6	-	V	
OLED Power supply		OVSS	-	-2.9	-	V	
Driver IC Source power supply		AVDD	-	5.8	-	V	
Digital Power supply		IOVCC	1.65	1.8	1.95	V	
Analog Power supply		VCI	2.8	3	3.2	V	
Input Signal Voltage	H Level	V_{IH}	0.8* IOVCC	-	IOVCC	V	RESX
	L Level	V_{IL}	0	-	0.2* IOVCC	V	

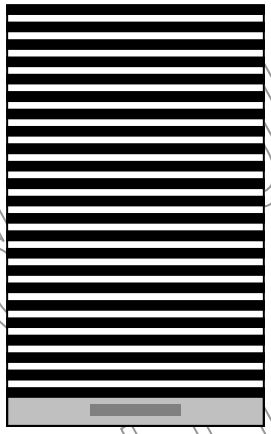
Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

2. Display Current Consumption

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Normal	I_{AVDD}	AVDD = 5.8V VCI = 3V IOVCC = 1.8V OVDD = 4.6V OVSS = -2.9V 25℃	-	15	30	mA	Note 1
	I_{VCI}		-	3	3	mA	
	I_{IOVCC}		-	38	40	mA	
	I_{OVDD}		-	-	16	mA	Note 2
	I_{OVSS}		-	-	16	mA	
Deep Standby (DSTB=1)	I_{AVDD}		-	-	1	uA	Display Off
	I_{VCI}		-	-	3	mA	
	I_{IOVCC}		-	-	30	uA	
	I_{OVDD}		-	-	0	uA	
	I_{OVSS}		-	-	0	uA	

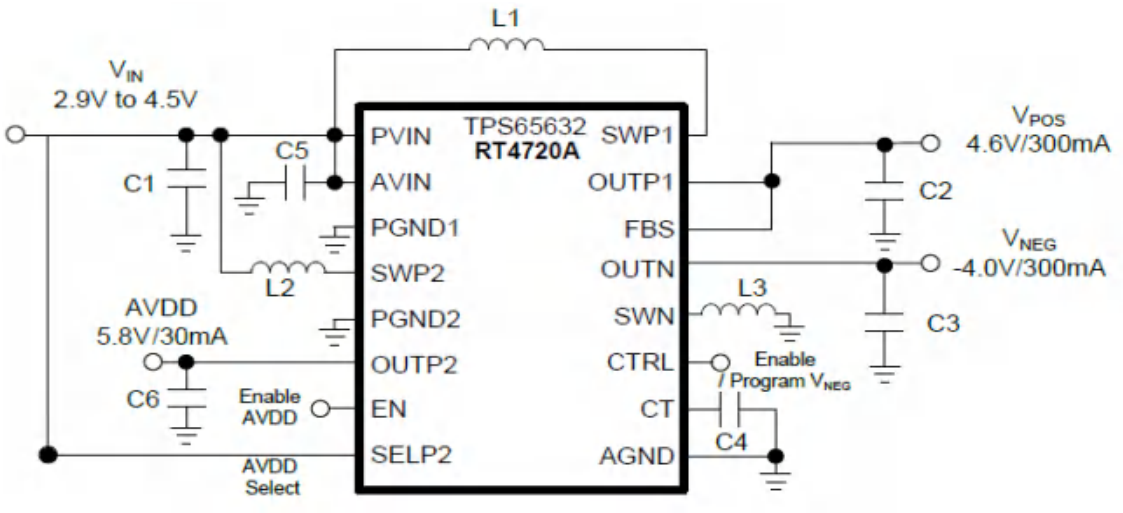


Note 1: Typ. Max.



Note 2: 100 nits White.

3. Recommend DC/DC Power IC Application Circuit



Note:

EN = AVDD_EN

CTRL = SWIRE

Power IC

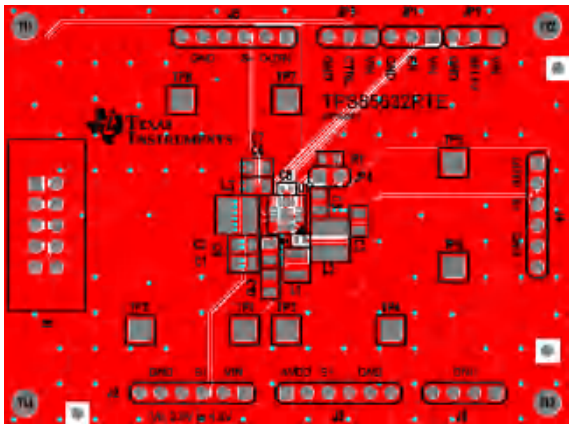
Vendor	Model
TI	TPS65632RTER
Richtek	RT4720A

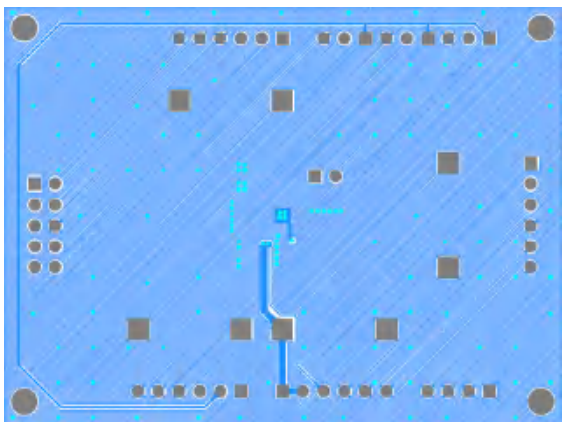
AUO don't suggest use other power IC instead of TPS65632RTER/ RT4720A , since they don't be qualified by AUO.

Bill of Materials

	Value	Part Number	Manufacturer
C1	3 x 10μF	GRM21BR71A106KE51	Murata
C2, C6	10μF	GRM21BR71A106KE51	Murata
C3	2 x 10μF	GRM21BR71A106KE51	Murata
C4, C5	100nF	GRM21BR71E104KA01	Murata
L1, L3	4.7μH	XFL4020-4R7ML	CoilCraft
L2	10μH	MMPP252012-100N	Coil Master

Example of board layout



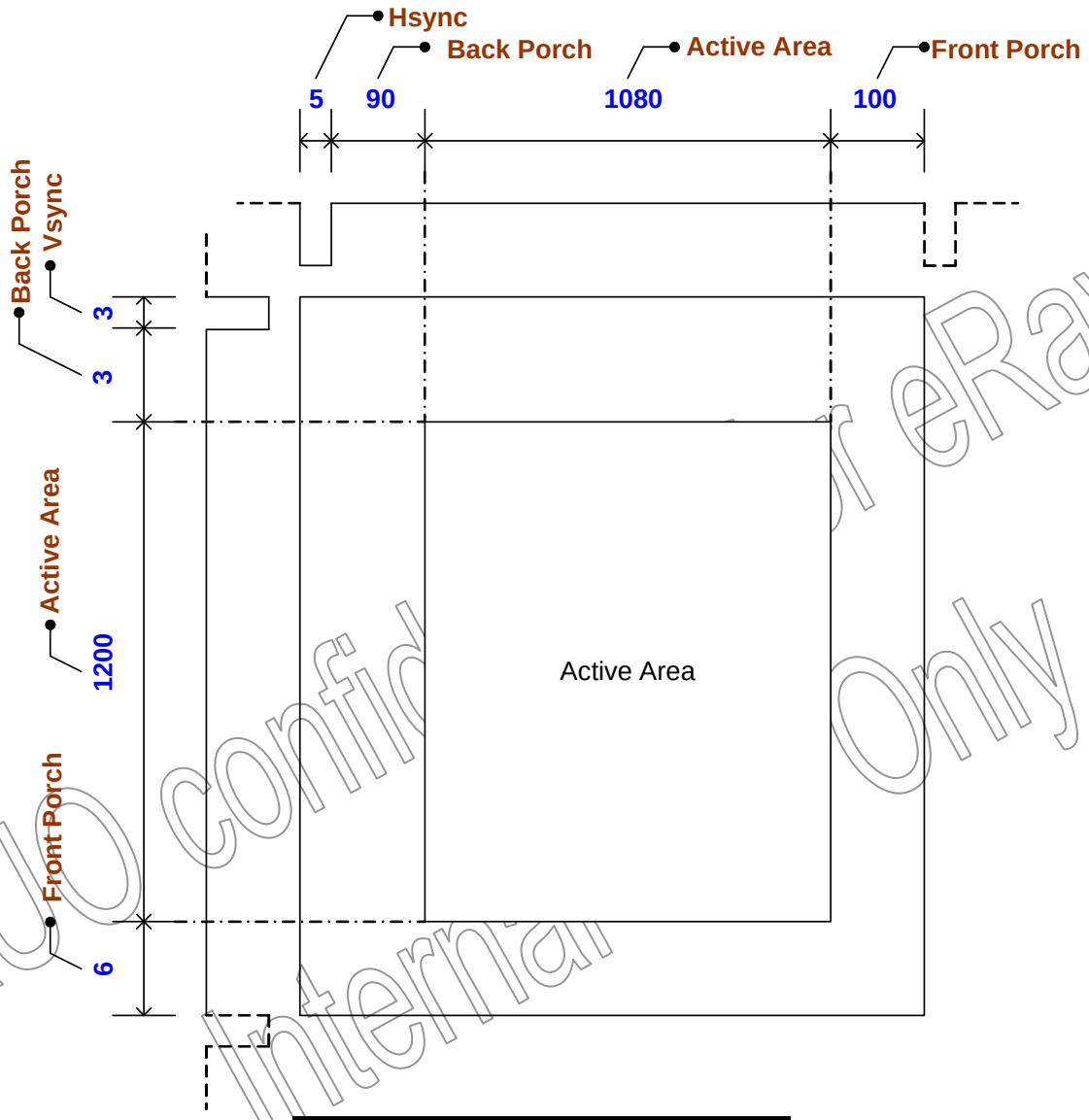


Top Layer

Bottom Layer

C. AC Characteristics

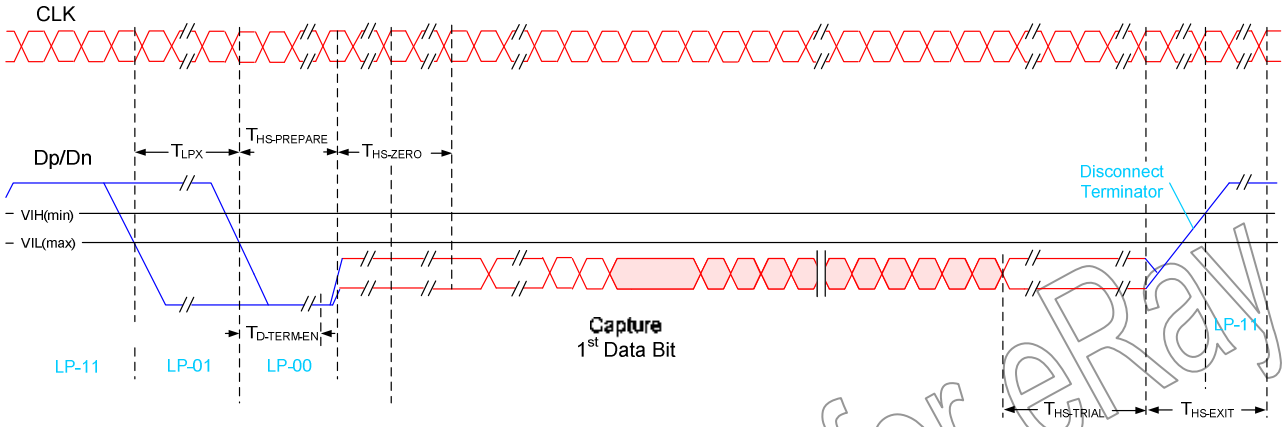
1. Display Video Timing



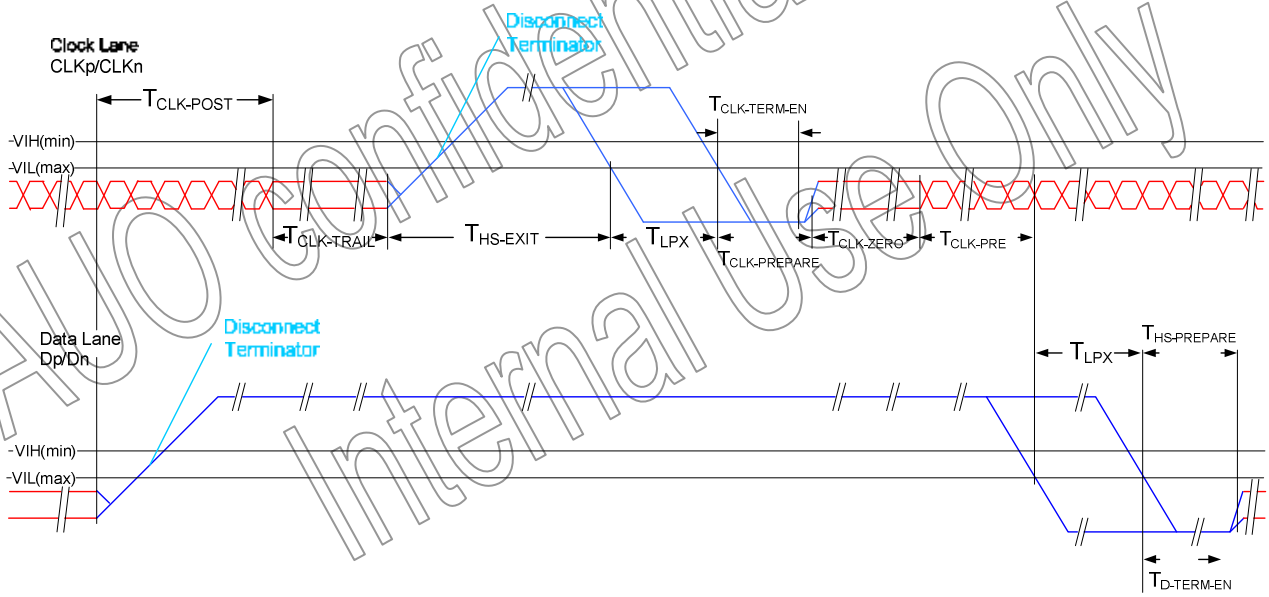
Name	Quantity	Unit
Frame Rate	90	Hz
Line Time	9.17	us
H Sync	5	Dot
H Back Porch	90	Dot
H Active	1080	Dot
H Front Porch	100	Dot
H Total	1275	Dot
V Sync	3	Line
V Back Porch	3	Line
V Active	1200	Line
V Front Porch	6	Line
V Total	1212	Line

2. MIPI Interface Characteristics

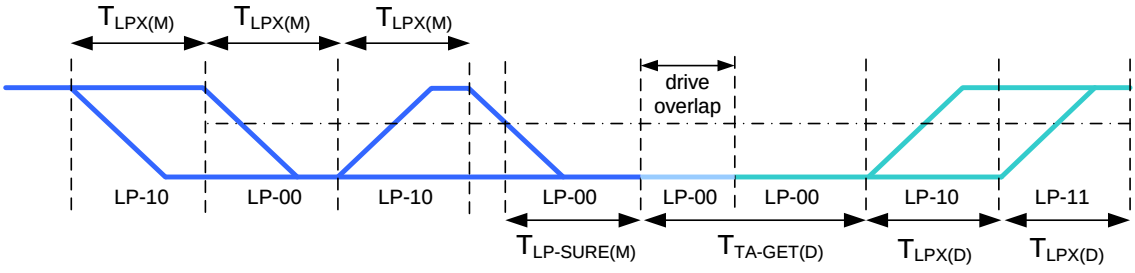
HS Data Transmission Burst



HS clock transmission



Turnaround Procedure



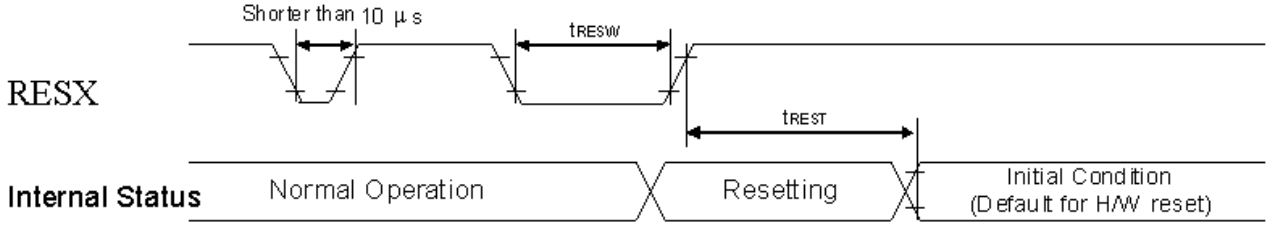
Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns
$T_{TA-SURE(M)}$	Time that the display module waits after the	$T_{LPX(M)}$		$2*T_{LPX(M)}$	ns

	LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.				
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5*T_{LPX(D)}$		ns
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4*T_{LPX(D)}$		ns
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2*T_{LPX(D)}$	ns

3. Display RESET Timing Characteristics

Reset input timing



IOVCC=1.65 to 1.95V, VCI=2.8 to 3.2V, GND=0V, Ta=-20 to 70℃

Timing Parameters

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

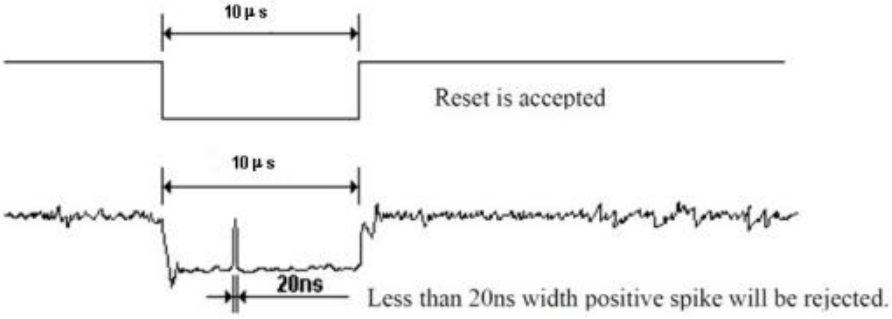
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Invalid Reset
Longer than 10µs	Valid Reset
Between 5µs and 10µs	Reset Initialization Precedure

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

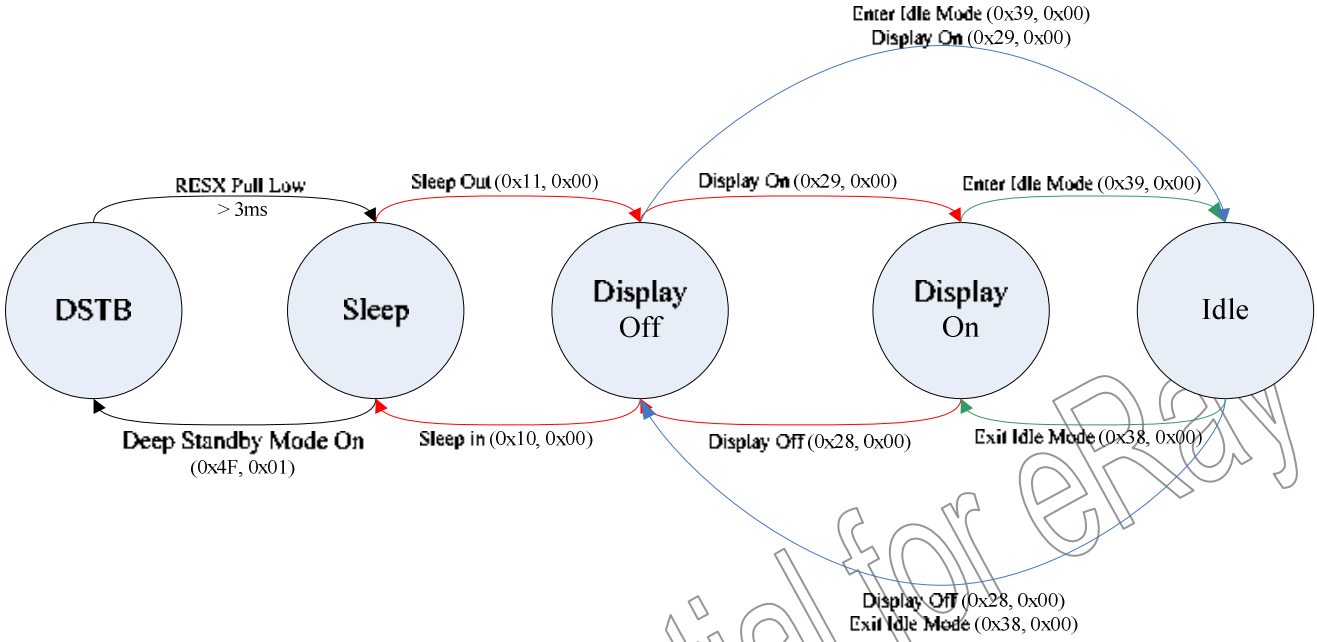
Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



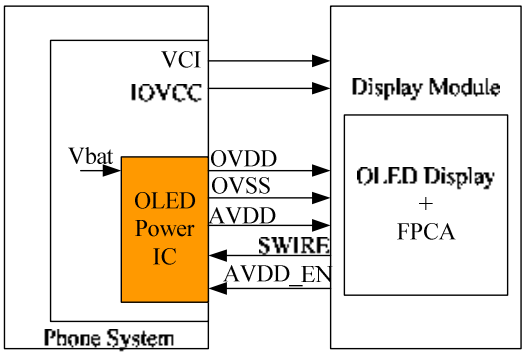
Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

4. Recommended Operating Sequence

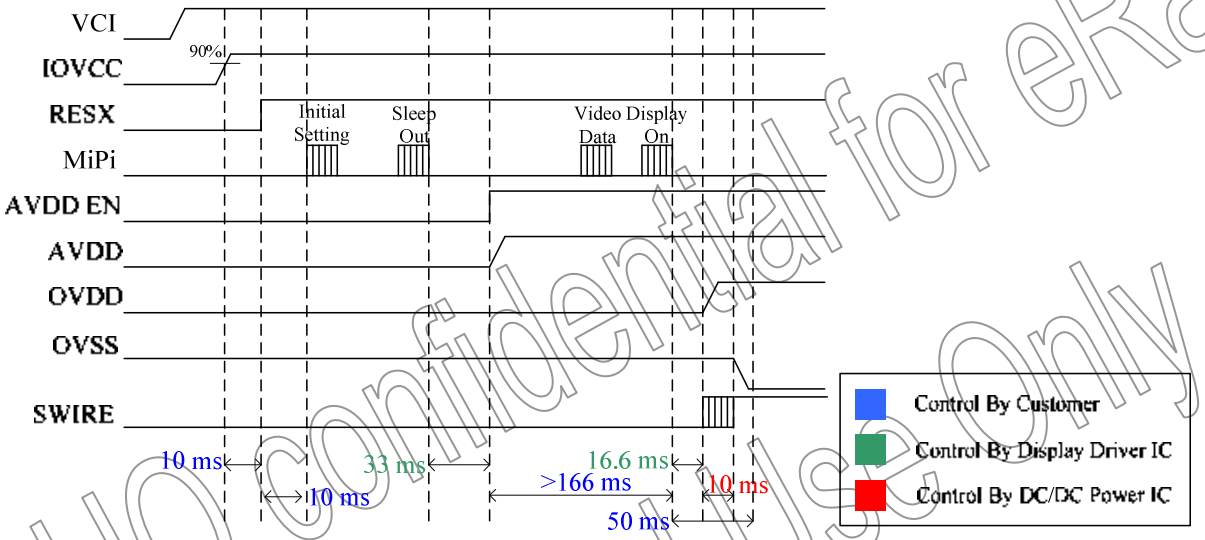
State Diagram



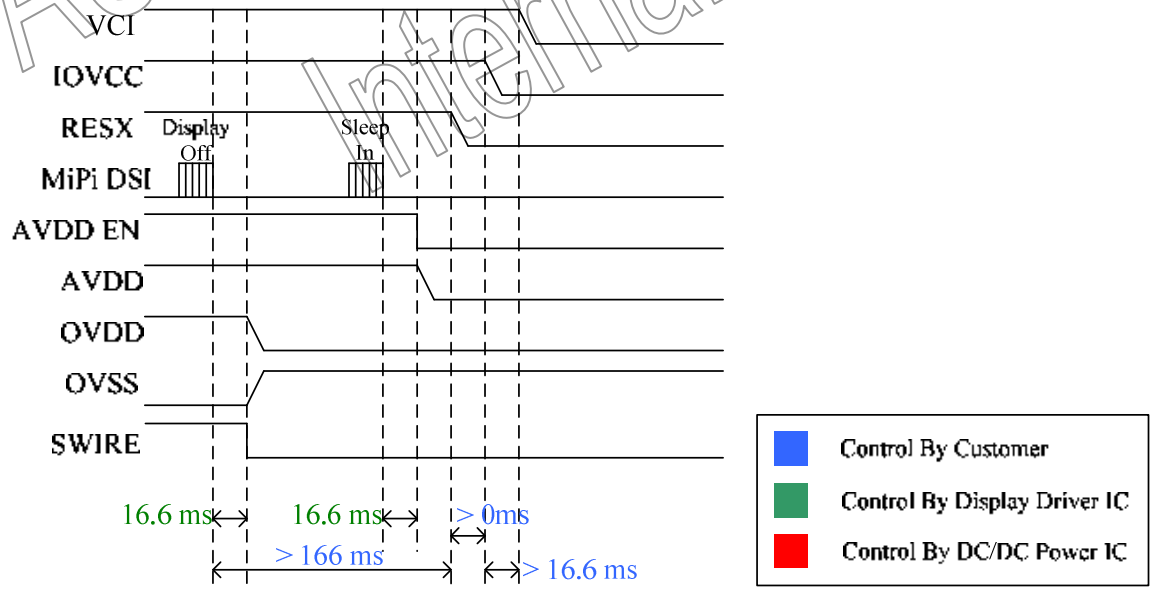
Power Structure



Power on sequence



Power off sequence



Please follow AUO's main FPC design suggestion.

Timing settings of Green are controlled by display driver IC. (The settings couldn't be adjusted.)

Timing settings of Red are controlled by DC/DC power IC. (The settings couldn't be adjusted.)

Initial Setting:

Item	Parameter Quantity	Address	P0
1	1	0xFE	0x08
2	1	0x07	0x1A
3	1	0xFE	0x00
4	1	0xC2	0x03
5	1	0x51	0xFF

Sleep Out:

Item	Parameter Quantity	Address	P0
1	1	0x11	0x00

Display On:

Item	Parameter Quantity	Address	P0
1	1	0x29	0x00

Sleep In

Item	Parameter Quantity	Address	P0
1	1	0x10	0x00

Display Off:

Item	Parameter Quantity	Address	P0
1	1	0x28	0x00

D. Optical Specification

All optical specifications are measured under typical condition. (Note 1)

Item		Abbr.	Min.	Typ.	Max.	Unit	Remark
Brightness		Y @ θ=0°	80	100		nits	Note 2
Contrast ratio		@ θ=0°	3000	--	--	--	
		@ θ=60°	900	--	--	--	
		@ θ=80°	480	--	--	--	
Viewing angle (CR > 480)		Top	80	--	--	Deg.	
		Bottom	80	--	--	Deg.	
		Left	80	--	--	Deg.	
		Right	80	--	--	Deg.	
Chromacity (CIE1931)	Red	x	0.640	0.670	0.700	--	Note 3
		y	0.300	0.330	0.360	--	
	Green	x	0.186	0.236	0.286	--	
		y	0.661	0.711	0.761	--	
	Blue	x	0.090	0.130	0.170	--	
		y	0.025	0.065	0.105	--	
	White	x	0.28	0.30	0.32	--	
		y	0.29	0.31	0.33	--	
Uniformity		9 points	70	--	--	%	Note 4
Flicker			--	--	-30	dB	Note 5
Crosstalk			--	--	4.0	%	Note 6
Life Time		95% @ 25°C	100			hrs	Note 7
Response Time		25°C Between 10% & 90%			2	ms	For Reference

Please follow AUO's main FPC design suggestion.

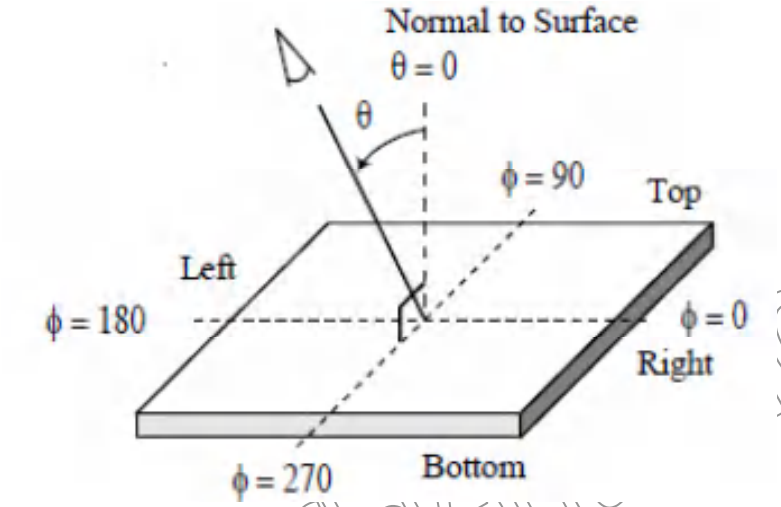
If you don't follow the AUO's main FPC design suggestion, then optical performance is not guaranteed.

Note 1: **Typical Condition**

Optical characteristics should be measured at the **center area** of the display with **Konica Minolta CA-310** and at the ambient temperature = **25℃±2℃** and in the dark room.

Note 2: **Viewing Angle & Contrast Ratio**

The optical performance is specified as the driver IC located at **ϕ=270˚**.



Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at "White" pattern}}{\text{Photo detector output when OLED is at "Black"}}$$

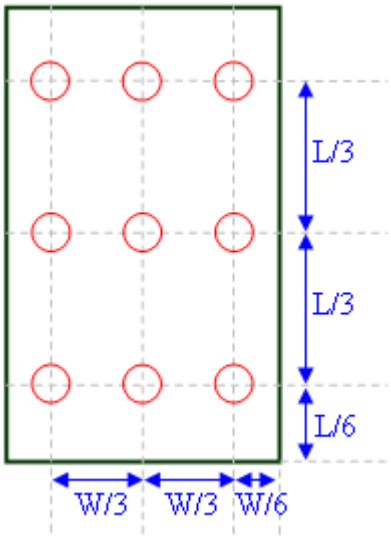
Note 3: **Chromacity**

Chromacity of **R, G, B** pattern are measured at Gray Level "**255**".

Chromacity of **White** pattern are measured at Gray Level "**255**".

Note 4: **Uniformity**

Uniformity under **White(L255)** pattern = $\frac{\text{minimum luminance of } \mathbf{9}}{\text{maximum luminance of } \mathbf{9}}$



Note 5: Flicker

Suggested Instruments: **Konica Minolta CA-310**

Measuring Point: **Center point of 128th gray**

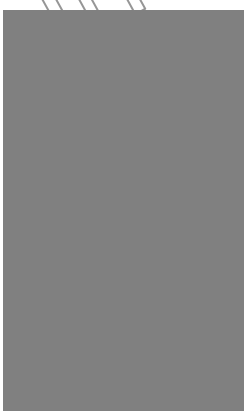
The flicker level is defined using Fast Fourier Transformation (FTT) as follows:

$$Flicker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad (dB)$$

where fFFTC(n) is the nth FFT coefficient, and fFFTC(0) is the 0th FFT coefficient which is DC component. FS(Hz) is the flicker sensitivity as a function of frequency.

The flicker level shall be measured with the test pattern in below.

Test Pattern: **L128 Gray**

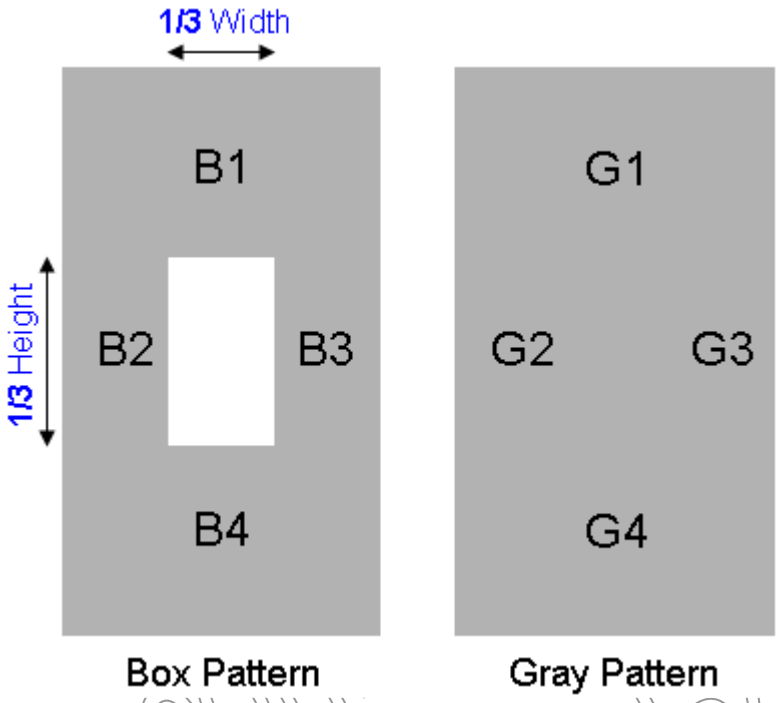


Note 6: **Crosstalk**

Crosstalk shall be calculated by the luminance of **B1~B4** and **G1~G4** in the patterns shown below.

Box Pattern: **L128** gray level background with a **L255** White window in the central area.

Gray Pattern: **L128** gray level background only.



Crosstalk

$$\equiv \textbf{\textit{Maximum}}: \frac{|B1-G1|}{G1}, \frac{|B2-G2|}{G2}, \frac{|B3-G3|}{G3}, \frac{|B4-G4|}{G4} \times 100\%$$

Note 7: **Life Time**

OLED life time is defined by the **Minimum Duration Time** that the luminance is decayed to a specific ratio (ex. **95%**) of initial state.

Test Pattern under duration period: **L255** White

E. Reliability Test Items

In the standard condition, there should **not** be any display function NG issue occurred during the reliability test and the performance is confirmed after panel is left at room temperature. All the cosmetic specifications are judged only **before** the reliability stress.

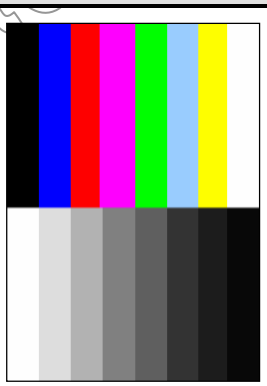
No.	Test items	Conditions		Remark
1	High Temperature Storage	T= 80℃	100Hrs	Note 1
2	Low Temperature Storage	T= -40℃	100Hrs	
3	High Temperature Operation	T= 70℃	100Hrs	
4	Low Temperature Operation	T= -20℃	100Hrs	
5	High Temperature & Humidity Operation	T= 60℃. 90% RH	100Hrs	
6	Thermal Shock	-30℃ ~ 80℃, 30 cycle, 1Hrs/cycle		Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, Class B Air = ± 8 kV, Class B		Note 2
8	Vibration (With Carton)	1.5Grms, 10~200Hz Total time: 90 mins (30 mins/axis for X, Y, Z)		
9	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		

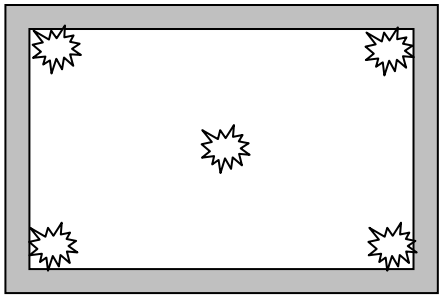
Note 1 : T＝Ambient Temperature

Please follow AUO's main FPC design suggestion.

If you don't follow the AUO's main FPC design suggestion, then reliability items are not guaranteed.

Note 2 : All test techniques follow IEC 61000-4-2 standard.

Test Condition		Note
Pattern		
Procedure & Set-up	Contact Discharge：330Ω, 150pF, 1sec, 5 point, 10 times/point Air Discharge：330Ω, 150pF, 1sec, 5 point, 10 times/point	

		
Criteria	Class B – Some performance degradation allowed. No data lost. Self-recoverable hardware failure.	
Others	1. Air Discharge: Gun to Panel Distance>1cm 2. No SPI command, keep default register settings.	