Version: 1.0

Total Page: 29

# CUSTOMER APPROVAL SHEET

**Company Name** Acer

**MODEL** **H477ULN01.1**

**CUSTOMER** **Title :**

**APPROVED** **Name :**

- ☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.____)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.____)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.____)**
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|---|---|
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# Product Specification

## 4.77" COLOR AMOLED MODULE

## MODEL NAME: H477ULN01.1

Trial-run sample P/N: 95.04H85.102

MP product P/N: (95.04H85.102)

< >Preliminary Specification

< ◆ >Final Specification



Note: The content of this specification is subject to change.

**Record of Revision**

| Version | Revise Date | Page | Content |
|---|---|---|---|
| 0.0 | 2016-09-29 | 1~26 | First Draft |
| 0.1 | 2017.10.02 | | Cascade IC |
| 1.0 | 2018.08.16 | | Update MP Part No.<br>95.04H85.101 → 95.04H85.102<br>(For Photo-System Upgrade, C3+V1.9) |
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# Contents

# A. General Specification

## 1. Physical Specifications

| NO | Item | unit | Specification | Remark |
|---|---|---|---|---|
| 1 | Screen Size | inch | 4.77” | Diagonal |
| 2 | Display Resolution | -- | 1792(H) X 2240(V) | |
| 3 | Outline Dimension | mm | 80.512 (H) x 103.240 (V)×**1.159(T)** | |
| 4 | Active Area | mm | 75.712 (H) x 94.640 (V) | |
| 5 | Pixel Pitch | um | 42.25 | |
| 6 | Color Configuration | -- | R, G, B | |
| 7 | Color Depth | -- | 16.7M | 8-bit x RGB |
| 8 | NTSC Ratio | % | 100 | CIE 1931 |
| 9 | Display Mode | -- | AMOLED | |
| 10 | Interface | -- | MIPI DSI – Video Mode | |
| 11 | Driver IC | | Raydium | |

## 2. Pin Assignment

L_Connector：

| # | Pin_name | I/O/P/N | Description | # | Pin_name | I/O/P/N | Description |
|---|---|---|---|---|---|---|---|
| 1 | OVSS | P | OLED Power | 2 | L_D3P_B | I | MIPI DSI Lane |
| 3 | OVSS | P | OLED Power | 4 | L_D3N_B | I | MIPI DSI Lane |
| 5 | OVSS | P | OLED Power | 6 | GND | G | Ground |
| 7 | GND | G | Ground | 8 | L_D2P_B | I | MIPI DSI Lane |
| 9 | OVDD | P | OLED Power | 10 | L_D2N_B | I | MIPI DSI Lane |
| 11 | OVDD | P | OLED Power | 12 | GND | G | Ground |
| 13 | OVDD | P | OLED Power | 14 | L_CKP_B | I | MIPI DSI Lane |
| 15 | GND | G | Ground | 16 | L_CKN_B | I | MIPI DSI Lane |
| 17 | AVDD | P | IC Power | 18 | GND | G | Ground |
| 19 | IOVCC | P | IC Power | 20 | L_D1P_B | I | MIPI DSI Lane |
| 21 | VCI | P | IC Power | 22 | L_D1N_B | I | MIPI DSI Lane |
| 23 | L_MTP | N | Open | 24 | GND | G | Ground |
| 25 | GND | G | Ground | 26 | L_D0P_B | I/O | MIPI DSI Lane |
| 27 | SWIRE | O | PWR IC Setting Pin | 28 | L_D0N_B | I/O | MIPI DSI Lane |
| 29 | GND | G | Ground | 30 | GND | G | Ground |
| 31 | AVDD_EN | O | AVDD Enable Pin | 32 | L_D3P_A | I | MIPI DSI Lane |
| 33 | GND | G | Ground | 34 | L_D3N_A | I | MIPI DSI Lane |
| 35 | L_TE | O | TE Signal | 36 | GND | G | Ground |
| 37 | GND | G | Ground | 38 | L_D2P_A | I | MIPI DSI Lane |
| 39 | RESX | I | RESET Pin | 40 | L_D2N_A | I | MIPI DSI Lane |
| 41 | NC | N | Open | 42 | GND | G | Ground |
| 43 | L_ERR | O | MiPi Error Flag | 44 | L_CKP_A | I | MIPI DSI Lane |
| 45 | GND | G | Ground | 46 | L_CKN_A | I | MIPI DSI Lane |
| 47 | OVDD | P | OLED Power | 48 | GND | G | Ground |
| 49 | OVDD | P | OLED Power | 50 | L_D1P_A | I | MIPI DSI Lane |
| 51 | OVDD | P | OLED Power | 52 | L_D1N_A | I | MIPI DSI Lane |
| 53 | GND | G | Ground | 54 | GND | G | Ground |
| 55 | OVSS | P | OLED Power | 56 | L_D0P_A | I/O | MIPI DSI Lane |
| 57 | OVSS | P | OLED Power | 58 | L_D0N_A | I/O | MIPI DSI Lane |
| 59 | OVSS | P | OLED Power | 60 | GND | G | Ground |

R_Connector：

| # | Pin_name | I/O/P/N | Description | # | Pin_name | I/O/P/N | Description |
|---|---|---|---|---|---|---|---|
| 1 | OVSS | P | OLED Power | 2 | R_D3P_B | I | MIPI DSI Lane |
| 3 | OVSS | P | OLED Power | 4 | R_D3N_B | I | MIPI DSI Lane |
| 5 | OVSS | P | OLED Power | 6 | GND | G | Ground |
| 7 | GND | G | Ground | 8 | R_D2P_B | I | MIPI DSI Lane |
| 9 | OVDD | P | OLED Power | 10 | R_D2N_B | I | MIPI DSI Lane |
| 11 | OVDD | P | OLED Power | 12 | GND | G | Ground |
| 13 | OVDD | P | OLED Power | 14 | R_CKP_B | I | MIPI DSI Lane |
| 15 | GND | G | Ground | 16 | R_CKN_B | I | MIPI DSI Lane |
| 17 | AVDD | P | IC Power | 18 | GND | G | Ground |
| 19 | IOVCC | P | IC Power | 20 | R_D1P_B | I | MIPI DSI Lane |
| 21 | VCI | P | IC Power | 22 | R_D1N_B | I | MIPI DSI Lane |
| 23 | R_MTP | N | Open | 24 | GND | G | Ground |
| 25 | GND | G | Ground | 26 | R_D0P_B | I/O | MIPI DSI Lane |
| 27 | NC | N | Open | 28 | R_D0N_B | I/O | MIPI DSI Lane |
| 29 | GND | G | Ground | 30 | GND | G | Ground |
| 31 | NC | N | Open | 32 | R_D3P_A | I | MIPI DSI Lane |
| 33 | GND | G | Ground | 34 | R_D3N_A | I | MIPI DSI Lane |
| 35 | R_TE | O | TE Signal | 36 | GND | G | Ground |
| 37 | GND | G | Ground | 38 | R_D2P_A | I | MIPI DSI Lane |
| 39 | NC | N | Open | 40 | R_D2N_A | I | MIPI DSI Lane |
| 41 | GND | G | Ground | 42 | GND | G | Ground |
| 43 | R_ERR | O | MiPi Error Flag | 44 | R_CKP_A | I | MIPI DSI Lane |
| 45 | GND | G | Ground | 46 | R_CKN_A | I | MIPI DSI Lane |
| 47 | OVDD | P | OLED Power | 48 | GND | G | Ground |
| 49 | OVDD | P | OLED Power | 50 | R_D1P_A | I | MIPI DSI Lane |
| 51 | OVDD | P | OLED Power | 52 | R_D1N_A | I | MIPI DSI Lane |
| 53 | GND | G | Ground | 54 | GND | G | Ground |
| 55 | OVSS | P | OLED Power | 56 | R_D0P_A | I/O | MIPI DSI Lane |
| 57 | OVSS | P | OLED Power | 58 | R_D0N_A | I/O | MIPI DSI Lane |
| 59 | OVSS | P | OLED Power | 60 | GND | G | Ground |

## B. DC Characteristics

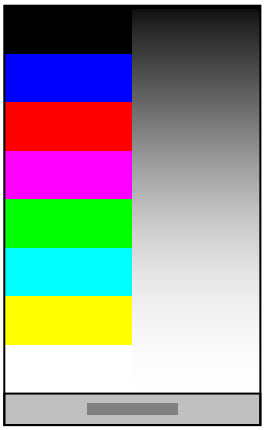
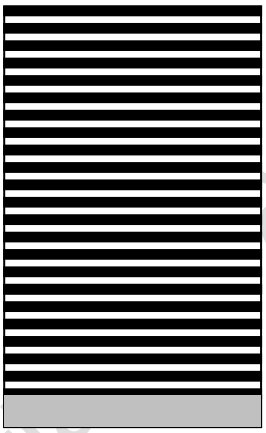
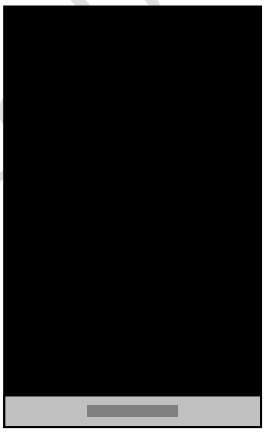
### 1. Typical Operating Conditions

| Item | | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| OLED Power supply | | OVDD | 4.57 | 4.6 | 4.63 | V | |
| OLED Power supply | | OVSS | -4.43 | -4.4 | -4.37 | V | |
| Driver IC Source power supply | | AVDD | 6.04 | 6.1 | 6.16 | V | |
| Digital Power supply | | IOVCC | 1.65 | 1.8 | 1.95 | V | |
| Analog Power supply | | VCI | 3.15 | 3.3 | 3.45 | V | |
| Input Signal Voltage | H Level | $V_{IH}$ | TBD | TBD | TBD | V | RESX |
| | L Level | $V_{IL}$ | TBD | TBD | TBD | V | |

Note 1: The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

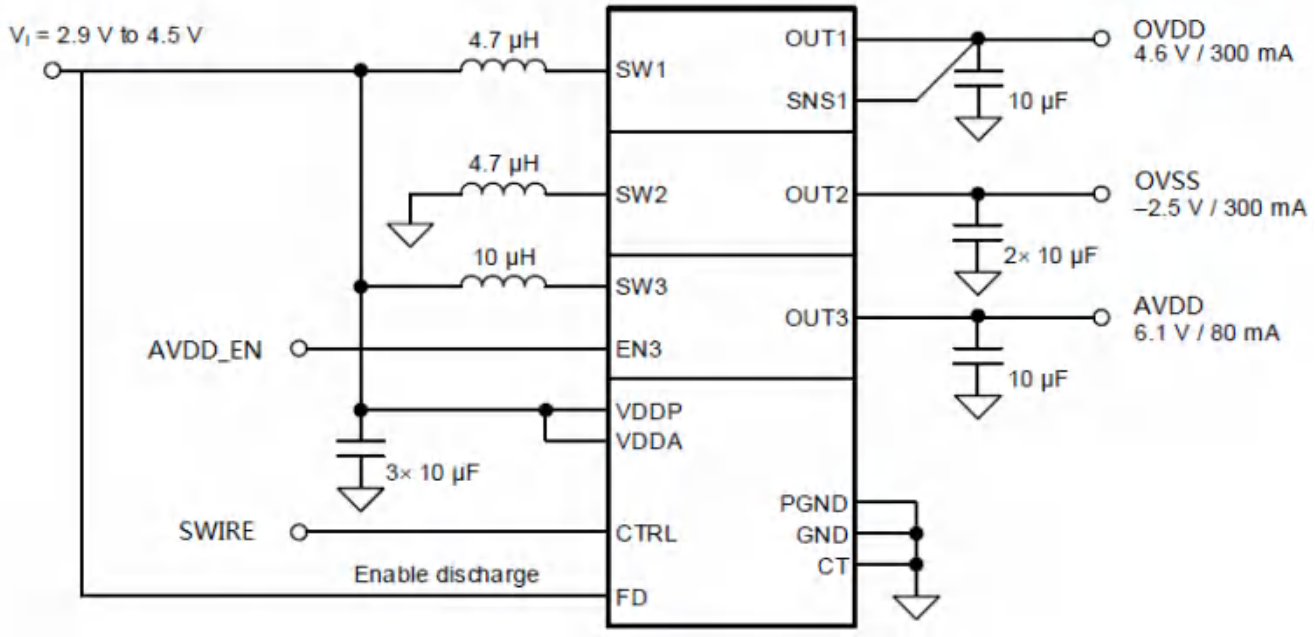
## 2. Display Current Consumption

| Mode | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| **Normal** | $I_{AVDD}$ | AVDD = 6.1V<br>VCI = 3.3V<br>IOVCC = 1.8V<br>OVDD = 4.6V<br>OVSS = -4.4V<br>25℃ | 70 | 77 | 84 | mA | Note 1 |
| | $I_{VCI}$ | | 4 | 4.4 | 4.8 | mA | |
| | $I_{IOVCC}$ | | 171 | 190 | 209 | mA | |
| | $I_{OVDD}$ | | 63 | 70 | 77 | mA | Note 2 |
| | $I_{OVSS}$ | | 63 | 70 | 77 | mA | |
| **Deep Standby (DSTB=1)** | $I_{AVDD}$ | | TBD | TBD | TBD | uA | Display Off |
| | $I_{VCI}$ | | TBD | TBD | TBD | mA | |
| | $I_{IOVCC}$ | | TBD | TBD | TBD | uA | |
| | $I_{OVDD}$ | | TBD | TBD | TBD | uA | |
| | $I_{OVSS}$ | | TBD | TBD | TBD | uA | |

Note 1: Typ.  Max.  min. 

Note 2: 150 nits White.

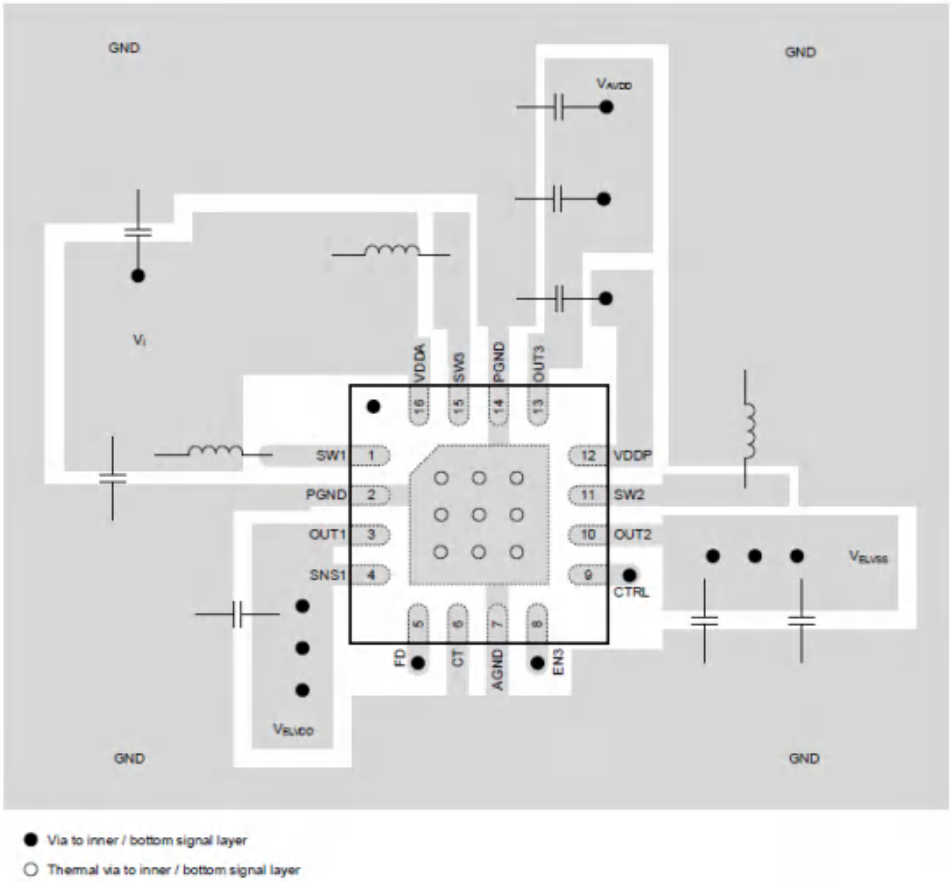
3. **Recommend DC/DC Power IC Application Circuit**




**Power IC**

| Vendor | Model |
|---|---|
| TI | TPS65651 |
| Richtek | TBD |

Example of board layout



# C. AC Characteristics

## 1. Display Video Timing

**Please refer to H477ULN01.2 Application Note.**

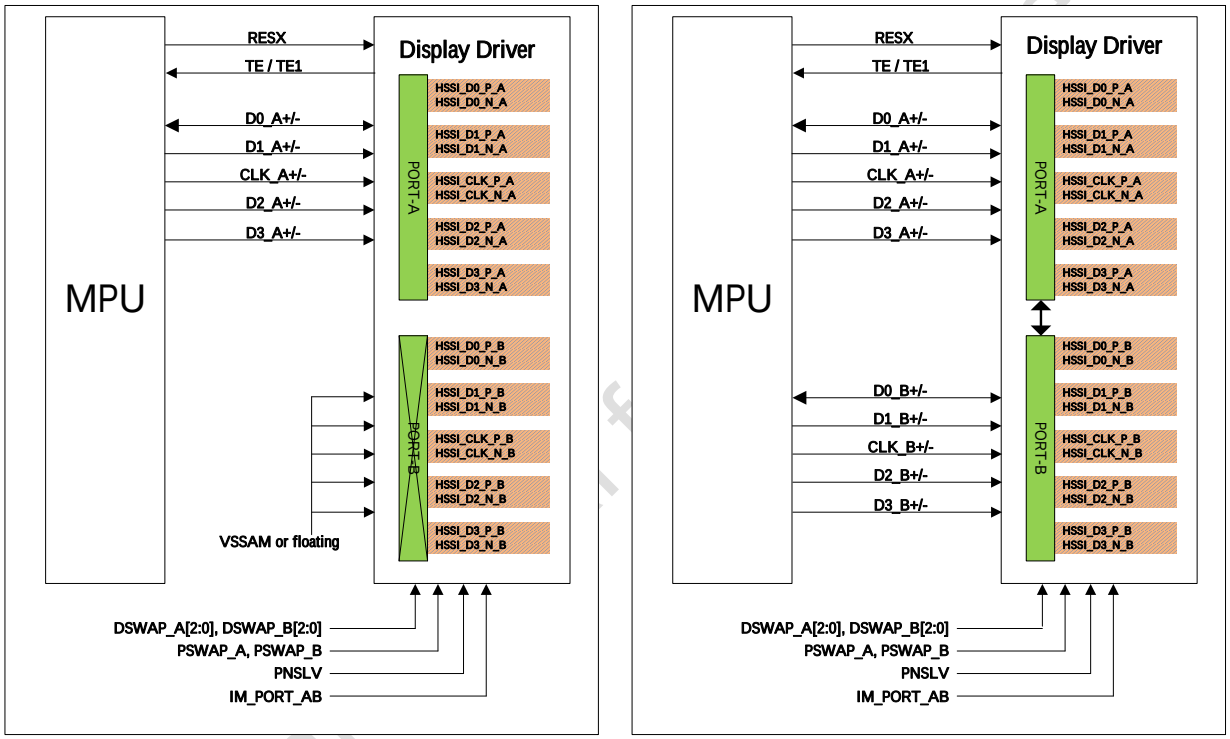
## 2. Scan Direction

**Please refer to H477ULN01.2 Application Note.**

## 3. MIPI Interface Characteristics

### Interface Connection

There are 2 options for the number of total MIPI data lanes depending on the total input data bandwidth. The left and right figures are used to represent the one-port and two-port system, respectively.



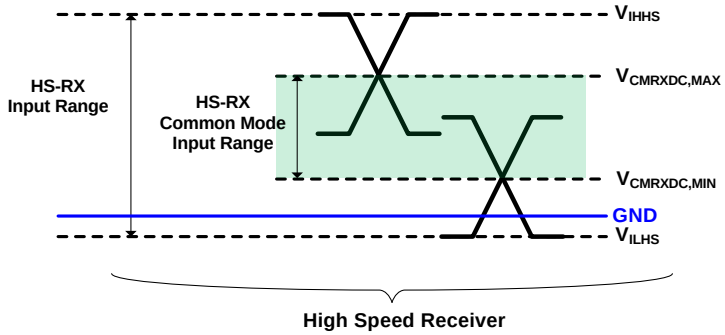

### Receiver Characteristics

#### High-Speed Receiver

The differential input high and low threshold voltages of the HS receiver are denoted by $V_{IDTH}$ and $V_{IDTL}$, respectively. $V_{ILHS}$ and $V_{IHHS}$ are the single-ended, input low and input high voltages, respectively. $V_{CMRXDC}$ is the differential input common-mode voltage. The HS receiver shall be able to detect differential signals at its DP and DN input signal pins when both signal voltages, $V_{DP}$ and $V_{DN}$, are within the common-mode voltage range and if the voltage difference of $V_{DP}$ and $V_{DN}$ exceeds either $V_{IDTH}$ or $V_{IDTL}$. The High-Speed receiver shall receive High-Speed data correctly while rejecting common-mode interference $\Delta V_{CMRX(HF)}$ and $\Delta V_{CMRX(LF)}$.

During operation of the HS receiver, termination impedance $Z_{ID}$ is required between the DP and DN pins of the HS receiver. $Z_{ID}$ shall be disabled when the module is not in the HS receive mode.

$C_{CM}$ is the common-mode AC termination, which ensures a proper termination of the receiver at higher frequencies. For higher data rates, $C_{CM}$ is needed at the termination centre tap in order to meet the common-mode reflection requirements.




## HS Receiver Specifications

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| $V_{CMRXDC}$ | Common-mode voltage for HS receiver | 70 | | 330 | mV | 1,2 |
| $V_{IDTH}$ | Differential input high threshold | | | 70 | mV | |
| $V_{IDTL}$ | Differential input low threshold | -70 | | | mV | |
| $V_{IHHS}$ | Single-ended input high voltage | | | 460 | mV | 1 |
| $V_{ILHS}$ | Single-ended input low voltage | -40 | | | mV | 1 |
| $Z_{ID}$ | Differential input impedance | 80 | 100 | 125 | Ω | |
| $C_{CM}$ | Common-mode termination | | | 60 | pF | 3 |

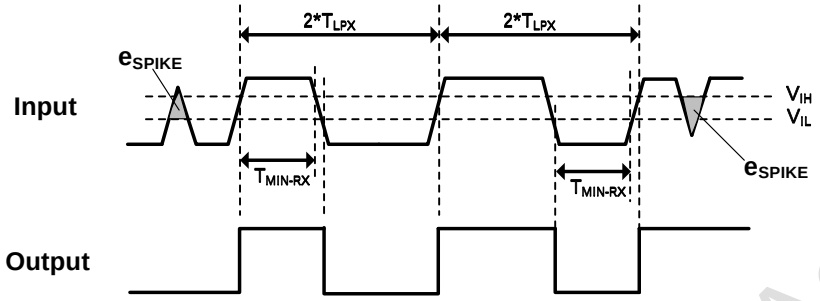
**Notes:**

1. **Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.**
2. **Values in this table include a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz**
3. **For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.**
4. **Voltage difference compared to the DC average common-mode potential.**

**Low-Power Receiver**

The Low-Power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. The input low-level voltage, $V_{IL}$, is the voltage at which the receiver is required to detect a low state in the input signal. A lower input voltage, $V_{IL-ULPS}$, may be used when the receiver is in the Ultra-Low Power State. $V_{IL}$ is larger than the maximum single-ended Line voltage during HS transmission. Therefore, a LP receiver shall detect low during HS signaling. The input high-level voltage, $V_{IH}$, is the voltage at which the receiver is required to detect a high state in the input signal. In order to reduce noise sensitivity on the received signal, an LP receiver shall incorporate a hysteresis, defined as $V_{HYST}$.

The LP receiver shall reject any input signal smaller than $e_{SPIKE}$. Signal pulses wider than $T_{MIN-RX}$ shall propagate through the LP receiver.




**Low-Power Receiver Specifications**

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Logic 1 input voltage | 880 | | | mV | |
| $V_{IL}$ | Logic 0 input voltage, not in ULP State | | | 550 | mV | |
| $V_{IL-ULPS}$ | Logic 0 input voltage, ULP State | | | 300 | mV | |
| $V_{HYST}$ | Input hysteresis | 25 | | | mV | |
| $e_{SPIKE}$ | Input pulse rejection | | | 300 | V*ps | |
| $T_{MIN-RX}$ | Minimum pulse width response | 20 | | | ns | |

## Transmitter Characteristics

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes It is therefore important that the static power consumption of a LP transmitter be as low as possible. The slew-rate of signal transitions is bounded in order to keep EMI low.

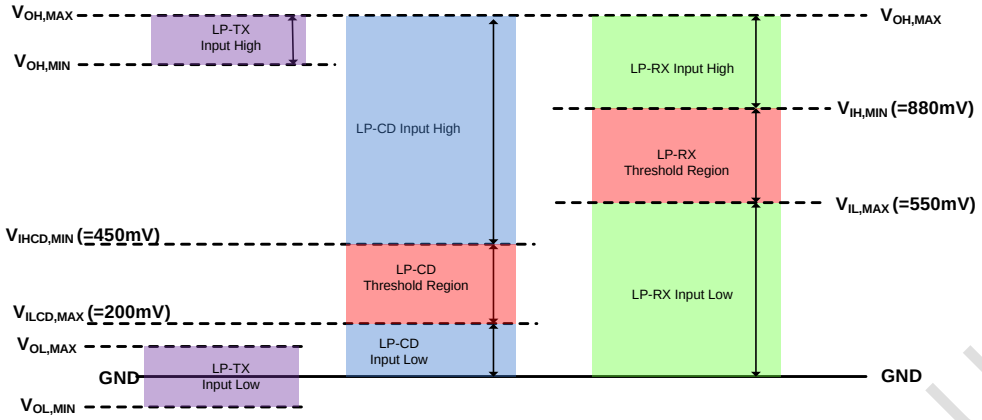
**Low-Power Transceiver Specifications**

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| **$V_{OH}$** | **Thevenin output high level** | **1.1** | **1.2** | **1.3** | **V** | |
| **$V_{OL}$** | **Thevenin output low level** | **-50** | | **50** | **mV** | |
| **$Z_{OLP}$** | **Output impedance of LP transmitter** | **110** | | | **Ω** | |

**Line Contention Detection**

The Low-Power receiver and a separate Contention Detector (LP-CD) shall be used in a bi-directional

Data Lane to monitor the line voltage on each Low-Power signal. This is required to detect line contention. The LP-CD shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than $V_{IHCD}$. An LP low fault shall not be detected when the pin voltage is less than $V_{ILCD}$. The LP-CD threshold voltages are shown along with the normal signaling voltages in the following figure.

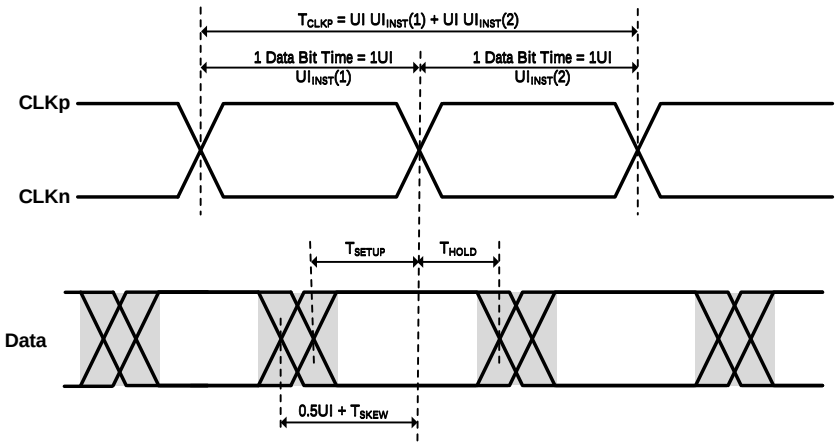



**Contention Detector (LP-CD) DC Specifications**

| Parameter | Description | Min | Nom | Max | Units | Note |
|---|---|---|---|---|---|---|
| $V_{IHCD}$ | Logic 1 contention threshold | 450 | | | mV | |
| $V_{ILCD}$ | Logic 0 contention threshold | | | 200 | mV | |

## Forward High-Speed Transmissions

Data to Clock Timing Definitions

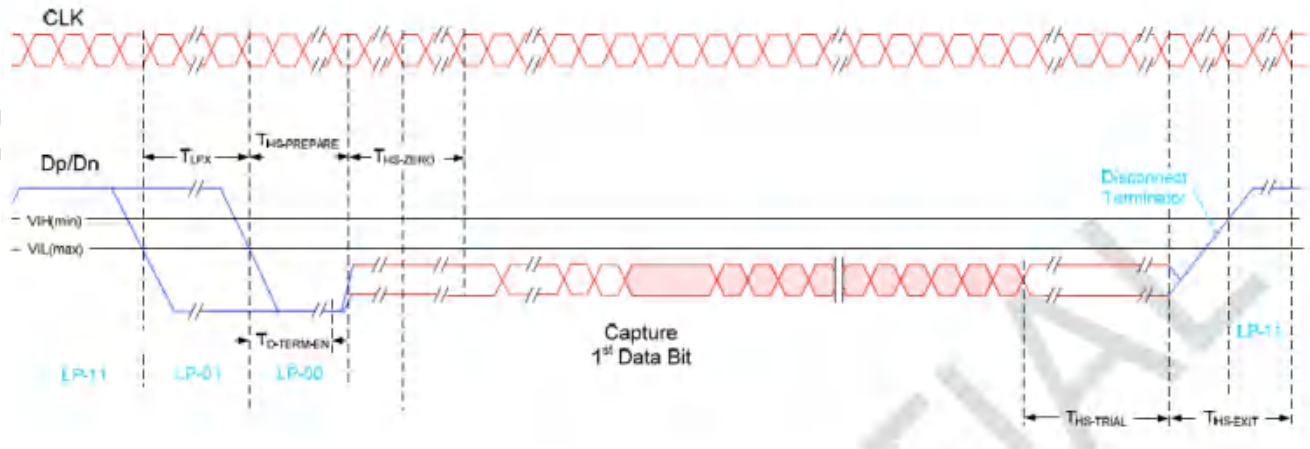



### Data-Clock Timing Specifications:

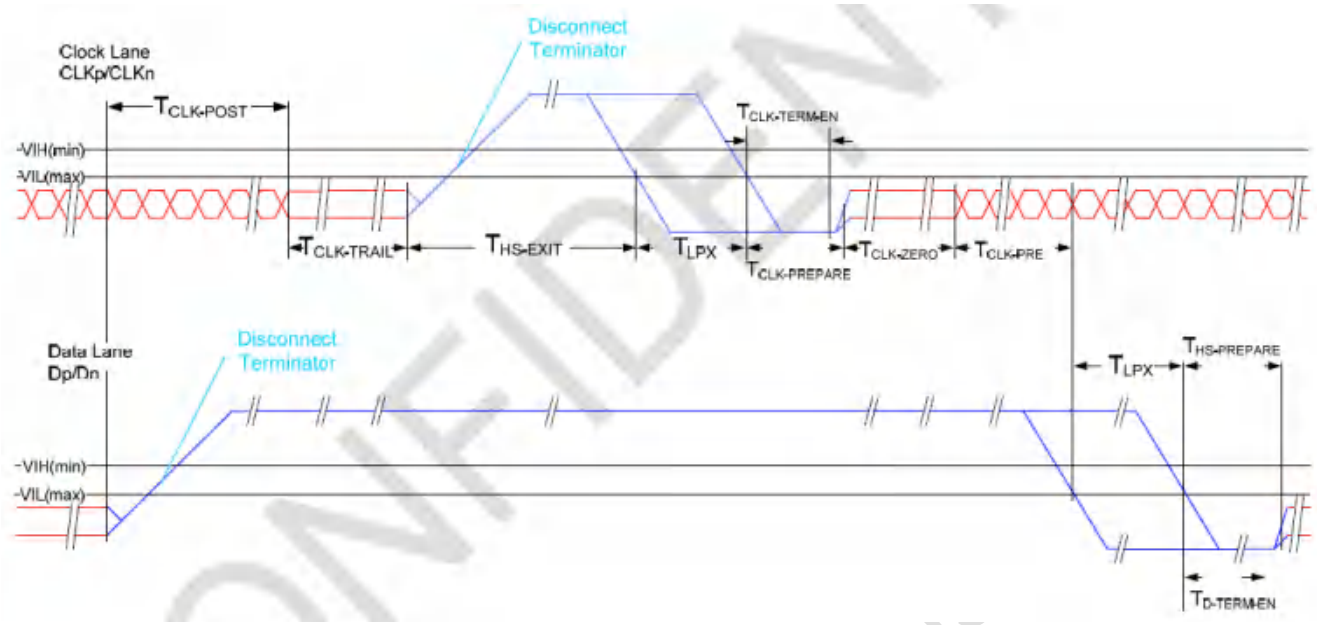
| Parameter | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| UI instantaneous | $UI_{INST}$ | 1 | | 12.5 | ns | 1,2 |
| Data-to-Clock Skew | $T_{SKEW}$ | -0.15 | | 0.15 | $UI_{INST}$ | 3 |
| Data-to-Clock Setup Time (Receiver side) | $T_{SETUP}$ | 0.15 | | | $UI_{INST}$ | 4 |
| Clock-to-Data Hold Time (Receiver side)] | $T_{HOLD}$ | 0.15 | | | $UI_{INST}$ | 4 |

**Notes:**
1. **This value corresponds to a minimum 80 Mbps data rate.**
2. **The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.**
3. **Total silicon and package delay budget of 0.3*$UI_{INST}$**
4. **Total setup and hold window for receiver of 0.3*$UI_{INST}$**

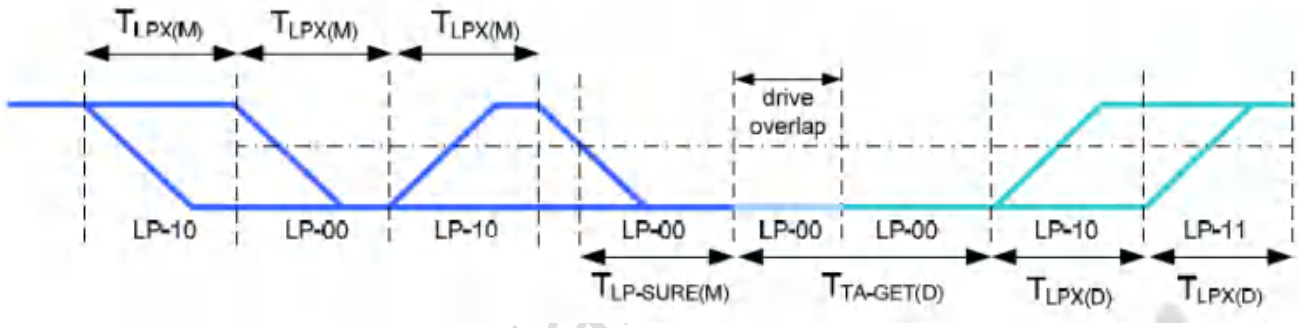
### HS Data Transmission Burst




### HS clock transmission




**Turnaround Procedure**




**Timing Parameters**

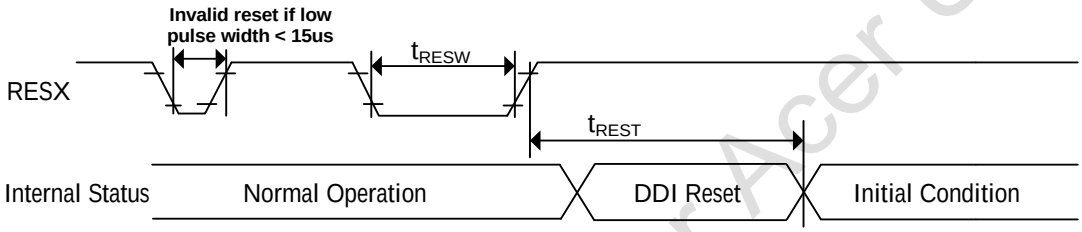
| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$ . | 60ns + 52*UI | | | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst. | 60 | | | ns |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | 300 | | | ns |
| $T_{CLK-TERM-EN}$ | Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$ . | - | | 38 | ns |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | 38 | | 95 | ns |

| | | | | | |
|---|---|---|---|---|---|
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | 8 | | | UI |
| $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock. | 300 | | | ns |
| $T_{D-TERM-EN}$ | Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$ . | - | | 35ns + 4*UI | |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission | 40 ns + 4*UI | | 85 ns + 6*UI | ns |
| $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ | $T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | 145 ns + 10*UI | | | ns |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst | 60 ns + 4*UI | | | ns |
| $T_{LPX(M)}$ | Transmitted length of any Low-Power state period of MCU to display module | 50 | | 150 | ns |
| $T_{TA-SURE(M)}$ | Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX(M)}$ | | $2*T_{LPX(M)}$ | ns |
| $T_{LPX(D)}$ | Transmitted length of any Low-Power state period of display module to MCU | 50 | | 150 | ns |
| $T_{TA-GET(D)}$ | Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround. | | $5*T_{LPX(D)}$ | | ns |
| $T_{TA-GO(D)}$ | Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround. | | $4*T_{LPX(D)}$ | | ns |
| $T_{TA-SURE(D)}$ | Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround. | $T_{LPX(D)}$ | | $2*T_{LPX(D)}$ | ns |

## 4. Display RESET Timing Characteristics

The Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode and then return to default condition for H/W reset. Spike Rejection also applies during a valid reset pulse as shown below.

During reset complete time (tREST), data in MTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX. It is necessary to wait 5msec after releasing RESX before sending commands. Also, the rising edge of RESX to Sleep Out command should be longer than120msec.




Reset timing @VDDI=1.65V to 3.6V, Ta=-40 to 85℃

| Symbol | Parameter | MIN | TYP | MAX | Unit | Note |
|---|---|---|---|---|---|---|
| $t_{RESW}$ | Reset low pulse width | 15 | - | - | μs | 1. Shorter than 5us, Reset rejected<br>2. Longer than 15μs, IC reset<br>3. Between 5μs and 15μs, It depends on voltage and temperature condition. |
| $t_{REST}$ | Reset complete time | - | - | 5 | ms | When reset applied at sleep-in mode |
| | | - | - | 120 | ms | When reset applied at sleep-out mode |

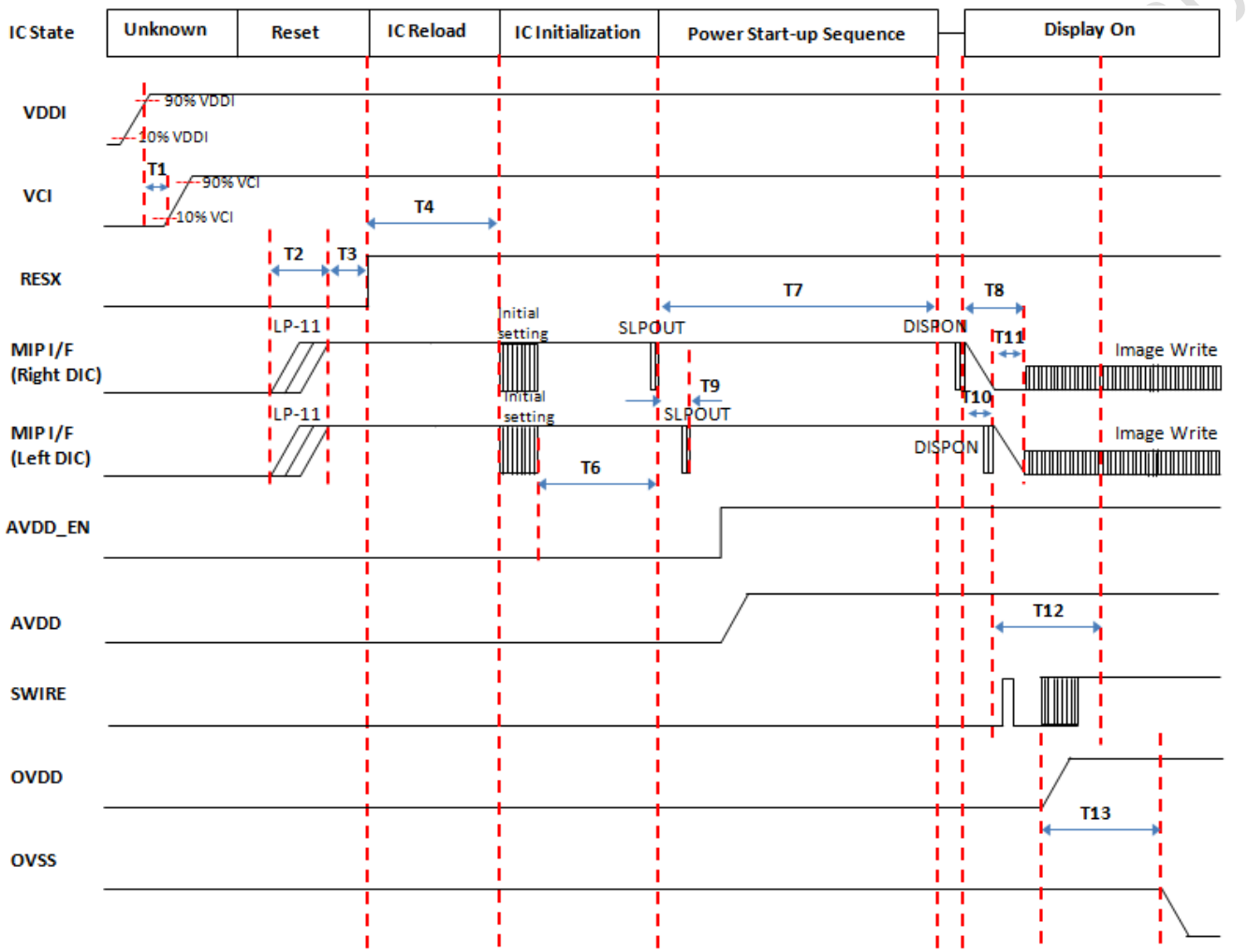
## 5. Recommended Operating Sequence

**State Diagram: Please refer to H477ULN01.2 Application Note**

### Power Structure

**Please refer to H477ULN01.2 Application Note**

### Power on sequence

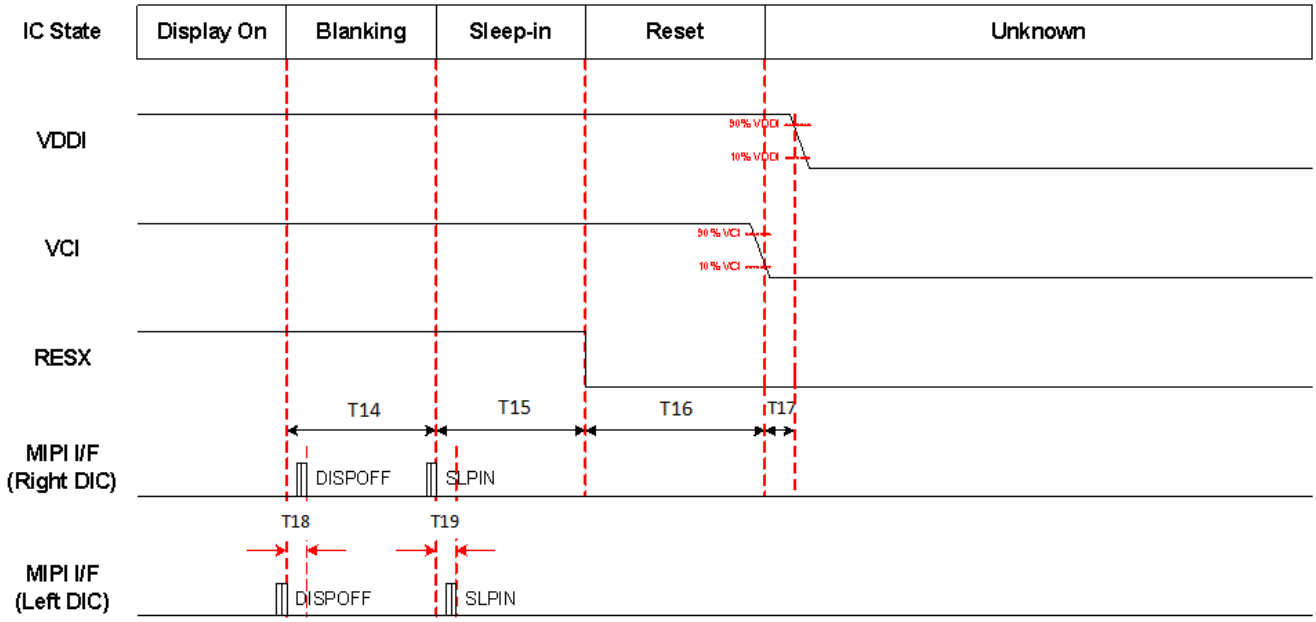



| Symbol | Value | | | Unit | Remark |
|---|---|---|---|---|---|
| | Min. | Typ. | Max | | |
| T1 | 2 | - | - | ms | |
| T2 | 1 | - | - | ms | MIPI set LP-11 |
| T3 | 1 | - | - | ms | Driver IC reset |
| T4 | 32 | - | - | ms | Reload IC setting |
| T6 | 1 | - | - | ms | |
| T7 | 96 | - | - | ms | Power start-up |
| T8 | 5 | - | - | ms | |
| T9 | 0 | - | 1 | ms | |

| | | | | | |
|---|---|---|---|---|---|
| T10 | 0 | - | 1 | ms | |
| T11 | 0 | - | 10 | clk | Unit is MIPI's byte clock |
| T12 | 2 | - | - | VS | Display-on blanking region |
| T13 | 32 | 40 | 48 | ms | Discharge time |

Note：DIC stands for "Driver IC." Right DIC is the "slave DIC," and left DIC is the "master DIC."

**Power off sequence**




| Symbol | Value | | | Unit | Remark |
|---|---|---|---|---|---|
| | Min. | Typ. | Max | | |
| T14 | 20 | - | - | ms | |
| T15 | 10 | - | - | ms | |
| T16 | 2 | - | - | ms | |
| T17 | 2 | - | - | ms | |
| T18 | 0 | - | 1 | ms | |
| T19 | 0 | - | 1 | ms | |

Note：DIC stands for "Driver IC." Right DIC is the "slave DIC," and left DIC is the "master DIC."

Please follow AUO's main FPC design suggestion.

Timing settings of Green are controlled by display driver IC. (The settings couldn't be adjusted.)

Timing settings of Red are controlled by DC/DC power IC. (The settings couldn't be adjusted.)

**Initial Setting:**

| Item | Parameter Quantity | Address | P0 |
|---|---|---|---|
| Reference H477ULN01.2 Application Note | | | |

**Sleep Out:**

| Item | Parameter Quantity | Address | P0 |
|---|---|---|---|
| Reference H477ULN01.2 Application Note | | | |

**Display On:**

| Item | Parameter Quantity | Address | P0 |
|---|---|---|---|
| Reference H477ULN01.2 Application Note | | | |

**Sleep In**

| Item | Parameter Quantity | Address | P0 |
|---|---|---|---|
| Reference H477ULN01.2 Application Note | | | |

**Display Off:**

| Item | Parameter Quantity | Address | P0 |
|---|---|---|---|
| Reference H477ULN01.2 Application Note | | | |

## D. Optical Specification

All optical specifications are measured under typical condition. (Note 1)

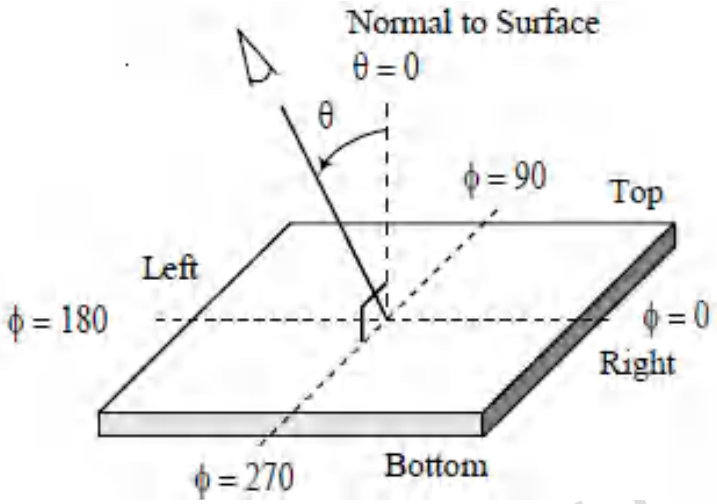
| Item | | Abbr. | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Brightness | | Y @ θ=0° | 120 | 150 | | nits | Note 2 |
| Contrast ratio | | @ θ=0° | 10000 | -- | -- | -- | |
| Viewing angle (CR > 10) | | Top | 88 | -- | -- | Deg. | |
| | | Bottom | 88 | -- | -- | Deg. | |
| | | Left | 88 | -- | -- | Deg. | |
| | | Right | 88 | -- | -- | Deg. | |
| Chromaticity (CIE1931) | Red | x | 0.640 | 0.670 | 0.700 | -- | Note 3 |
| | | y | 0.300 | 0.330 | 0.360 | -- | |
| | Green | x | 0.186 | 0.236 | 0.286 | -- | |
| | | y | 0.661 | 0.711 | 0.761 | -- | |
| | Blue | x | 0.090 | 0.130 | 0.170 | -- | |
| | | y | 0.025 | 0.065 | 0.105 | -- | |
| | White | x | 0.293 | 0.313 | 0.333 | -- | |
| | | y | 0.309 | 0.329 | 0.349 | -- | |
| Brightness Uniformity | | 9 points | 75 | -- | -- | % | Note 4 |
| Color Uniformity | | 9 points | | +/- 0.03 | | | Full White (L255) |
| NTSC | | | 95 | 100 | | % | CIE1931 |
| Flicker | | | -- | -- | -30 | dB | Note 5 |
| Crosstalk | | | -- | -- | 4.0 | % | Note 6 |
| Life Time | | 95% @ 25°C | 100 | | | hrs | Note 7 |
| Response Time | | 25°C<br>Tr : 10% to 80%;<br>Tf : 90% to 10%;<br>Tr+Tf | | | 0.8 | ms | 依據 1st sample 的實測數據討論並微調 Spec. |
| Gamma | | | 2.0 | 2.2 | 2.4 | | |
| Persistence | | | | 1.1 | | ms | Duty10% @ 90Hz |

Note 1: **Typical Condition**

Optical characteristics should be measured at the **center area** of the display with **Konica Minolta CA-310** and at the ambient temperature = **25℃±2℃** and in the dark room.

Note 2: **Viewing Angle & Contrast Ratio**

The optical performance is specified as the driver IC located at **ψ =270˚**.




Contrast ratio is calculated with the following formula:

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when OLED is at “White” pattern}}{\text{Photo detector output when OLED is at “Black” pattern}}$$

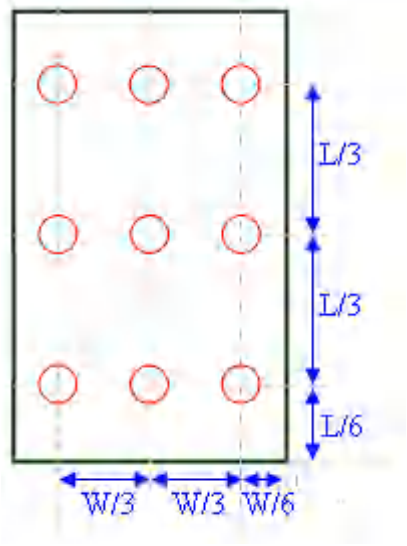
Note 3: **Chromaticity**

Chromaticity of **R, G, B** pattern are measured at Gray Level “**255**”.

Chromaticity of **White** pattern are measured at Gray Level “**255**”.

Note 4: **Uniformity**

Uniformity under **White (L255)** pattern = $\frac{\text{minimum luminance of } \mathbf{9} \text{ points}}{\text{maximum luminance of } \mathbf{9} \text{ points}}$




**Note 5: Flicker**

Suggested Instruments: **Konica Minolta CA-310**

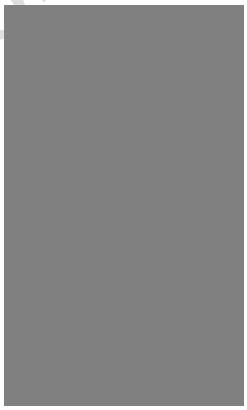
Measuring Point: **Center point of 128th gray**

The flicker level is defined using Fast Fourier Transformation (FTT) as follows:

$$Flicker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad (dB)$$

where fFFTC(n) is the nth FFT coefficient, and fFFTC(0) is the 0th FFT coefficient which is DC component. FS (Hz) is the flicker sensitivity as a function of frequency. The flicker level shall be measured with the test pattern in below.

Test Pattern: **L128 Gray**

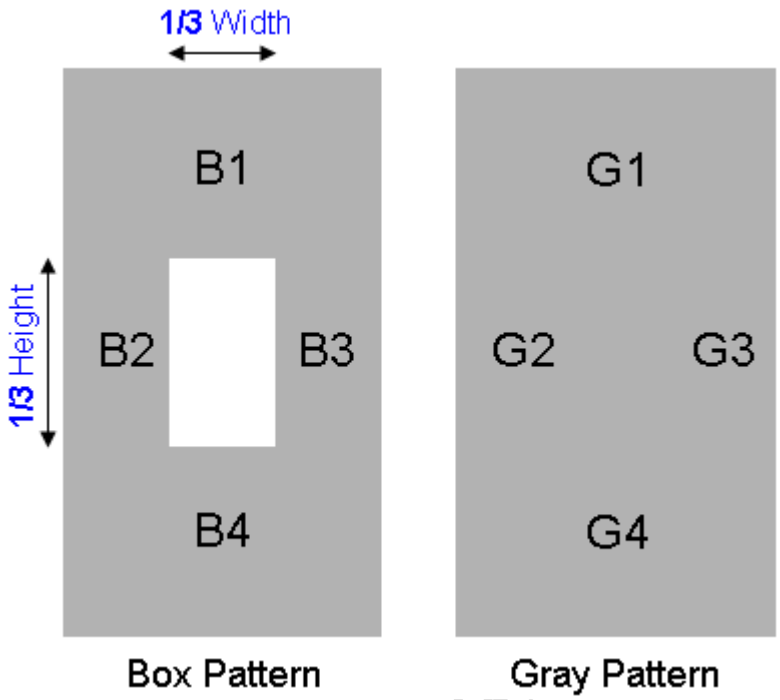


Note 6: **Crosstalk**

Crosstalk shall be calculated by the luminance of **B1~B4** and **G1~G4** in the patterns shown below.

Box Pattern: **L128** gray level background with a **L255** White window in the central area.

Gray Pattern: **L128** gray level background only.




$$Crosstalk \equiv Maximum: \left\{ \frac{|B1-G1|}{G1}, \frac{|B2-G2|}{G2}, \frac{|B3-G3|}{G3}, \frac{|B4-G4|}{G4} \right\} \times 100\%$$

Note 7: **Life Time**

OLED life time is defined by the **Minimum Duration Time** that the luminance is decayed to a specific ratio (ex. **95%**) of initial state.

Test Pattern under duration period: **L255** White

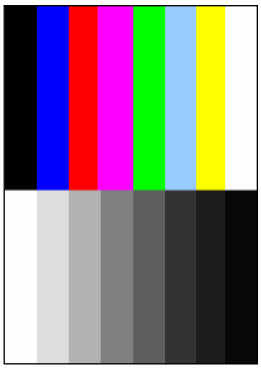
## E. Reliability Test Items

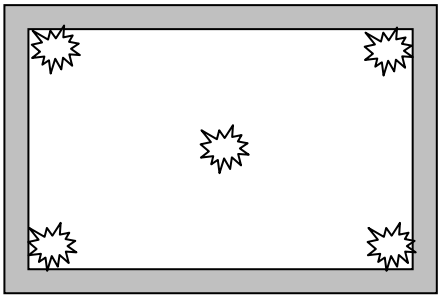
In the standard condition, there should **not** be any display function NG issue occurred during the reliability test and the performance is confirmed after panel is left at room temperature. All the cosmetic specifications are judged only **before** the reliability stress.

| No. | Test items | Conditions | | Remark |
|---|---|---|---|---|
| 1 | High Temperature Storage | T= 80℃ | 100Hrs | Note 1 |
| 2 | Low Temperature Storage | T= -40℃ | 100Hrs | |
| 3 | High Temperature Operation | T= 70℃ | 100Hrs | |
| 4 | Low Temperature Operation | T= -20℃ | 100Hrs | |
| 5 | High Temperature & Humidity Operation | T= 60℃. 90% RH | 100Hrs | |
| 6 | Thermal Shock | -30℃ ~ 80℃, 30 cycle, 1Hrs/cycle | | Non-operation |
| 7 | Electrostatic Discharge | Contact = ± 4 kV, Class B<br>Air = ± 8 kV, Class B | | Note 2 |
| 8 | Vibration (With Carton) | Non operation @ 1.5G ±X,Y,Z axis condition, 30minutes each axis<br>Frequecy 10~500Hz Random | | |
| 9 | Drop (With Carton) | Height: 76cm (ISTA standard)<br>1 corner, 3 edges, 6 surfaces | | |
| 10 | Image Sticking | 25℃, burning 12hrs, release 10min<br>CR<1% ;JND <2.6 | | |

Note 1 : T＝Ambient Temperature

Note 2: All test techniques follow IEC 61000-4-2 standard.

| Test Condition | | Note |
|---|---|---|
| **Pattern** |  | |
| **Procedure & Set-up** | Contact Discharge：330Ω, 150pF, 1sec, 5 point, 10 times/point<br>Air Discharge：330Ω, 150pF, 1sec, 5 point, 10 times/point | |

| | | |
|---|---|---|
| |  | |
| **Criteria** | Class B – Some performance degradation allowed.<br>No data lost. Self-recoverable hardware failure. | |
| **Others** | 1. Air Discharge: Gun to Panel Distance>1cm<br>2. No MiPi D-PHY command, keep default register settings. | |

## F. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module within the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period; otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Display surface never likes dirt or stains.
10. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
11. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
12. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
13. Acetic acid or chlorine compounds are not friends with TFT display module.
14. Static electricity will damage the module; please do not touch the module without any grounded device.
15. Do not disassemble and reassemble the module by self.
16. Be careful do not touch the rear side directly.
17. No strong vibration or shock. It will cause module broken.
18. Storage the modules in suitable environment with regular packing.
19. Be careful of injury from a broken display module.
20. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.

# G. Packing Information

**Packing Form**

# H. Outline Dimension

## Module Outline