PREPARED BY : DATE	SHARP	SPEC No. LD-25803B
		FILE No.
APPROVED BY : DATE		ISSUE : Oct. 11. 2013
		PAGE : 41 pages
	DISPLAY DEVICE BUSINESS GROUP SHARP CORPORATION	APPLICABLE GROUP DISPLAY DEVICE BUSINESS GROUP
	SPECIFICATION	

DEVICE SPECIFICATION FOR

TFT-LCD Module

MODEL No.

LQ101R1SX01A

☐ CUSTOMER'S APPROVAL

DATE

BY

PRESENTED

BY

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RECORDS OF REVISION

LQ101R1SX01A

SPEC No.	DATE	REVISED No.	PAGE	SUMMARY	NOTE
LD-25803A	Sep.6.2013	-	-		1st Issue
LD-25803B	Oct.11.2013	△1	22	7-2-2 Videomode Sync Event. Revise support mode	2nd Issue
			31	7-5 TE control. Description is changed Please refer to application note of LQ101R1SX01.	
			37	Revise carton size	
			39	Add High temperature & high humidity storage test	

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Table of contents

1. Application

This specification sheets applies to a color TFT-LCD module, LQ101R1SX01A.

2. Overview

This module is a color active matrix LCD module incorporating Oxide TFT (Thin Film Transistor). It is composed of a color TFT-LCD panel, driver ICs, a control circuit and power supply circuit, and a backlight unit. Graphics and texts can be displayed on a 2560×3×1600 dots panel (300 ppi) with (16,777,216) colors by using MIPI (Mobile Industry Processor Interface) DUAL DSI interface , supplying +3.3V DC supply voltage for TFT-LCD panel driving and supplying DC supply voltage for LED Backlight.. (Backlight-driving DC/DC converter is not built in this module.)

Features:

- **Wide view angle display**
- **24bit (RGB 8bit) True Color display (16,777,216 colors)**
- **Dual MIPI DSI I/F** is available: connectable directly from SoC chip.
- **Low power consumption for the whole system**: it is achieved by adopting high transparent panel, CABC Function, and by supporting MIPI Command Mode with embedded Frame Memory.
- **High picture quality**: greater color rendering properties is achieved by Color Enhancement Function.
- **Ultrathin structure**:1.88 mm thickness (at flat portion in the middle of the module)

3. Mechanical Specifications

Parameter	Specifications	Unit
Display size	25.6 (10.07") Diagonal	cm
Active area	216.96 (H)×135.6 (V)	mm
Pixel format	2560 (H)×1600 (V)	pixel
	(1 pixel = R+G+B dots)	
Pixel pitch	0.08475 (H)×0.08475 (V)	mm
Pixel configuration	R,G,B vertical stripe	
Display mode	Normally black	
Surface treatment	Clear hard coating	

Outline dimensions

Parameter		Min.	Typ.	Max.	Unit	Remark
Unit outline dimensions [Note 3-1]	Width	227.7	228.0	228.3	mm	
	Height	148.2	148.5	148.8	mm	
	Depth	1.575	1.875	2.175	mm	
		3.595	4.095	4.595	mm	PWB Portion
Mass		136	151	166	g	

[Note 3-1] Outline dimensions is shown in Fig.2

4. Input Terminals

4 - 1. Symbol

CN1 (MIPI signals, +3.3V DC power supply, and B/L power supply)

Pin No.	Symbol	Function	Remark
1	TE	Tearing Output	
2	MDIF2_3N	MIPI 2ch 3-	
3	MDIF2_3P	MIPI 2ch 3+	
4	GND	GND	
5	MDIF2_0N	MIPI 2ch 0-	
6	MDIF2_0P	MIPI 2ch 0+	
7	GND	GND	
8	MDIF2_CLKN	MIPI 2ch CLK-	
9	MDIF2_CLKP	MIPI 2ch CLK+	
10	GND	GND	
11	MDIF2_1N	MIPI 2ch 1-	
12	MDIF2_1P	MIPI 2ch 1+	
13	GND	GND	
14	MDIF2_2N	MIPI 2ch 2-	
15	MDIF2_2P	MIPI 2ch 2+	
16	GND	GND	
17	MDIF1_3N	MIPI 1ch 3-	
18	MDIF1_3P	MIPI 1ch 3+	
19	GND	GND	
20	MDIF1_0N	MIPI 1ch 0-	
21	MDIF1_0P	MIPI 1ch 0+	
22	GND	GND	
23	MDIF1_CLKN	MIPI 1ch CLK-	
24	MDIF1_CLKP	MIPI 1ch CLK+	
25	GND	GND	
26	MDIF1_1N	MIPI 1ch 1-	
27	MDIF1_1P	MIPI 1ch 1+	
28	GND	GND	
29	MDIF1_2N	MIPI 1ch 2-	
30	MDIF1_2P	MIPI 1ch 2+	
31	GND	GND	
32	LCD_VCC	LCD Power(3.3V)	
33	LCD_VCC	LCD Power(3.3V)	
34	LCD_VCC	LCD Power(3.3V)	
35	LCD_VCC	LCD Power(3.3V)	
36	NC	Not Connected	[Note4-1-1]
37	(SCL)	Not Connected	[Note4-1-1]
38	(SDA)	Not Connected	[Note4-1-1]
39	(HSYNC)	For TP sync	
40	PWMIN	System PWM （1.8V Level)	[Note4-1-2]
41	PWMOUT	PWM out for external LED DRV (1.8V Level)	[Note4-1-2]
42	LED_6	LED Cathode 6	

43	LED_5	LED Cathode 5	
44	LED_4	LED Cathode 4	
45	LED_3	LED Cathode 3	
46	LED_2	LED Cathode 2	
47	LED_1	LED Cathode 1	
48	NC	Not Connected	[Note4-1-1]
49	VLED	LED Anode	
50	VLED	LED Anode	

[Note 4-1-1] Don't input any signals or any powers into a NC pin. Keep the NC pin open.

[Note 4-1-2] If not using LCD Built-in CABC function, don't need to use these pins.

- Connector used : 20525-050E-02 (IPEX)

4 - 2. MIPI interface

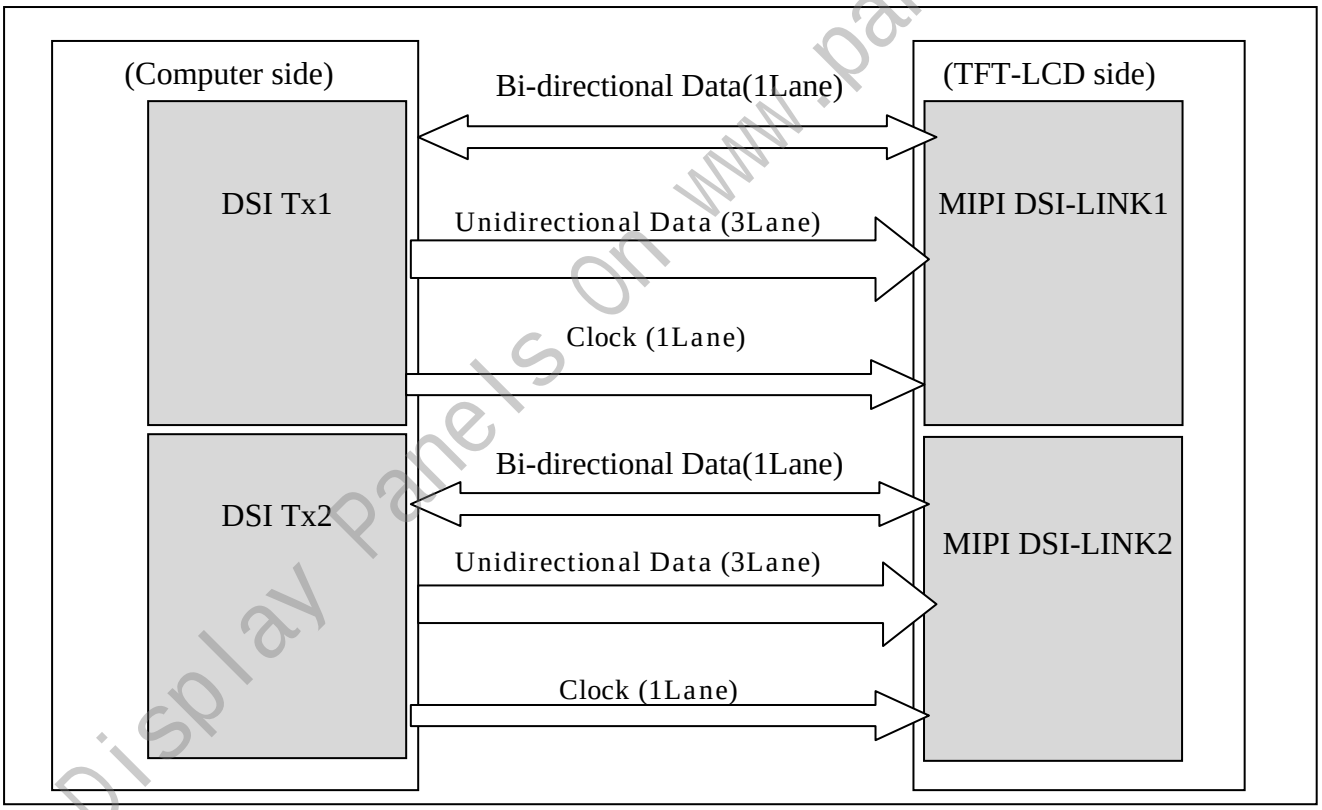


Fig.4-2-1 MIPI architecture.

4.2-1 Long packet format

Long packet consists of 16 bit packet header (PH), data payload for application (various byte number), and 32 bit packet footer (PF). Furthermore, packet header consists of 8bit data identification, 16 bit word count and 8 bit ECC. Packet footer consists of only check sum.

Long packet length is 6 – 65,541 bytes. Long packet structure is shown below.

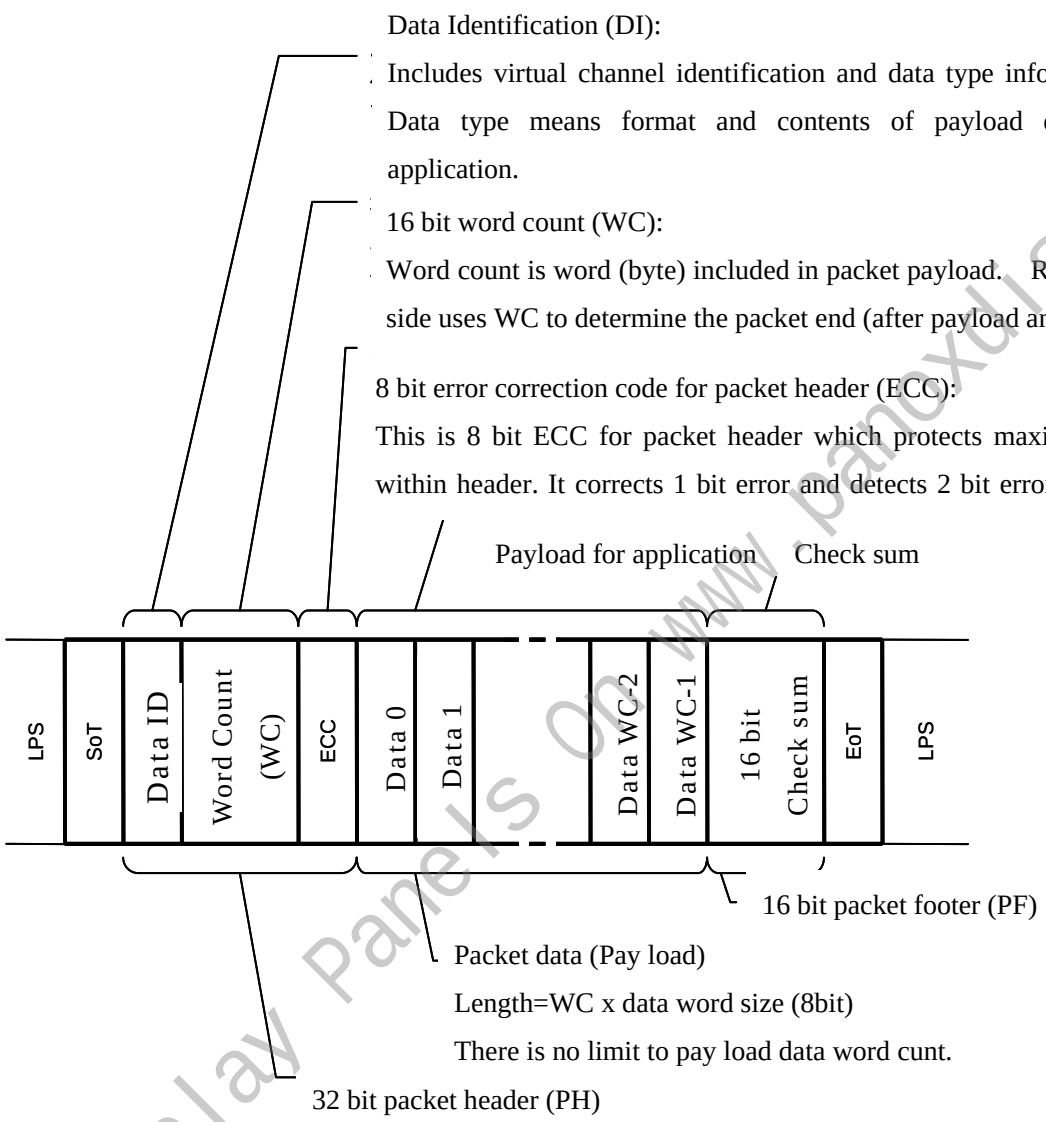


Chart 4.1 Long Packet Format

4-2-2 Short packet format

Short packet has 8 bit data ID that includes two command or data bites and 8 bit ECC.It does not have packet footer. Short packet length is 4 bytes. It corrects 1 bit error and detects 2 bit error in short packet with error correction code (ECC).

Data Identification (DI):
Includes virtual channel identification and data type information. Data type means format and contents of payload data for application.

Packet Data:
Length is 2 bytes, fixed. There is no limit to pay load data word count.

8 bit error correction code (ECC) for packet header:
8 bit ECC for packet header. It corrects 1 bit error and detects 2 bit error in packet header.

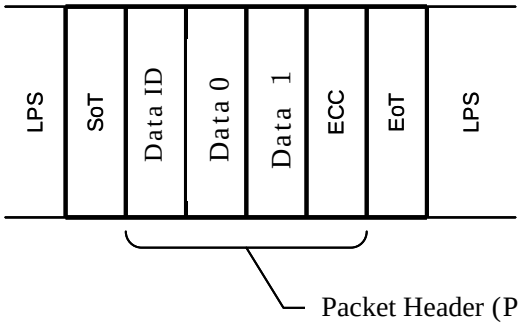


Chart 4.2 Short Packet Format

4-2-3 Data Type

Table 1.3 MIPI DSI Data Type（Host→Peripheral）

Data Type, hex	Data Type, binary	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x08	00 1000	End of Transmission packet (EoTp)	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x24	10 0100	Generic READ, 2 parameters	Short
0x05	00 0101	DCS Short WRITE, no parameters	Short
0x15	01 0101	DCS Short WRITE, 1 parameter	Short
0x06	00 0110	DCS READ, no parameters	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, no data	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
0xX0 and 0xXF, unspecified	XX 0000 XX 1111	DO NOT USE All unspecified codes are reserved	

Table 4.4 MIPI DSI Data Type（Peripheral→Host）

Data Type, hex	Data Type, binary	Description	Packet Size
0x00 – 0x01	00 000X	Reserved	Short
0x02	00 0010	Acknowledge and Error Report	Short
0x03 – 0x07	00 0011 – 00 0111	Reserved	
0x08	00 1000	End of Transmission packet (EoTp) (*1)	Short
0x09 – 0x10	00 1001 – 01 0000	Reserved	
0x11	01 0001	Generic Short READ Response, 1 byte returned	Short
0x12	01 0010	Generic Short READ Response, 2 bytes returned	Short
0x13 – 0x19	01 0011 – 01 1001	Reserved	
0x1A	01 1010	Generic Long READ Response	Long
0x1B	01 1011	Reserved	
0x1C	01 1100	DCS Long READ Response	Long
0x1D – 0x20	01 1101 – 10 0000	Reserved	
0x21	10 0001	DCS Short READ Response, 1 byte returned	Short
0x22	10 0010	DCS Short READ Response, 2 bytes returned	Short
0x23 – 0x3F	10 0011 – 11 1111	Reserved	

Note：
*1: Normally not used。

4-2-4 DCS Command

Supported DCS commands are as follow:

Table 4.5 DCS commands

Command	Hex Code	Description Code
nop	00h	No Operation
get_power_mode	0Ah	Get the current power mode.
get_pixel_format	0Ch	Get the current pixel format.
get_diagnostic_result	0Fh	Get Peripheral Self-Diagnostic Result
enter_sleep_mode	10h	Power for the display panel is off.
exit_sleep_mode	11h	Power for the display panel is on.
set_gamma_curve	26h	Selects the gamma curve used by the display device.
set_display_off	28h	Blanks the display device.
set_display_on	29h	Show the image on the display device.
set_column_address	2Ah	Set the column extent.
set_page_address	2Bh	Set the page extent.
write_memory_start	2Ch	Transfer image data from the Host Processor to the peripheral starting at the location provided by set_column_address and set_page_address.
set_tear_off	34h	Synchronization information is not sent from the display module to the host processor.
set_tear_on	35h	Synchronization information is sent from the display module to the host processor at the start of VFP.
exit_idle_mode	38h	Full color depth is used on the display panel.
enter_idle_mode	39h	Reduced color depth is used on the display panel.
set_pixel_format	3Ah	Defines how many bits per pixel are used in the interface.
write_memory_continue	3Ch	Transfer image information from the Host Processor interface to the peripheral from the last written location.

4-2-5 Error report

MIPI DSI error report is as follow:

Table 4.6 MIPI DSI error report（Peripheral→Host）

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

4-2-6 Escape entry code

MIPI DSI escape entry codes are as follow:

Table 4.7 MIPI DSI escape entry code

Entry Command Pattern (first bit transmitted to last bit transmitted) (BIN.)	**Escape Command**	**Command Type**	**Host →Peripheral**	**Peripheral →Host**
1110 0001	Low-Power Data Transmission	Mode	Supported	Supported
0001 1110	Ultra-Low Power State	Mode	Supported	–
1001 1111	Undefined-1	Mode	–	–
1101 1110	Undefined-2	Mode	–	–
0110 0010	Reset-Trigger [Remote Application]	Trigger	Supported	–
0101 1101	Tearing Effect	Trigger	–	Supported
0010 0001	Acknowledge	Trigger	–	Supported
1010 0000	Unknown-5	Trigger	–	–

5.Absolute Maximum Ratings

Parameter	Symbol	Condition	Ratings		Unit	Remark
			Min.	Max.		
+3.3V supply voltage	VDD	Ta=25℃	-0.3	+4.0	V	
LED current	If	Ta=25℃	-	35	mA	[Note 5-4]
Input voltage(MIPI)	VI	Ta=25℃	-0.3	+2.5	V	[Note 5-1]
Input voltage(BL)	VPWM	Ta=25℃	-0.3	+4.0	V	[Note 5-2]
Storage temperature (ambient)	Tstg	—	-20	+70	℃	[Note 5-3]
Operating temperature(ambient)	Topa	—	0	+60	℃	
Operating temperature (panel surface in active area)	Topp	—	0	+80	℃	

[Note 5-1] MIPI signals

[Note 5-2] Back light control signals (PWMIN)

[Note 5-3] Humidity：90%RH Max. at Ta≦+40℃.

Maximum wet-bulb temperature at +39℃ or less at Ta>+40℃.

No condensation.

[Note 5-4] In the condition of other than Ta = 25℃ , LED current must be controlled in accord with ambient temperature around the LCM.

6 Electrical Characteristics

6-1 TFT-LCD panel driving

6-1-1 DC characteristics

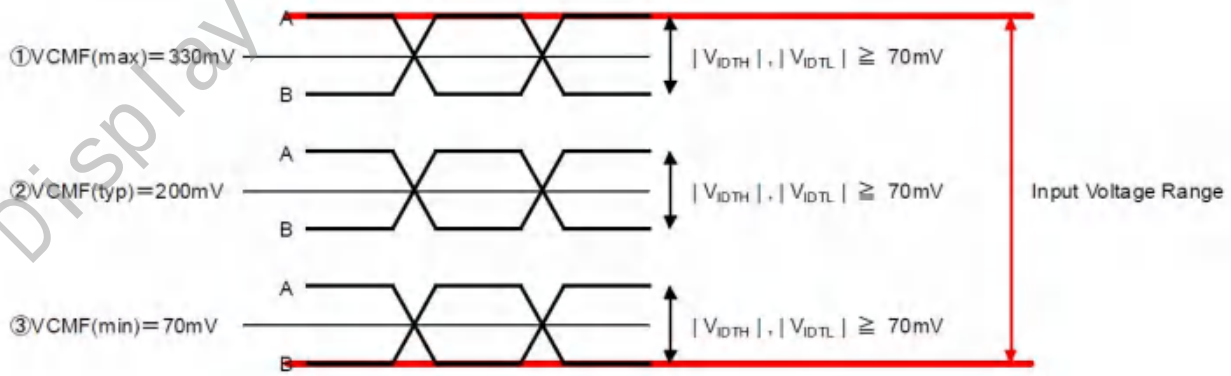
Ta＝+25℃

DC Electrical Characteristics						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply voltage	VDD	+3.0	+3.3	+3.6	V	[Note 6-1-1]
Current dissipation	IDD	—	185	370	mA	[Note 6-1-2]
Permissive input ripple voltage	V_{RP}	—	—	100	mV_{P-P}	VDD = +3.3V

6-1-2 MIPI DC characteristics

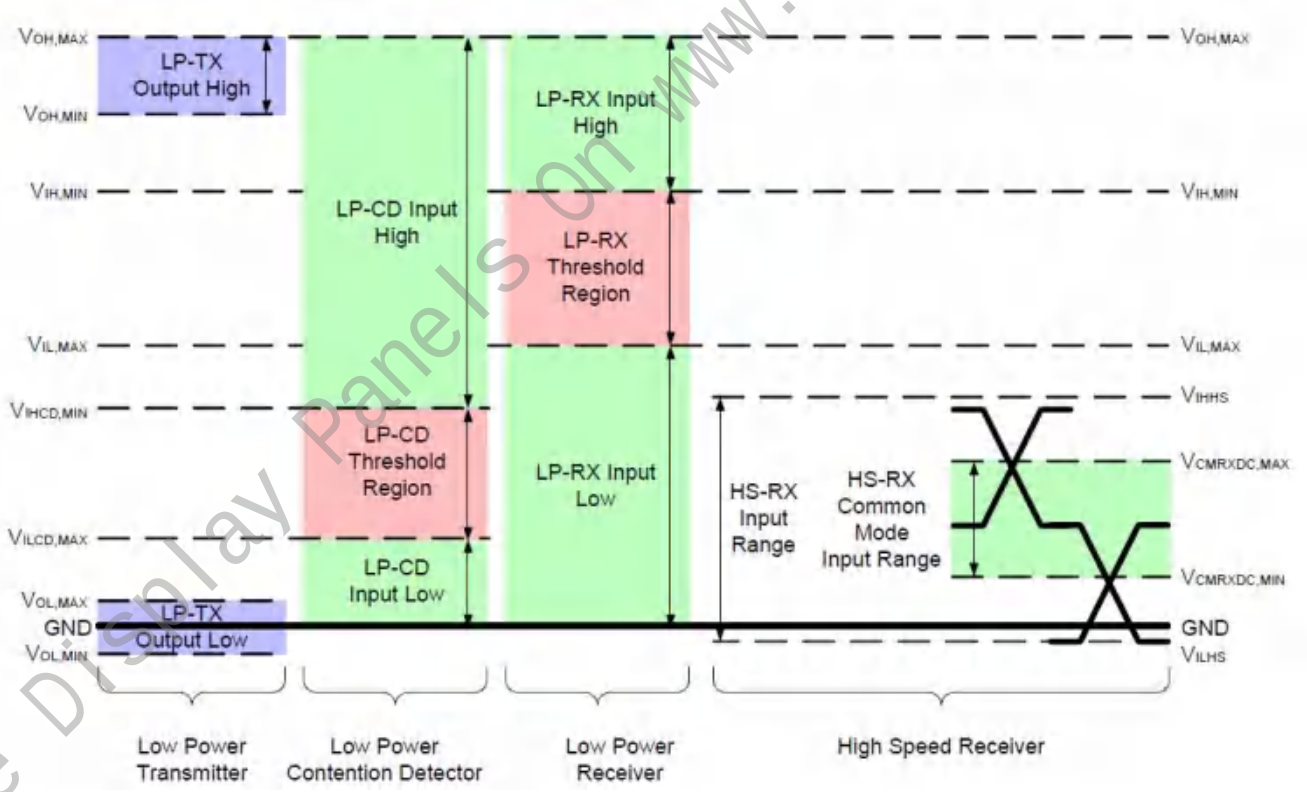
MIPI DSI HS-RX mode DC Characteristics						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Common-mode voltage HS receive mode	$V_{CMRX(DC)}$	70	-	330	mV	
Differential input high threshold	V_{IDTH}	-	-	70	mV	
Differential input low threshold	V_{IDTL}	-70	-	-	mV	
Single-ended input high voltage	V_{IHHS}	-	-	460	mV	
Single-ended input low voltage	V_{ILHS}	- 40	-	-	mV	
Differential input impedance	Z_{ID}	80	100	125	Ω	

[Note 6-1-1] ON-OFF conditions for supply voltage



MIPI DSI LP-RX mode DC Characteristics						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Logic 1 input voltage	V_{IH}	880	-	-	mV	
Logic 0 input voltage, not in ULP State	V_{IL}	-	-	550	mV	
Logic 0 input voltage, ULP State	$V_{IL-ULPS}$	-	-	300	mV	

MIPI DSI LP-CD mode DC Characteristics						
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Logic 1 contention voltage	V_{IHCD}	450	-	-	mV	
Logic 0 contention voltage	V_{ILCD}	-	-	200	mV	



6-1-3 POWER Sequence *1

Symbol	Min	Max	Unit	Note
t1	0.2	10	ms	
t2	10	50	ms	
t3	1	-.	s	

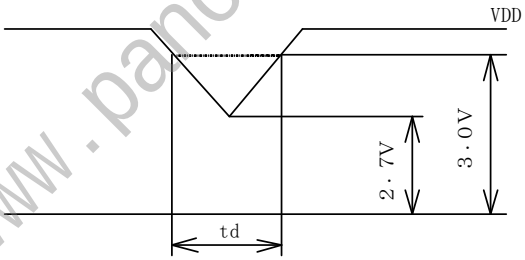
*1 Be sure to follow 6-1-3-1, 6-1-3-2 sequence when power ON/OFF.

VDD-dip conditions

1) 2.7V≦VDD＜3.0V

td≦10 ms

Under above condition, the display image should return to an appropriate figure after VDD voltage recovers.

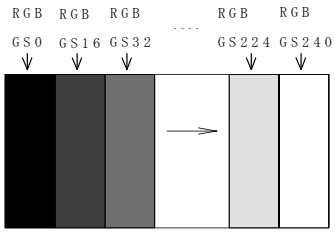


2) VDD＜2.7V

VDD-dip conditions should also follow the ON-OFF conditions for supply voltage

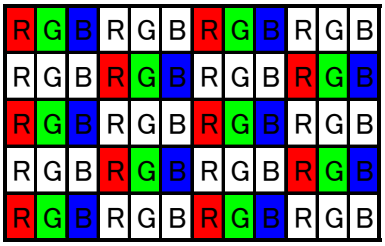
[Note 6-1-2] Typical current condition: 16-gray-bar pattern.

VDD=+3.3V

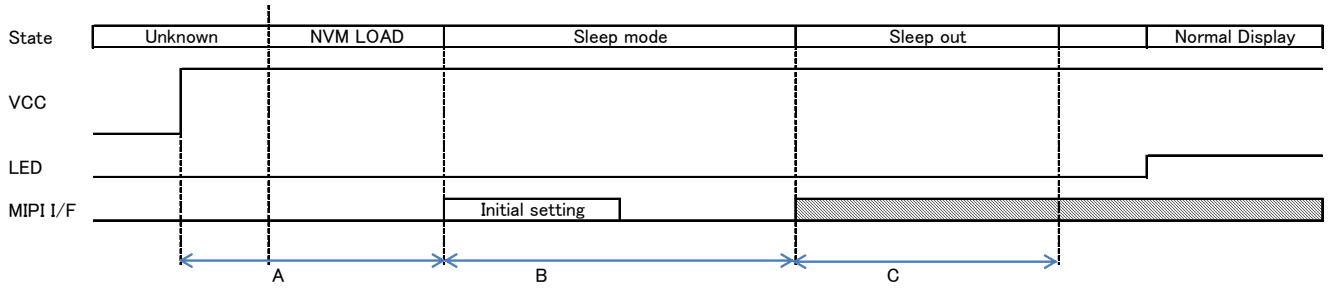


Maximum current condition: Pixel Checker pattern

VDD=+3.0V



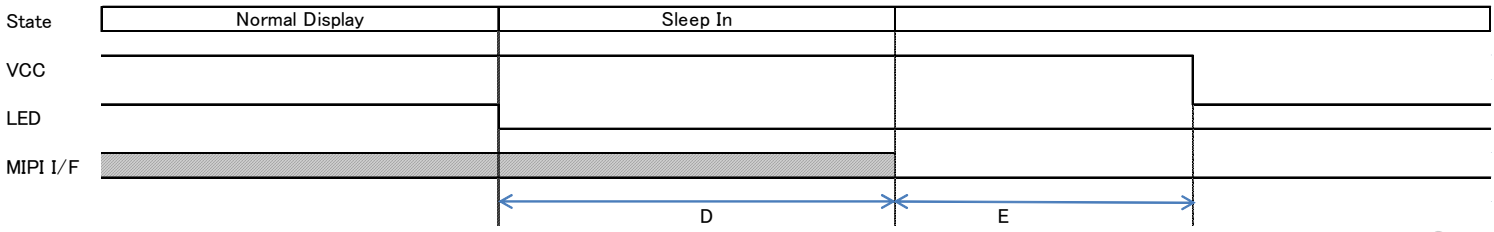
6-1-3-1 POWER ON sequence



Recommended POWER ON SEQUENCE

Step	Reg. Data	Delay	Command	term	DSI Link 1	DSI Link 2
1	Initial condition		ALL Input = L		1. DSI signals should be 0V at this point	1. DSI signals should be 0V at this point
2	Power Supply VCC (Typ 3.3V)		VCC ON (Refer power sequence)	A	2. Turn on 3.3V VCC to LCD	
3	Wait	Min. 10ms			3. Min 10ms	
4	Wait	Min. 250ms			4. Delay 250ms	
5	If customer need, please send initial command here		Link setting, mode setting, etc. Default link: Link1	B	5-1. LP-11 5-2. Send mode setting commands in LP mode (LP-11 after sending commands) ex) RAM Bypass ①0x29,0x10,0x00,0x17 (Generic Write) 0x05,0x00 (DCS SHORT NOP) wait min 3us ②0x29,0x10,0x07,0x07 (Generic Write) 0x05,0x00 (DCS SHORT NOP) wait min 3us	5-1. LP-11
6	0x11（Exit Sleep)		DCS short write no parameters		6-1. Send 0x11 DCS short write no parameters in LP mode	6-2. Send 0x11 DCS short write no parameters in LP mode
7	Wait	Min. 40ms			7. Delay 40ms min	
8	0x29(Set_Disp_On)			C	8-1. Send 0x29 DCS short write no parameters in LP mode	
9	Wait	Min.20ms			9-1 Delay 20ms min	
10	Host display data transfer		Image Write		10-1. Start refresh in Video mode(Odd)	10-1. Start refresh in Video mode(Even)
11	Wait	Min. 120 ms	Wait min. 120ms		11-1. Delay 120ms	—
12	LED On				12. Turn LED On	

6-1-3-2 POWER OFF sequence



Recomended POWER OFF SEQUENCE

Step	Reg. Data	Delay	Command	term	DSI Link 1	DSI Link 2
1	LED OFF			D	Status: Refreshing in Video mode (Odd) 1-1. Turn LED Off 1-2. Stop refresh in DC 1-3. Wait for DC to finish frame and then for DSI-A to be idle (Link1 should be in LP-11 after this step)	Status: Refreshing in Video mode (Even) 1-4. Check for DSI-B to be idle (Link2 should be in LP-11 after this step)
2	Stop Display Data Transfer		Both Link1 & Link2		2-1. Stop refresh in DC 2-2. Wait for DC to finish frame and then for DSI-A to be idle (Link1 should be in LP-11 after this step)	2-3. Check for DSI-B to be idle (Link2 should be in LP-11 after this step)
3	Wait	Min. 20ms		E	3-1 Start refresh in Video mode (Odd) 3-2. Delay 20ms	3.1. Start refresh in Video mode (Even)
4	0x28h(Set_Disp_Off)		Display off		4-1. Send 0x28 DCS short write no parameters in LP mode	
5	Wait	Min. 50ms			5. Delay 50ms	
6	0x10(Enter_Sleep)		Sleep in		6-1. Send 0x10 DCS short write no parameters in LP mode (Link1 should be in LP-11 after this step)	
7	Wait	Min. 200ms			7. Delay 200ms	
8	Final condition		ALL input = L			
9	Power Off		VCC Off		9. Turn power off	

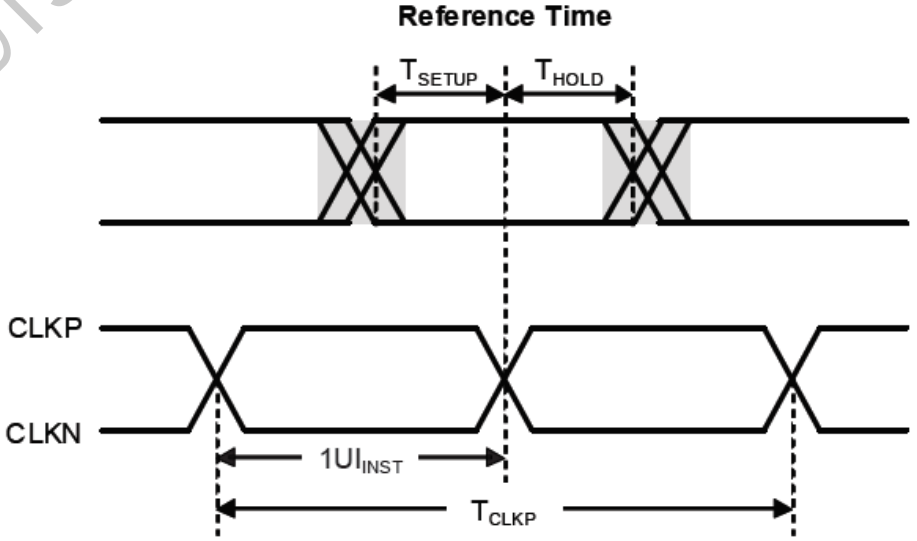
[Note 6-1-3]As for the power sequence for backlight, it is recommended to apply above mentioned input timing. If the backlight is light on and off at a timing other than shown above, displaying image may get disturbed.

[Note 6-1-4] Do not keep the interface signal high-impedance or unusual signal when power is on.

6-1-4 AC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Data to Clock Setup Time (receiver) *	$T_{SETUP[RX]}$	0.15	-	-	UI_{INST}	
Clock to Data Hold Time (receiver) *	$T_{HOLD[RX]}$	0.15	-	-	UI_{INST}	

* : Total setup and hold window for receiver of $0.3*UI_{INST}$



6-2 Backlight driving

The backlight system is an edge-lighting type with white-LED.
(It is usually required to measure under the following condition.: Ta=25℃±2℃)

Parameter	Symbol	Min.	Typ.	Max	Unit	Remark
LED voltage	Vf	18.2	21.0	23.1	V	【Note6-2-1】
LED current	If	—	20.0	21.0	mA	【Note6-2-2】
Modulated light signal voltage	$V_{PWMIN}H$	1.65	1.8	1.95	V	
	$V_{PWMIN}L$	0	—	0.1	V	
	$V_{PWMOUT}H$	1.65	1.8	1.95	V	
	$V_{PWMOUT}L$	0	—	0.1	V	
Brightness Control Duty Ratio	Duty	1	—	100	%	【Note6-2-3】
Brightness Control pulse width	T_{PWM}	30	—	—	Us	【Note6-2-4】
Brightness Control frequency	f_{PWM}	150	200	250	Hz	
Input signal pin current	I_{IN}	—	—	1.0	μA	V_{PWMIN} pin
LED lifetime	-	—	10,000	—	h	LED 【Note6-2-5】

【Note6-2-1】Per line (6 parallel) @ If = 20.0mA

【Note6-2-2】Per line of 7 LEDs connected in serial

【Note6-2-3】V_{PWM} Input : 100%= Max luminance 1%= Min luminance

【Note6-2-4】The minimum value of the dimming signal pulse width is assumed regulations of the width of high and the width of low.

【Note6-2-5】LED luminance becomes 50% of an initial value. (Ta＝25℃, DUTY=100%)

7 Timing Characteristics of Input Signals

7-1 Command Mode: Pixel Data Send Sequence

Pixel data transfer sequence with write_memory_start command and write_memory_continue command in command mode. Data alignment changes accordingly to set_pixel_format command setting.

7-1-1 When setting RGB888（set_pixel_format command：07h）

Set 07h with set_pixel_format command before sending write_memory_start command and write_memory_continuecommand. After setting, you can write pixel data to frame memory in below sequence. Make sure to writeto frame memory in 2 pixel unit.

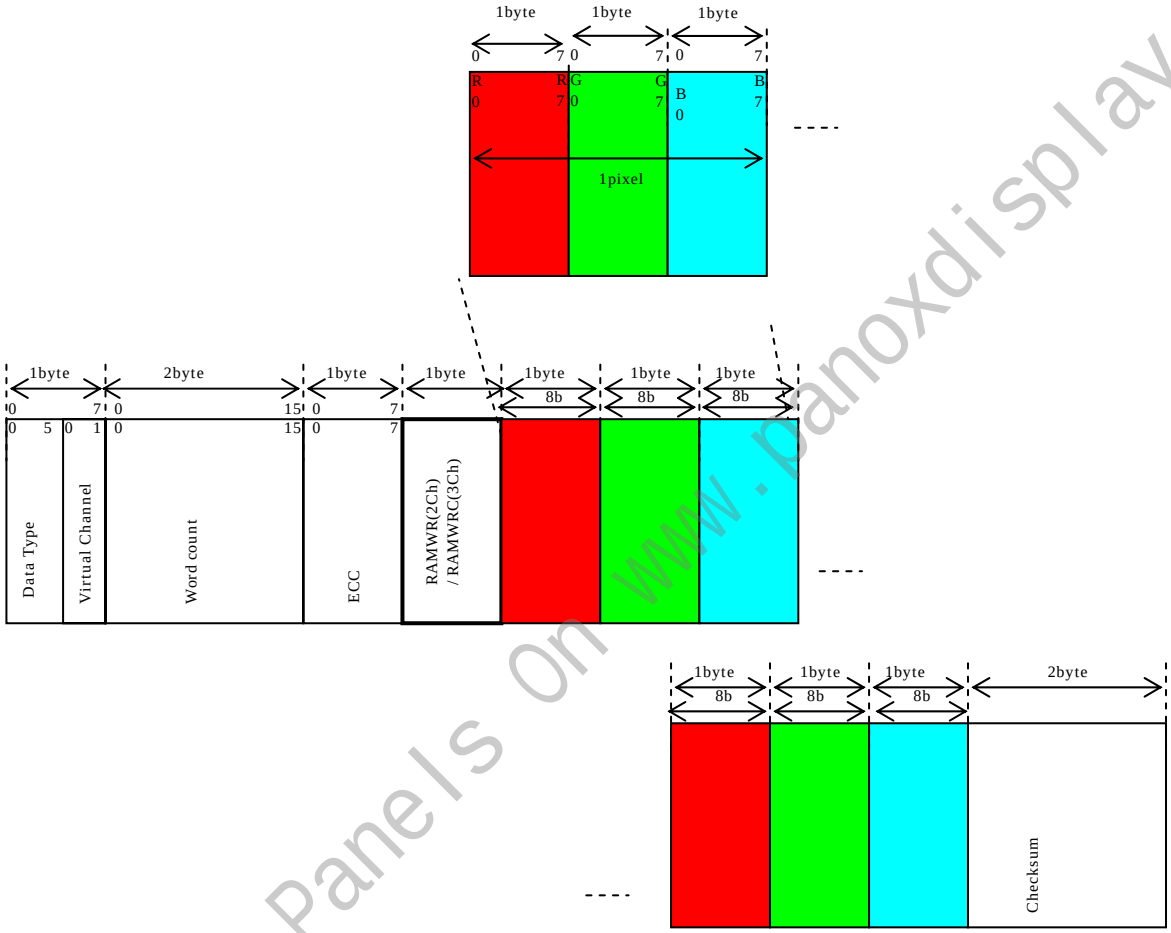


Chart 7.1 Command Mode: RGB888 setting

7-2 Video Mode: Pixel data send sequence

In video mode, pixel data transfer sequence with video stream packet (data type: 0Eh, 1Eh, 3Eh) is as follow. Data alignment can be changed with set_pixel_format command setting.

7-2-1 When setting RGB888（set_pixel_format command：07h）

Set 07h with set_pixel_format command before sending the video stream packet (data type: 3Eh).
After setting, pixel data can be written to the frame memory in below sequence.
Make sure to write to the frame memory in 2pixel unit.

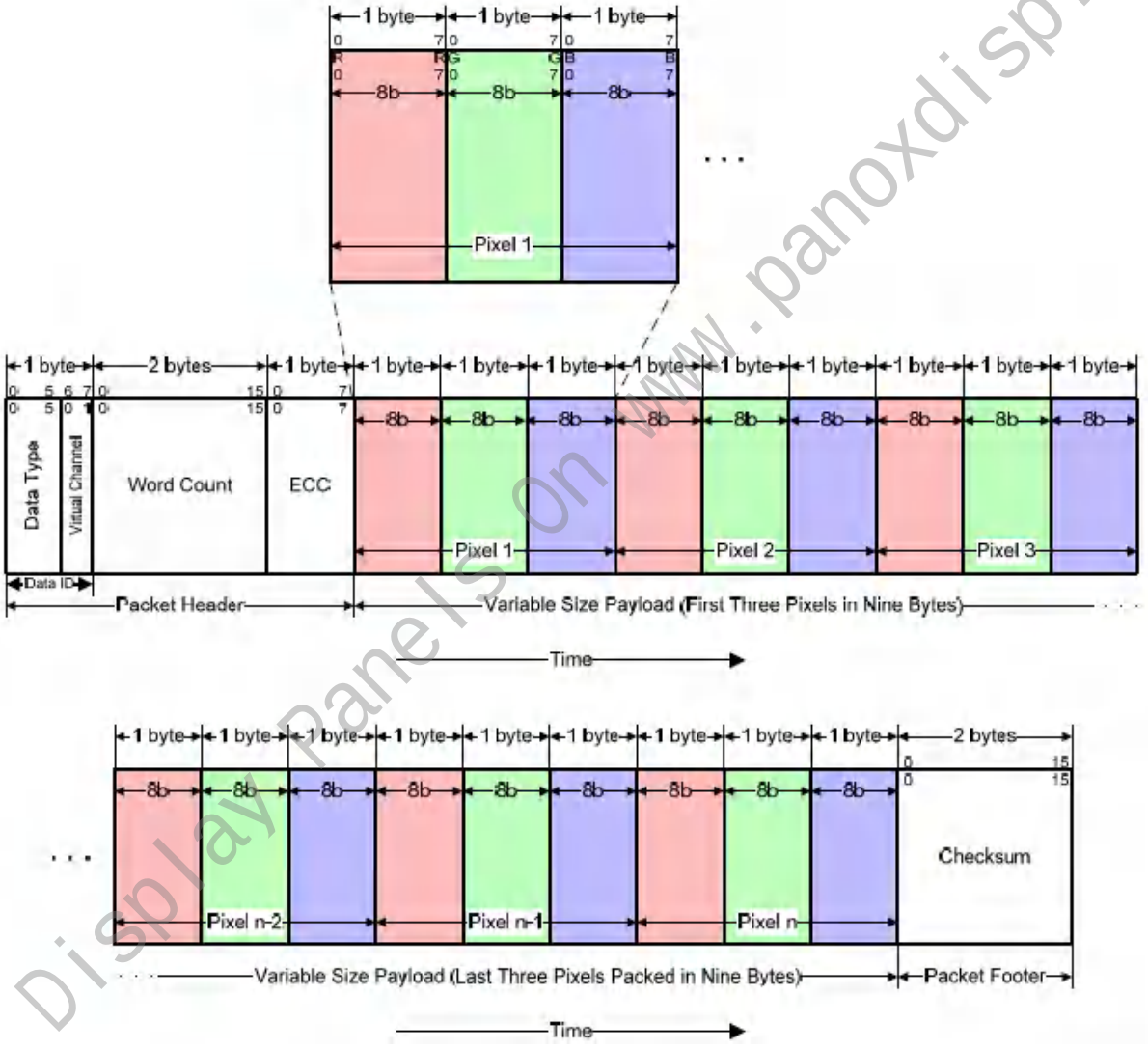


Chart7.2 video mode: RGB888 setting

7-2-2 Videomode Sync Event

Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Event mode(H Start, V Start) can use in video mode. △1

H End and V End cannot support. △1

V sync Evemt

- Need to transmit LP State after V Sync Even(HS Transmission)
- When V sync Event(LPTD) no restriction.

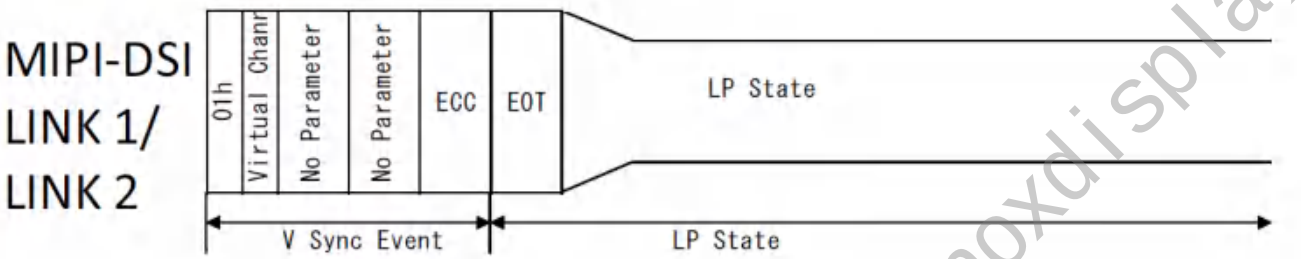


Chart 7.3 Vsync event(HS Transmission)

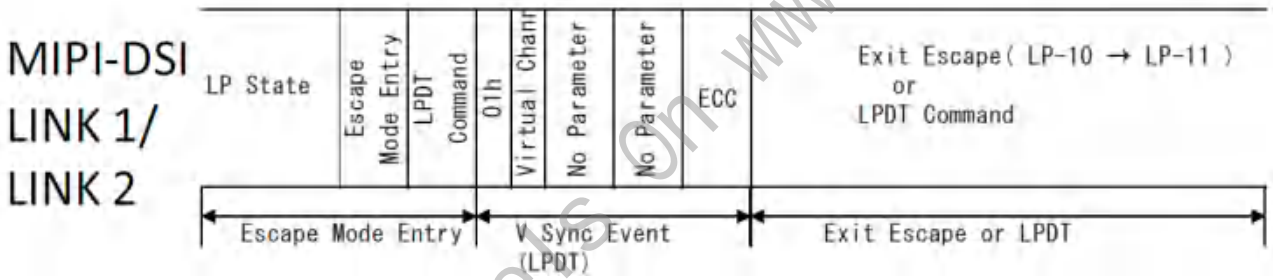


Chart 7.4 Vsync event(LPDT)

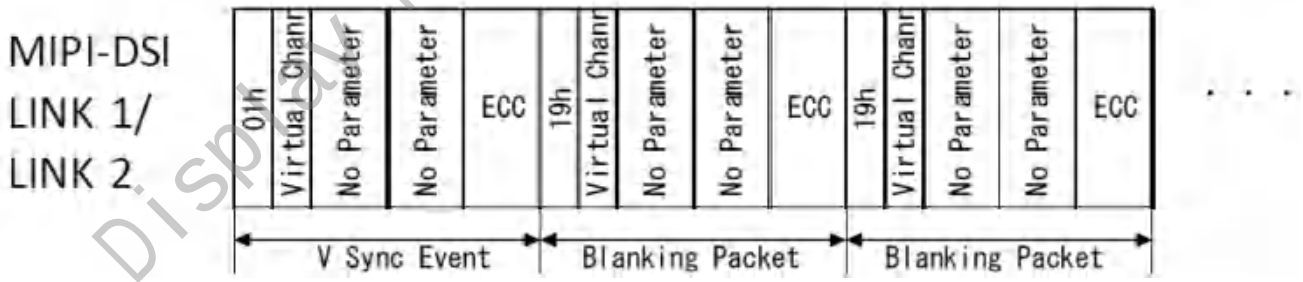


Chart 7.5 Prohibit Blanking Packet under Vsync event

After V Sync Event(V Start), Blanking Packet have to insert after LP State. △1

H Sync Event(H Start), Blanking Packet Insert timing is no limit. △1

7-3 dual link setting

There are four windows access modes available when using dual link.
Video Mode (Odd-Even division)
Video Mode (Left-Right division)
Command Mode (Odd-Even division)
Command Mode (Left-Right division)

How to use each mode is shown from next page.

7-3-1 Video Mode (Odd-Even division)

In Video Mode, Even pixels (column 0, 2, 4) data is sent via DSI-LINK 1 and Odd pixels (column 1, 3, 5) data via DSI-LINK2. There is no limitation to DSI lane Clock phase. When transfering Pixel data, each LINK's Vsync Skew/Hsync Skew should be within half of horizontal line.

Vsync/Hsync signals of either LINK 1 or 2 can be selected.

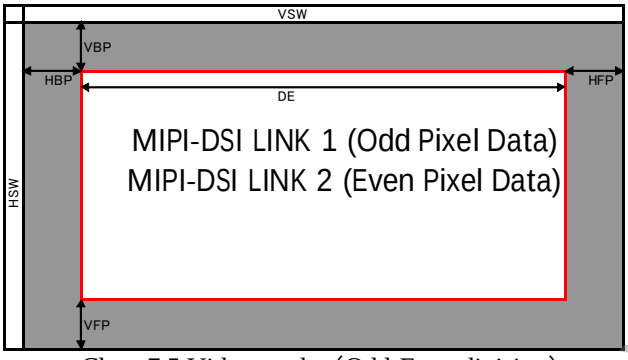


Chart 7.5 Video mode（Odd-Even division）

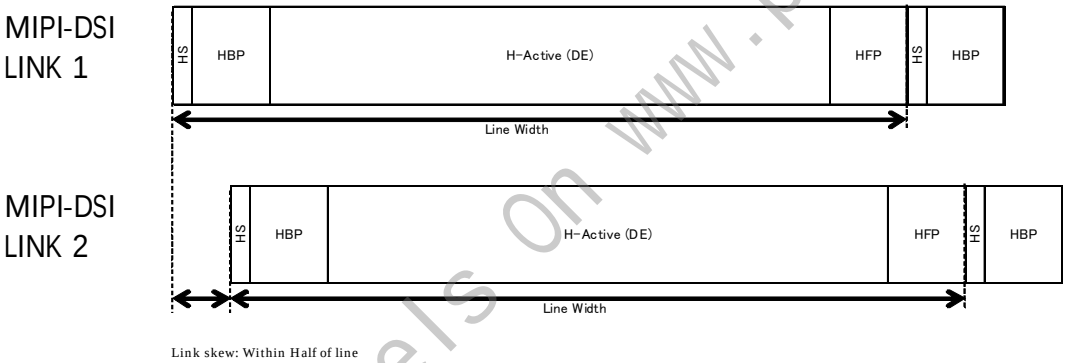


Chart 7.6 Video Mode（Odd-Even division）

Function	Abbreviation	VALUE
Horizontal dot	HADR	2560
HSYNC	HS	32
Horizontal BP	HBP	80
Horizontal FP	HFP	48
Vertical line	VADR	1600
VSYNC	VS	6
Vertical BP	VBP	37
Vertical FP	VFP	3
Frame rate		60

Table 7.1 Image format specification △1

7-3-2 Video Mode（Left-Right Division）

In Video Mode, Left pixel data is sent via DSI-LINK 1 and Right pixel is sent via DSI-LINK2. There is no limitation to DSI lane Clock phase. When transferring Pixel data, each LINK's Link Skew should be within 1 Horizontal Line. Vsync/Hsync signals of either LINK 1 or 2 can be selected by MIPI_IF_SEL (10h01h).

MIPI_IF_SEL =2'h0：Vsync/Hsync is Link1.

MIPI_IF_SEL =2'h1：Vsync/Hsync is Link2.

Left Pixel data area and Right Pixel data area can be overlapped.

If overlap exist, Overlap pixel number "X" can be set by HOVERLAP(10h32h)

Overlap maximum pixel number is 16 pixel.

Overlap pixel number "X" have to be same number for Left pixel and Right pixel.

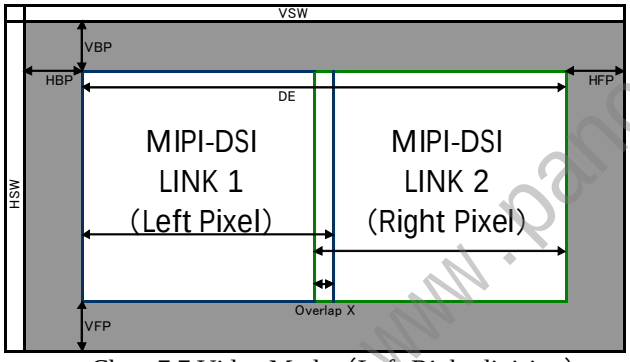


Chart 7.7 Video Mode（Left-Right division）

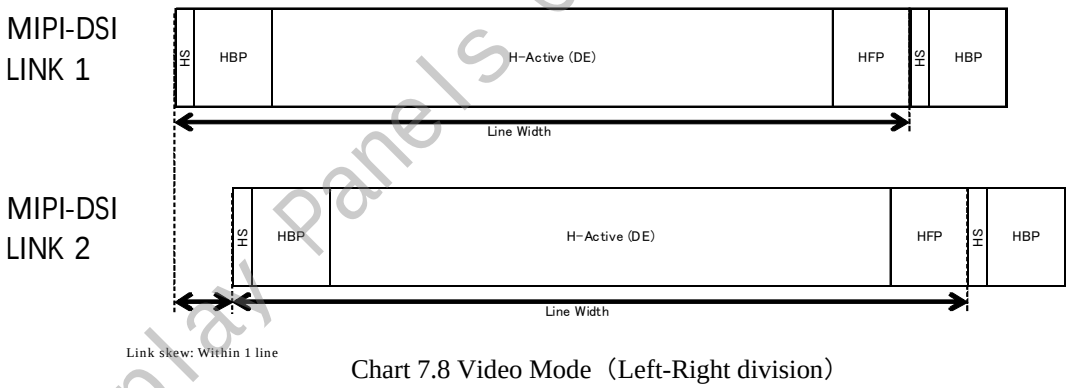


Chart 7.8 Video Mode（Left-Right division）

Function	Abbreviation	MAX	STEP
Horizontal Dot	HADR	2560	
Vertical Line	VADR	1600	
Overlap X		0-16	1
Frame Rate		60	

Table 7.2 Image Format Specification

7-3-3 Command Mode（Odd-Even Division）

In Command Mode, Even pixels (column 0, 2, 4) data is sent by DSI-LINK 1 and Odd pixels (column 1, 3, 5) data by DSI-LINK2. There is no limitation to DSI lane Clock phase. When transfering Pixel data, each LINK's Link Skew should be within half of Horizontal Line. When issue the Write Memory Start commands, 2page address (2Line) or above time need to wait after last page transfer before issuing Write Memory Start commands.

Pixel data being transferred can select one of the addresses below set by DSI-LINK 1 or DSI-LINK 2.

1)DEC_SEL(00h1Fh)=2'h0

SC1/EC1 and SP1/EP1: Set with set_column_address/set_page_address command from DSI-LINK 1.

2)DEC_SEL(00h1Fh)=2'h1

SC2/EC2 and SP2/EP2: Set with set_column_address/set_page_address command from DSI-LINK 2.

3)DEC_SEL(00h1Fh)=2'h2

Follow 00h0Ch-00h1Bh

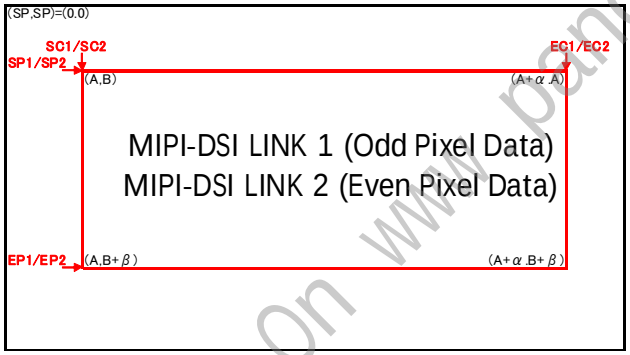


Chart 7.9 Command Mode（Odd-Even Division）

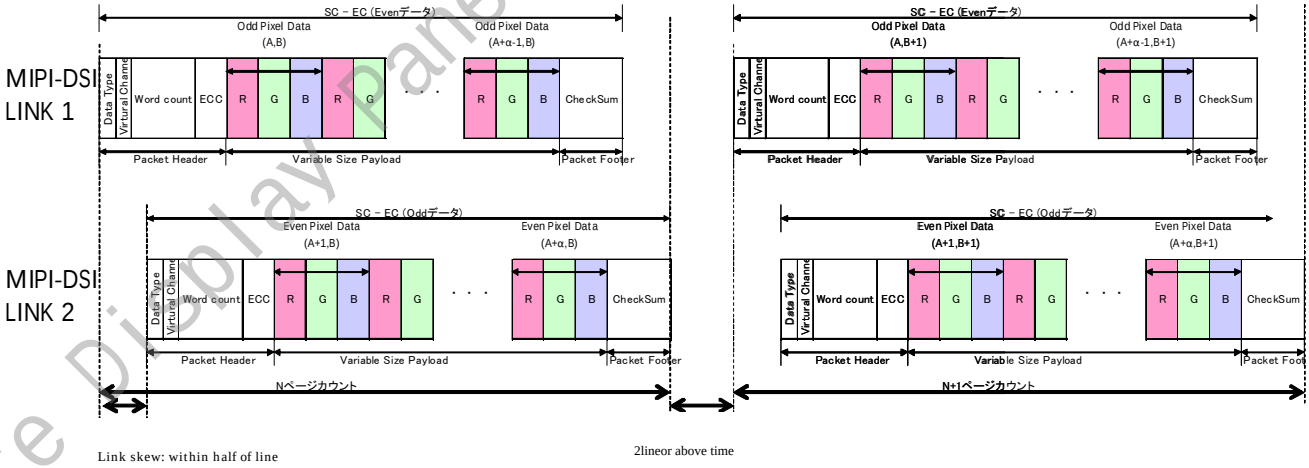


Chart7.10 Command Mode（Odd-Even division）

Function	Abbreviation	Value	STEP
Horizontal Dot	HADR	2560	64
Vertical Line	VADR	1600	1
Start Colomn	SC	0	64
End Colomn	EC	2559	64
Start Page	SP	0	1
End Page	EP	1599	1
Colomn Width	EC-SC	2560	64
Page Width	EP-SP	1600	1
Frame Rate		60	

Table7.3 Image Format Specification

7-3-4 Command Mode（Left-Right Division）

In Command Mode, each LINK operates independently. There is no limitation to DSI lane Clock phase. When transfering Pixel data, there is no limitation to Link Skew between LINKs. Write Memory Start/WriteMemory Continue commands can be sent separately. Pixel data is transferred accordingly to the following address setting.

1)DEC_SEL(00h1Fh)=2'h0 or 2'h1

・SC1/EC1 and SP1/EP1: Set with set_column_address/set_page_address command from DSI-LINK 1.

・SC2/EC2 and SP2/EP2: Set with set_column_address/set_page_address command from DSI-LINK 2.

2)DEC_SEL(00h1Fh)=2'h2

Follow 00h0Ch-00h1Bh

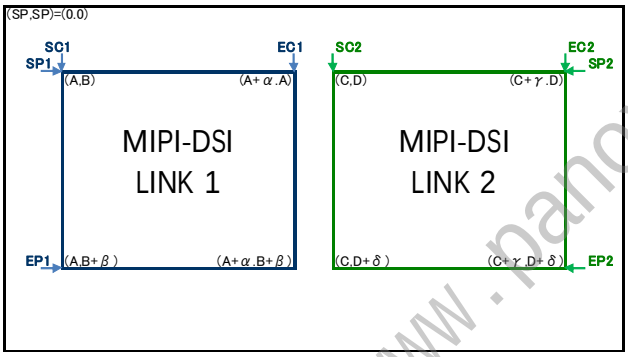


Chart 7.11 Command Mode (Left-Right Division）

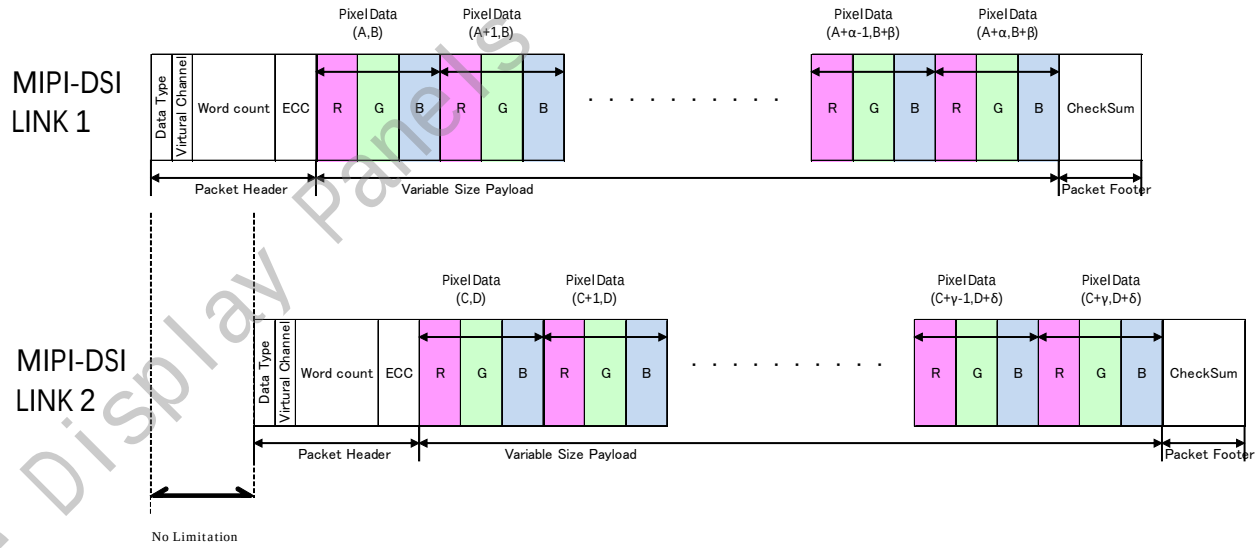


Chart7.12 Command Mode（Left-Right Division）

Function	Abbreviation	Value	STEP
Horizontal Dot	HADR	2560	128
Vertical Line	VADR	1600	1
Start Colomn 1	SC1	0	64
End Colomn 1	EC1	1279	64
Start Page 1	SP1	0	1
End Page 1	EP1	1599	1
Colomn Width 1	EC1-SC1	1280	64
Page Width 1	EP1-SP1	1600	1
Start Colomn 2	SC2	0	64
End Colomn 2	EC2	1279	64
Start Page 2	SP2	0	1
End Page 2	EP2	1599	1
Colomn Width 2	EC2-SC2	1280	64
Page Width 2	EP2-SP2	1600	1
Frame Rate		60	

Table7.4 Image Format Specification

7-4 Register Access

7-4-1 Register Write Access

Use Generic Long write (29h) for accessing Register Write from MIPI_IF. It can be accessed exclusively from LINK1 or LINK2, however, simultaneous access is prohibited.

Data Payload 1st byte is upper address, 2nd byte is lower address, 3rd byte and thereafter are Write Data, and I-64 data can be transferred.

After Write Data is transferred, Register data transfer completes with NOP command transfer.

After data transfer is complete, no Generic command can be sent to LINK1 or LINK2 for 3us (OSC_CLK*80clk). (DCS command and VIDEO data can still be sent.

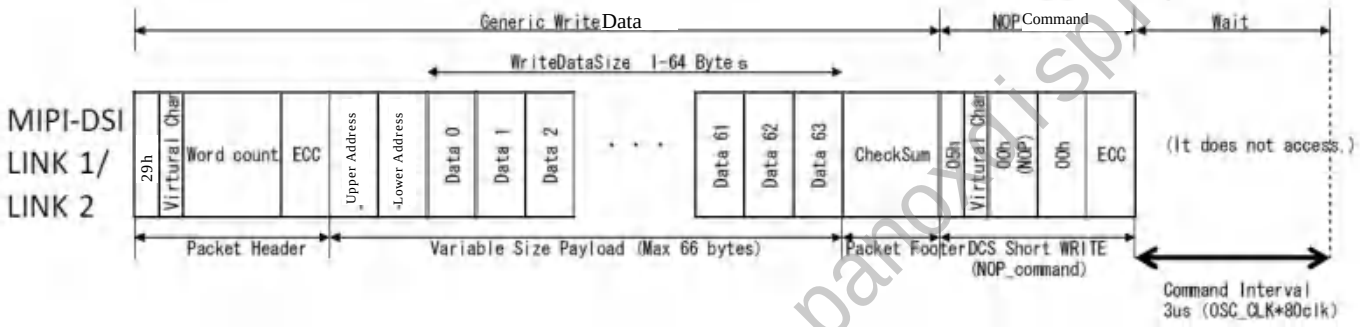


Chart7.13 Register Write Access

7-4-2 Register Read Access

Register Read can be accessed from MIPI-IF with Generic READ and 2 parameter (24h) command.

It can be accessed exclusively from LINK1 or LINK2. Simultaneous access is prohibited.

PACKETHEADER(PH)'s Data0 is upper address and Data1 is lower address. After command is issued, BusTurnAround (BTA) returns ReadData bytes set in Set Maximum Return Packet Size (24h).

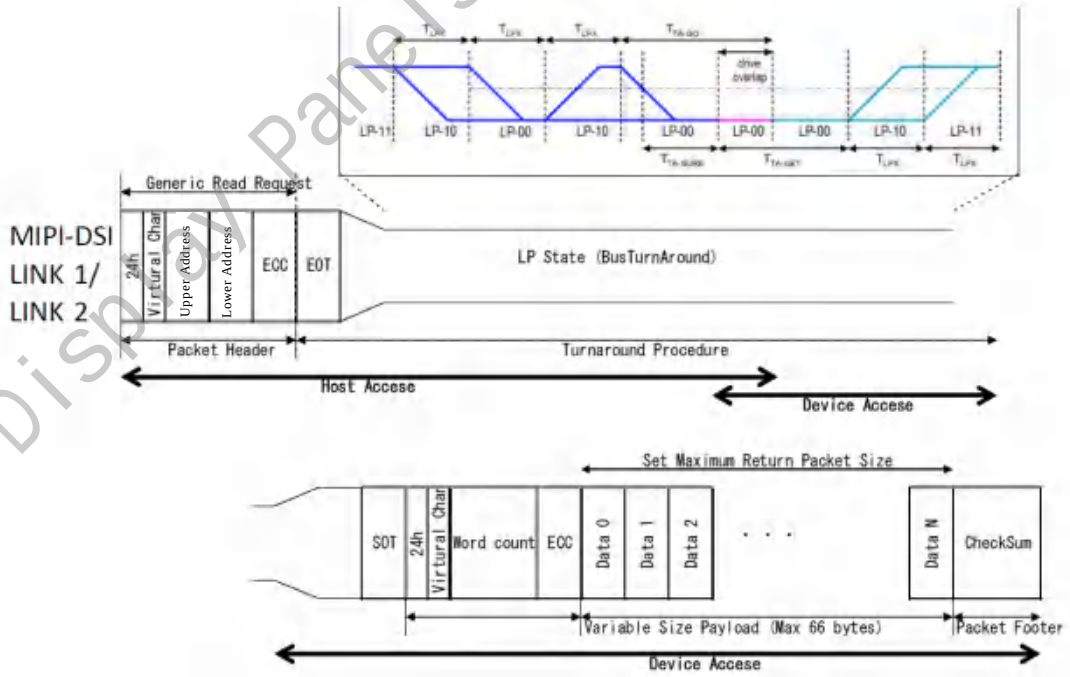
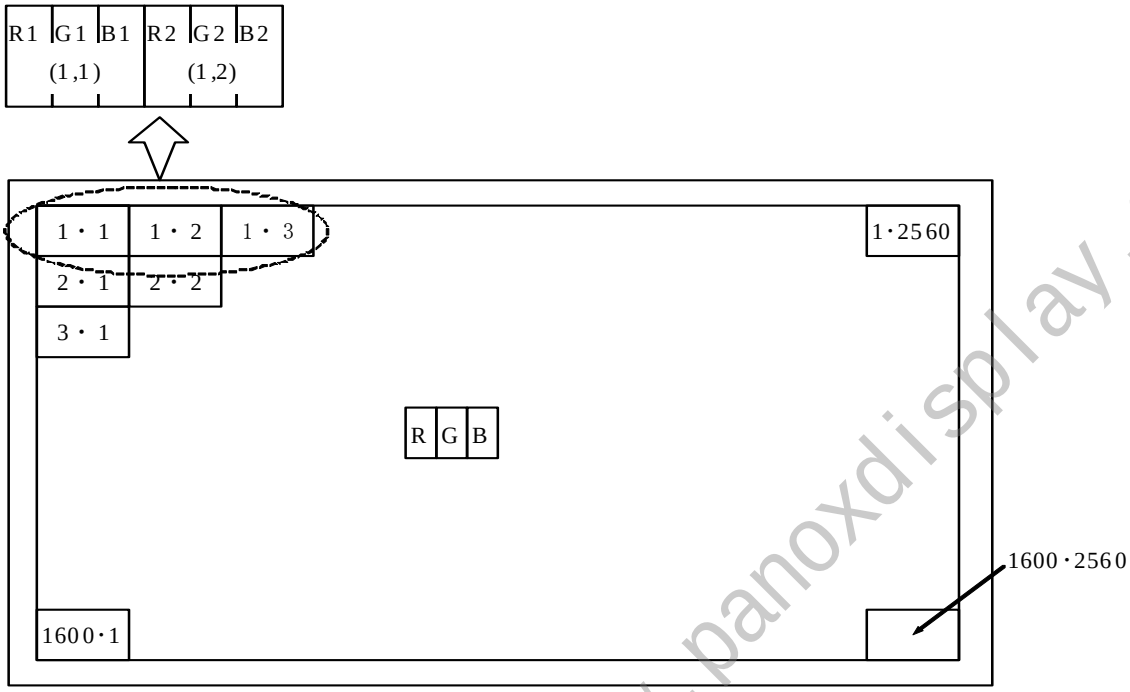


Chart7.13 Register Read Access

7-5 TE Control

Please refer to application note of LQ101R1SX01A. △1

7-6 Input data signals and display position on the screen



Display position of input data(V・H)

8 Input Signals, Basic Display Colors and Gray Scale of Each Color

	Colors & Gray Scale	Gray Scale	Date signal																							
			R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
			LSB							MSB	LSB							MSB	LSB							MSB
Basic Color	Black	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	–	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	–	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	–	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	–	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	–	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓							↓								↓				
	⇩	↓					↓							↓								↓				
	Brighter	GS253	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS254	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓							↓								↓				
	⇩	↓					↓							↓								↓				
	Brighter	GS253	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	⇩	GS254	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	GS255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	⇧	↓					↓							↓								↓				
	⇩	↓					↓							↓								↓				
	Brighter	GS253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	⇩	GS254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	GS255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

0 : Low level voltage, 1 : High level voltage

Each basic color can be displayed in 256 gray scales from 8 bit data signals.

According to the combination of 24 bit data signals, the 16.7M color display can be achieved on the screen.

9 Optical Characteristics

Ta=+25℃, VDD=+3.3V

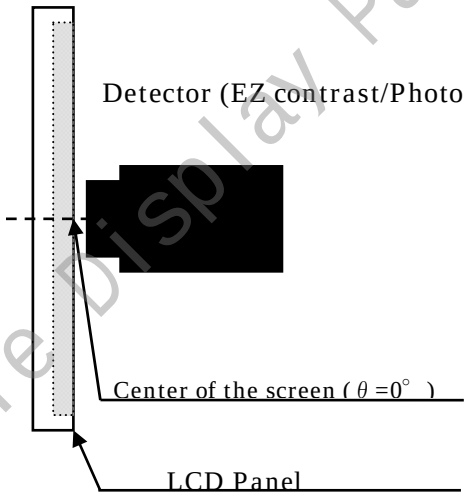
Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Horizontal	θ 21, θ 22	CR>10	80	—	—	deg.	[Note 9-1, 9-3, 9-4, 9-6]
	Vertical	θ 11		80	—	—	deg.	
		θ 12		80	—	—	deg	
Contrast ratio		CR	θ =0°	700	900	—		[Note 9-2, 9-4, 9-6]
Response time		τ r+ τ d	θ =0°	—	25	—	ms	[Note 9-2, 9-5, 9-6]
Chromaticity of white		x		0.283	0.313	0.343		[Note 9-2, 9-6] Normal operation (PWM Duty=100%)
		y		0.299	0.329	0.359		
Chromaticity of red		x		—	0.608	—		
		y		—	0.346	—		
Chromaticity of green		x		—	0.329	—		
		y		—	0.567	—		
Chromaticity of blue		x		—	0.152	—		
		y		—	0.130	—		
Luminance of white		Y_{LI}		320	400	—	cd/m^2	
White Uniformity		δ_W	θ =0°	—	1.25	1.40		[Note 9-2, 9-7]

※ The measurement shall be taken (30) minutes after lighting the module at the following rating:

Condition: PWM Duty = 100%

The optical characteristics shall be measured in a dark room or equivalent.

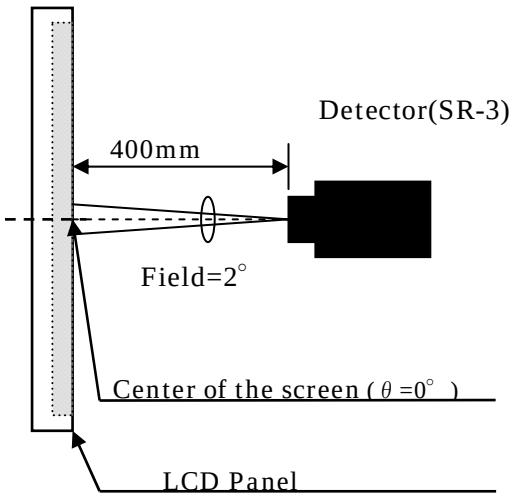
[Note 9-1] Measurement of viewing angle range and Response time.



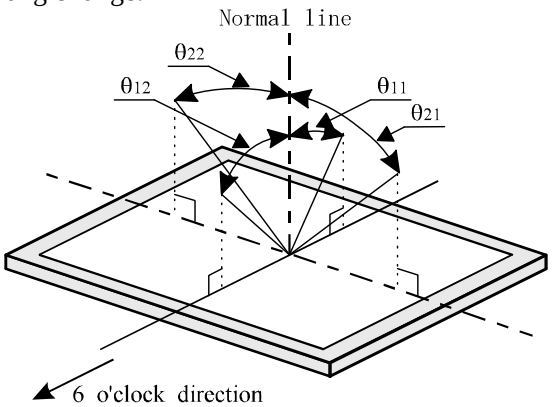
Viewing angle range:EZ-CONTRAST

/Response time: Photo diode)

[Note 9-2] Measurement of luminance and Chromaticity and Contrast.



[Note 9-3] Definitions of viewing angle range:



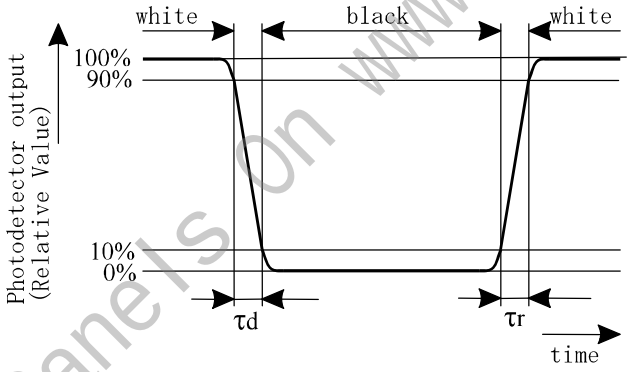
[Note 9-4] Definition of contrast ratio:

The contrast ratio is defined as the following.

$$\text{Contrast Ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

[Note 9-5] Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white" .

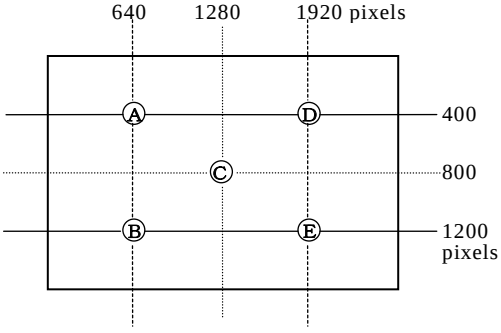


[Note 9-6] This shall be measured at center of the screen.

[Note 9-7] Definition of white uniformity:

White uniformity is defined as the following with five measurements (A～E).

$$\delta w = \frac{\text{Maximum Luminance of nine points (brightness)}}{\text{Minimum Luminance of nine points (brightness)}}$$



10 Display Quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standard.

11 Handling Precautions

a) Be sure to turn off the power supply when inserting or disconnecting the cable.
Please insert for too much stress not to join a connector in the case of insertion of a connector.

b) Be sure to design the cabinet so that the module can be installed without any extra stress such as warp or twist.

c) Since the front polarizer is easily damaged, pay attention not to scratch it.

d) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

e) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

f) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface. Handle with care.

g) Since CMOS LSI is used in this module, take care of static electricity and injure the human earth when handling. Observe all other precautionary requirements in handling components.

h) This module has its circuitry PCBs on the side and should be handled carefully in order not to be stressed.

i) Protect sheet(Laminate film) is attached to the module surface to prevent it from being scratched. Peel the sheet off slowly just before the use with strict attention to electrostatic charges. Ionized air shall be blown over during the action. Blow off the 'dust' on the polarizer by using an ionized nitrogen gun, etc. Working under the following environments is desirable.

- All workers wear conductive shoes, conductive clothes, conductive fingerstalls and grounding belts without fail.
- Use Ionized blower for electrostatic removal, and peel of the protect sheet with a constant speed. (Peeling of it at over 2 seconds)

j) The polarizer surface on the panel is treated with Anti Glare . In case of attaching protective board over the LCD, be careful about the optical interface fringe etc. which degrades display quality.

k) Do not expose the LCD module to a direct sunlight, for a long period of time to protect the module from the ultra violet ray.

l) When handling LCD modules and assembling them into cabinets, please be noted that long-term storage in the environment of oxidization or deoxidization gas and the use of such materials as reagent, solvent, adhesive, resin, etc. which generate these gasses, may cause corrosion and discoloration of the LCD modules.

m) Liquid crystal contained in the panel may leak if the LCD is broken. Rinse it as soon as possible if it gets inside your eye or mouth by mistake.

n) Disassembling the module can cause permanent damage and should be strictly avoided.
Please don't remove the fixed tape, insulating tape etc that was pasted on the original module.
(Except for protection film of the panel.)

o) Be careful when using it for long time with fixed pattern display as it may cause afterimage.
(Please use a screen saver etc., in order to avoid an afterimage.)

p) If a minute particle enters in the module and adheres to an optical material, it may cause display non-uniformity issue, etc. Therefore, fine-pitch filters have to be installed to cooling and inhalation hole if you intend to install a fan.

q) Epoxy resin (amine series curing agent), silicone adhesive material (dealcoholization series and oxime series),
tray forming agent (azo compound) etc, in the cabinet or the packing materials may induce abnormal display with polarizer film deterioration regardless of contact or noncontact to polarizer film.
Be sure to confirm the component of them.

r) Do not use polychloroprene. If you use it, there is some possibility of generating Cl_2 gas that influences the reliability of the connection between LCD panel and driver IC.

t) Do not put a laminate film on LCD module, after peeling of the original one. If you put on it, it may cause discoloration or spots because of the occurrence of air gaps between the polarizer and the film.

u) Ground module bezel to stabilize against EMI and external noise.

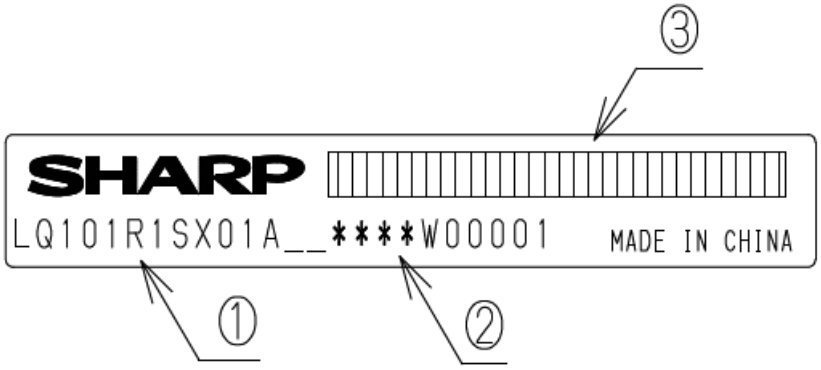
12 Packaging Condition

Piling number of cartons	6
Package quantity in one carton	40
Carton size △1	430(W)×346(H)×296(D)
Total mass of one carton filled with full modules	12.5kg
Packing form	Fig.1

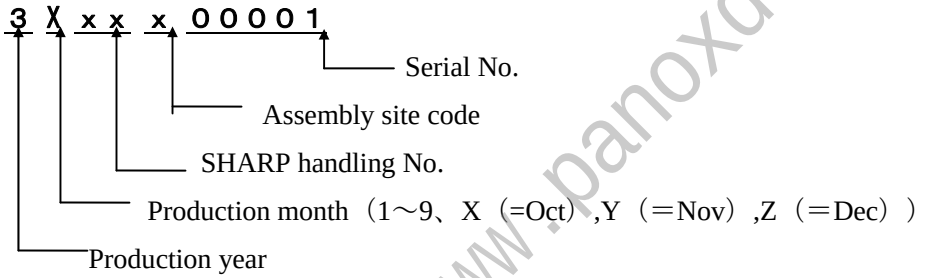
13 Label

1) Module Bar code label:

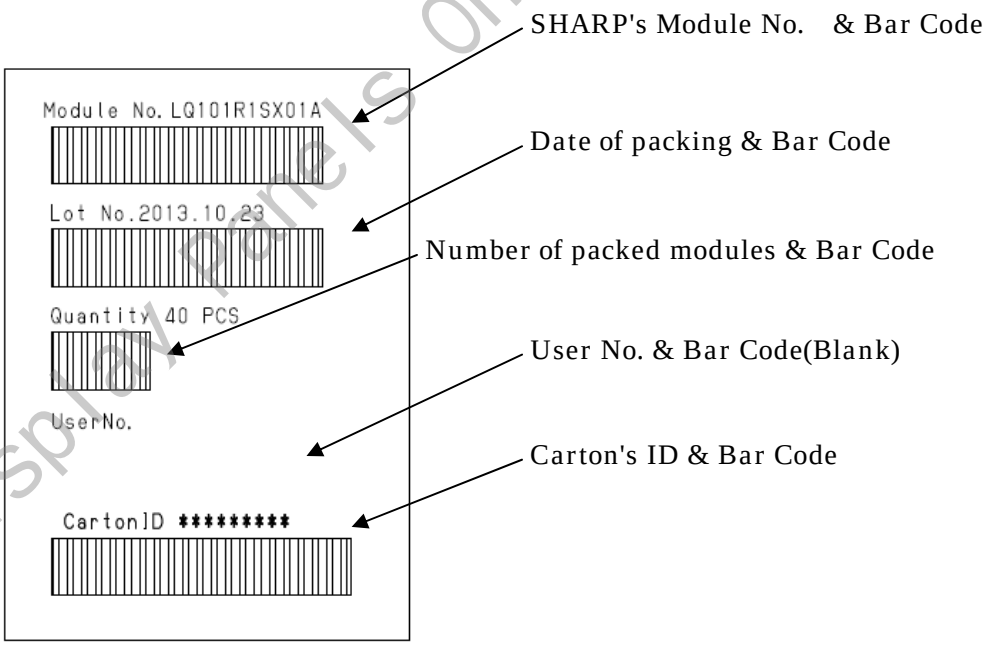
①Model.No. ②Serial No. ③Barcode(Serial No.)



Serial No.



2) Packing bar code label



14 RoHS Directive

This LCD module is compliant with RoHS Directive.

15 Reliability Test Item

No.	Test item	Conditions
1 △1	High temperature & high humidity storage test	Ta = 40℃ ; 95%RH 240h (No condensation)
2	High temperature storage test	Ta = 70℃ 240h
3	Low temperature storage test	Ta = -20℃ 240h
4	High temperature & high humidity operation test	Ta = 40℃ ; 90%RH 240h (No condensation)
5	High temperature operation test	Ta = 60℃ 240h
6	Low temperature operation test	Ta = -10℃ 240h
7	Vibration test (non- operating)	Frequency:10~57Hz/Vibration width (one side):0.076mm :57~500Hz/acceleration:9.8m/s^2 Sweep time: 11minutes Test period: 1 hour for each direction of X,Y,Z
8	Shock test (non- operating)	Max. gravity : 490 m/s^2 Pulse width : 11 ms, half sine wave Direction : ±X,±Y,±Z once for each direction.
9	ESD	±200V, 200pF(0Ω) 1time/each terminal

[Result Evaluation Criteria] Under the display quality test conditions with normal operation state. Do not change these conditions as such changes may affect practical display function.

[Normal operation state] Temperature : +15～+35℃, Humidity : 45～75%, Atmospheric pressure : 86～106kPa

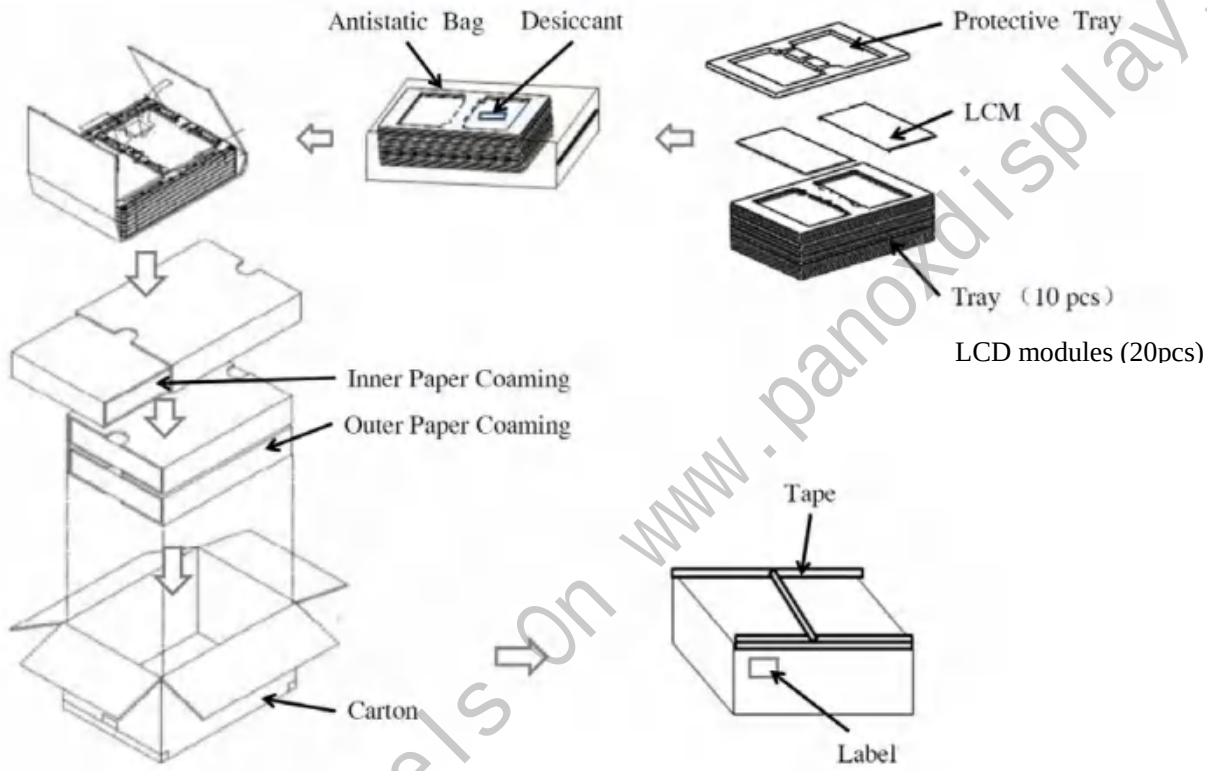
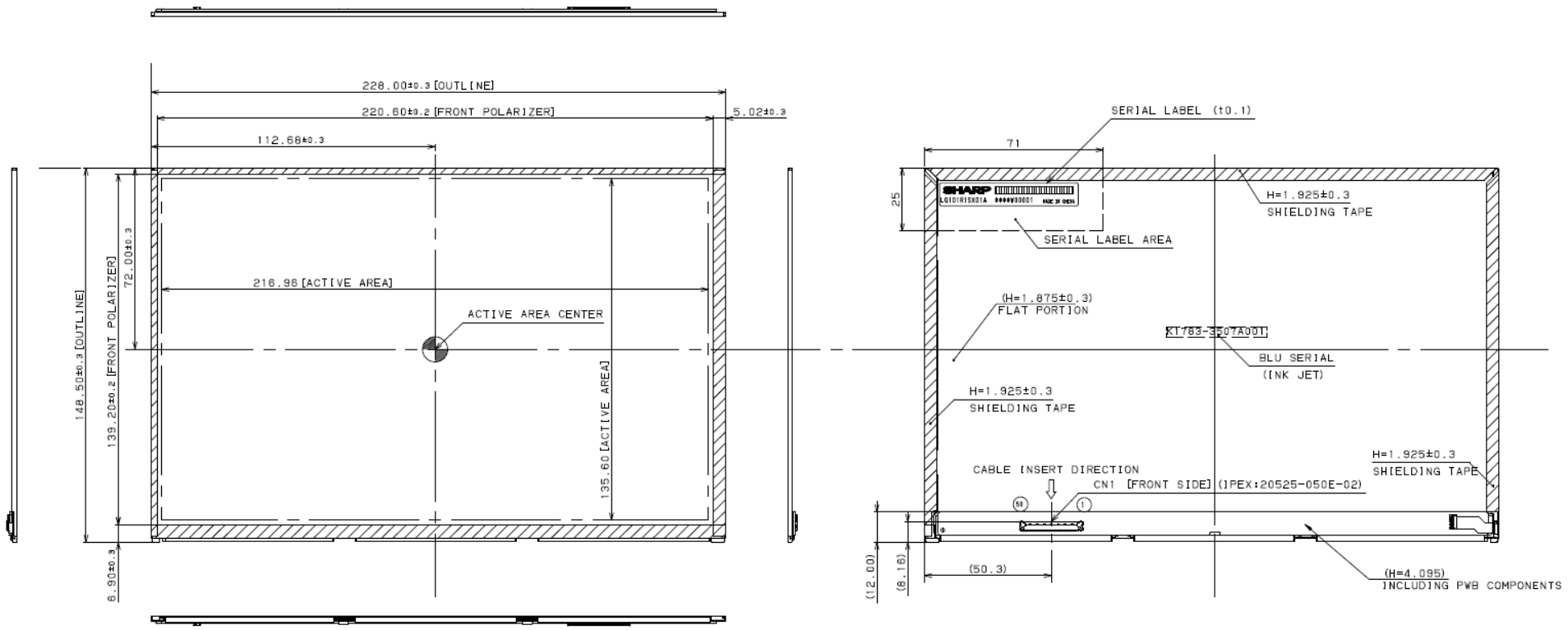


Fig. 1 Packaging Condition



Note

1. Unspecified tolerance to be 0.5.
2. Without warpage and deflection.
3. [H] means Module thickness from Front Polarizer surface to pertinent part.

Drawing No.2D-136-013-00

Fig. 2 Outline Dimensions