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	Technical Literature	DEVELOPMENT DIVISION BUSINESS UNIT 6 BUSINRSS DIVISON 2 DISPLAY DEVICE COMPANY SHARP CORPORATION

DEVICE Technical literature for
TFT LCD Module

Model No.

LS055B3SX04

Draft Version

DEVELOPMENT DIVISION
BUSINESS UNIT 6
BUSINRSS DIVISON 2
DISPLAY DEVICE COMPANY
SHARP CORPORATION

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[For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of glass, dropping the module or banging it against hard objects may cause cracks or fragmentation.

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.
(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

1. Operators
   Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.
2. Equipment and containers
   Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.
3. Floor
   Floor is an important part to leak static electricity which is generated from human body or equipment.
   There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the counter measure (electrostatic earth:$1\times10^{8}\Omega$) should be made.
4. Humidity
   Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.
5. Transportation/storage
   Storage materials must be anti-static to prevent causing electrostatic discharge.
6. Others
   Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.

(15) Do not touch the COG's patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

(22) Reflection sheet is exposed in the rear side of LCD module in order to make this module thinner and lighter.
Please do not laminate something on reflection sheet and push reflection sheet.
If do so, mura or blem could be occurred due to deflection of reflection sheet or breakage inside of LCD module.

[For Operating LCD Module]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

[Precautions for Storage]

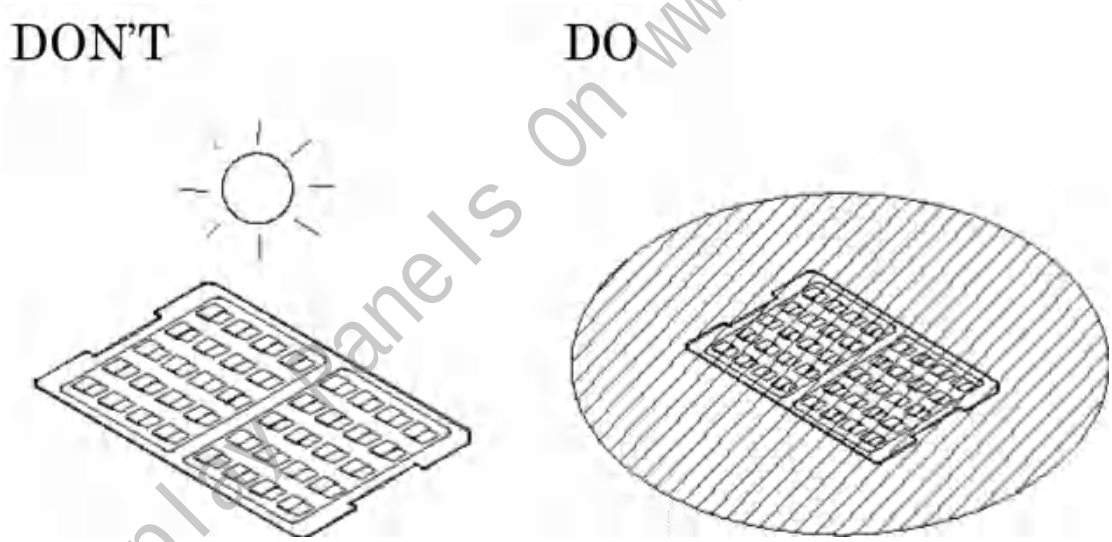
(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.

(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C, 60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.

(3) Keeping Method

a. Don't keeping under the direct sunlight.

b. Keeping in the tray under the dark place.



(4) Do not operate or store the LCD module under outside of specified environmental conditions.

(5) Be sure to prevent light striking the chip surface.

[Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VDDI-GND) are low when LCD module is working, place the de-coupling capacitor nearby LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don't touch to FPC surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

(8) U/V glue (Liquid OCA) should not be attached on upper polarizer edge, when customer laminate cover glass and touch panel and EyeCup on LCD.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.
Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenic (Aims test: negative) material is employed.

FPC: Dispose of as similar way to circuit board from electric device.

1. Application

This data sheet is to introduce the specification of active matrix 16,777,216 color LCD module.
Main color LCD module is controlled by Driver IC (Synaptics R63455).
If any problem occurs concerning the items not stated in this specification, it must be solved sincerely by both parties after deliberation.
As to basic specification of driver IC refer to the IC specification and handbook.

2. Construction and Outline

This module is a color transmissive, high contrast, wide viewing angle and active matrix LCD module.
Construction: LCD panel, Driver (COG), FPC with electric components, LEDs, prism sheet, diffuser, light guide, reflector and metal frame (+ plastic frame) to fix them mechanically.

3. Mechanical Specification

Table 1

Item	Specifications	Unit	Remarks
Screen size (Diagonal)	5.46inch	mm	
Active area	63.072(H) x 123.5817(V)	mm	
Pixel format	1920(H) x 3664(V)	Pixel	
	1 Pixel =R+G+B dots	-	
Pixel pitch	10.95(H) x 32.85(V)	µm	
Pixel configuration	R,G,B Vertical Stripes	-	
Display mode	Normally Black	-	
Number of colors	16,777,216	Colors	24 bits
Outline dimensions	66.3(W) x 135.98(H) x 1.65(D)	mm	Note 3-1
Mass	TBD	g	

Note 3-1) The above-mentioned table indicates module sizes without some projections and FPC

4. Pixel Configuration

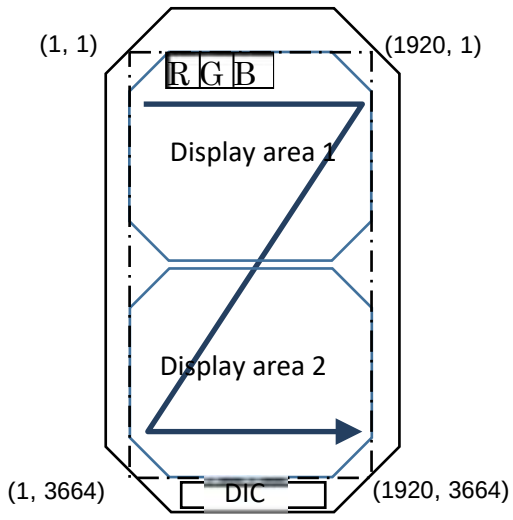


Fig.1

5. Input Terminal Names and Functions

Table2

Pin No	Signal	Function	I / O
1	GND	GND=0V	-
2	GND	GND=0V	-
3	TE	Tearing effect output	O
4	BLU_PWM_2	Control signal for LED backlight (refer to next page)	O
5	PNSLV	Selects the master port ("H"=port B, "L"=port A)	I
6	GND	GND=0V	-
7	GND	GND=0V	-
8	RESET	Reset pin (Low active)	I
9	Data 2P_B	Mipi data2 positive signal of MIPI Port B	I
10	GND	GND=0V	-
11	Data 2N_B	Mipi data2 negative signal of MIPI Port B	I
12	GND	GND=0V	-
13	GND	GND=0V	-
14	Data 1P_B	Mipi data1 positive signal of MIPI Port B	I
15	CLK P_B	Mipi clock positive signal of MIPI Port B	I
16	Data 1N_B	Mipi data1 negative signal of MIPI Port B	I
17	CLK N_B	Mipi clock negative signal of MIPI Port B	I
18	GND	GND=0V	-
19	GND	GND=0V	-
20	Data 0P_B	Mipi data0 positive signal of MIPI Port B	I / O
21	Data 3P_B	Mipi data3 positive signal of MIPI Port B	I
22	Data 0N_B	Mipi data0 negative signal of MIPI Port B	I / O
23	Data 3N_B	Mipi data3 negative signal of MIPI Port B	I
24	GND	GND=0V	-
25	GND	GND=0V	-
26	VSN	Power supply to the analog circuit (-5.7V)	I
27	VDDIO	Power supply to the logic circuit (1.8V)	I
28	VSN	Power supply to the analog circuit (-5.7V)	I
29	VDDIO	Power supply to the logic circuit (1.8V)	I
30	GND	GND=0V	-
31	VDDIO	Power supply to the logic circuit (1.8V)	I
32	VSP	Power supply to the analog circuit (5.7V)	I
33	GND	GND=0V	-
34	VSP	Power supply to the analog circuit (5.7V)	I
35	Data 3N_A	Mipi data3 negative signal of MIPI Port A	I
36	GND	GND=0V	-
37	Data 3P_A	Mipi data3 positive signal of MIPI Port A	I
38	Data 0N_A	Mipi data0 negative signal of MIPI Port A	I / O
39	GND	GND=0V	-
40	Data 0P_A	Mipi data0 positive signal of MIPI Port A	I / O
41	CLK N_A	Mipi clock negative signal of MIPI Port A	I
42	GND	GND=0V	-
43	CLK P_A	Mipi clock positive signal of MIPI Port A	I

44	Data 1N_A	Mipi data1 negative signal of MIPI Port A	I
45	GND	GND=0V	-
46	Data 1P_A	Mipi data1 positive signal of MIPI Port A	I
47	Data 2N_A	Mipi data2 negative signal of MIPI Port A	I
48	GND	GND=0V	-
49	Data 2P_A	Mipi data2 positive signal of MIPI Port A	I
50	BLU_PWM_1	Control signal for LED backlight 1 (refer to next page)	O
51	GND	GND=0V	-
53	GND	GND=0V	-
53	LED-C2	LED cathode 2	I
54	LED-C1	LED cathode 1	I
55	LED-A2	LED-anode 2	I
56	LED-A1	LED-anode 1	I
57	LED-C4	LED cathode 4	I
58	LED-C3	LED cathode 3	I
59	LED-A4	LED-anode 4	I
60	LED-A3	LED-anode 3	I

Connector: AXE660124(Panasonic)

6. Absolute Maximum Ratings

Table3 GND=0V

Parameter	Symbol	Conditions	Rated Value	Unit	Remarks
Driver IC (Positive Analog) Power Supply Voltage	VSP	Ta=+25°C	-0.3 to +6.5	V	Note6-1
Driver IC (Negative Analog) Power Supply Voltage	VSN	Ta=+25°C	+0.3 to -6.5	V	Note6-1
Driver IC (Digital) Power Supply Voltage	VDDIO	Ta=+25°C	-0.3 to +2.3	V	Note6-1
Temperature for storage	T_{stg}	-	-30 to +70	°C	Note6-2
Temperature for operation	T_{opr}	-	0 to +55	°C	Note6-2
LED Input electric current	ILED	Ta=+25°C	0 to 100 (Duty 10%)	mA	Note6-3

Note6-1) Voltage applied to GND pins. GND pin conditions are based on all the same voltage (0V). Always connect all GND externally and use at the same voltage.

Note6-2) Humidity: 95%RH Max.(at T*a*≤40°C). Maximum wet-bulb temperature is less than 39°C (at T*a*>40°C). Condensation of dew must be avoided.

Note6-3) Ambient temperature and the maximum input are fulfilling the following operating conditions.

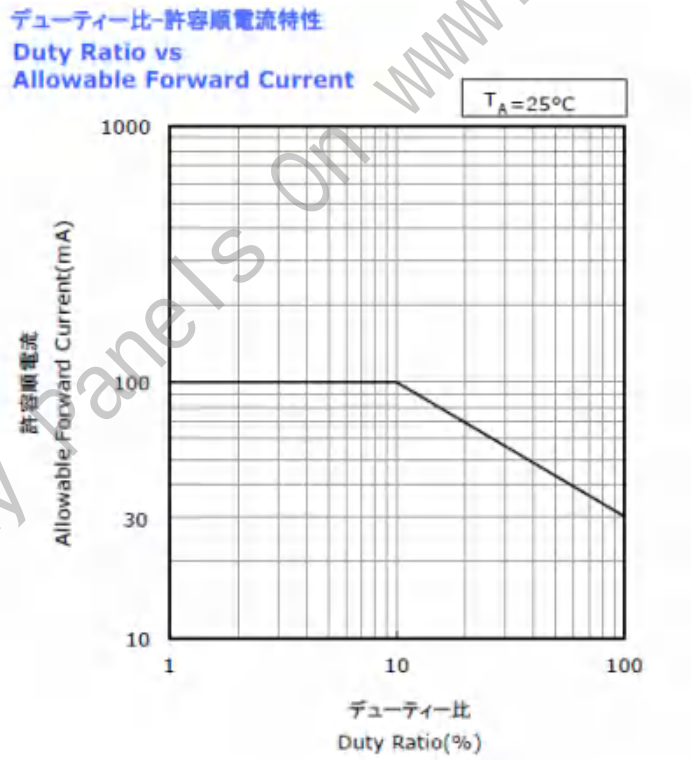


Fig. 2

7. Electrical Specifications

7-1. TFT-LCD Panel Driving Section

Table4

Ta=+25°C, GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Driver IC(Digital) Power Supply Voltage	VDDIO	1.7	1.8	1.9	V	Note7-1
Driver IC(Positive Analog) Power Supply Voltage	VSP	5.6	5.7	5.8	V	Note7-1
Driver IC(Negative Analog) Power Supply Voltage	VSN	-5.8	-5.7	-5.6	V	Note7-1
Input voltage (Low)	V_{IL}	0	-	0.3 VDDIO	V	Note7-2
Input voltage (High)	V_{IH}	0.7 VDDIO	-	VDDIO	V	Note7-2
Input current (Low)	I_{IL}	-10	-	-	μA	
Input current (High)	I_{IH}	-	-	10	μA	
Output voltage (Low)	V_{OL}	0	-	0.2 VDDIO	V	I_{OL}=+0.1mA
Output voltage (High)	V_{OH}	0.8 VDDIO	-	VDDIO	V	I_{OH}=-0.1mA
Current consumption	I_{VDDIO}	-	-	TBD	mA	Note7-3
	I_{VSP}	-	-	TBD	mA	
	I_{VSN}	TBD	-	-	mA	
Power consumption		-	495	TBD	mW	Note7-4

Note7-1) Include Ripple Noise

Note7-2) Applied overshoot

Note7-3) 72Hz / D-phy 8lane / with DSC / Worst pattern

Note7-4) 72Hz / D-phy 8lane / with DSC / White pattern

7-2. Back Light Driving Section

Table5

Ta=+25°C, GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
LED Voltage	V_{LED}	-	6.08	-	V	per unit
LED Current	I_{LED}	-	46.8	-	mA	Duty 10%
Power Consumption	W_{LED}	-	455	-	mW	100cd/m2
LED Quantity			16		pcs	

8. Timing characteristics of input signals

8-1. MIPI DC/AC Characteristics

<DC characteristics>

MIPI DSI characteristics

Table6

Item		Symbol	Unit	Test Condition	Minimum	Typical	Maximum
HS-RX	Differential input high threshold	VIDTH	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	–	–	70
	Differential input low threshold	VIDTL	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	-70	–	–
	Single-ended input low voltage	VILHS	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	-40	–	–
	Single-ended input high voltage	VIHHS	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	–	–	460
	Common-mode voltage HS receive mode[1]	VCMRX(DC)	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	70	–	330
	Differential input impedance[2]	ZID	Ω	IOVCC = DPHYVCC = 1.65V ~ 1.95V	–	100	–
LP-RX	Logic 0 input voltage not in ULP State	VIL	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	-50	–	550
	Logic 1 input voltage	VIH	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	880	–	1350
	I/O leakage current	ILEAK	μA	Vin = -50 mV ~ 1350 mV	-10	–	10
LP-TX	Thevenin output low level	VOL	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	-50	–	50
	Thevenin output high level	VOH	V	IOVCC = DPHYVCC = 1.65V ~ 1.95V	1.1	1.2	1.3
	Output impedance of LP transmitter[2]	ZOLP	Ω	IOVCC = DPHYVCC = 1.65V ~ 1.95V	110	–	–
CD-RX	Logic 0 contention threshold	VILCD	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	–	–	200
	Logic 1 contention threshold	VIHCD	mV	IOVCC = DPHYVCC = 1.65V ~ 1.95V	450	–	–

1. VCMRX (DC) = (VDP+VDN)/2
2. Excluding COG resistance (contact resistance and indium tin oxide (ITO) wiring resistance)

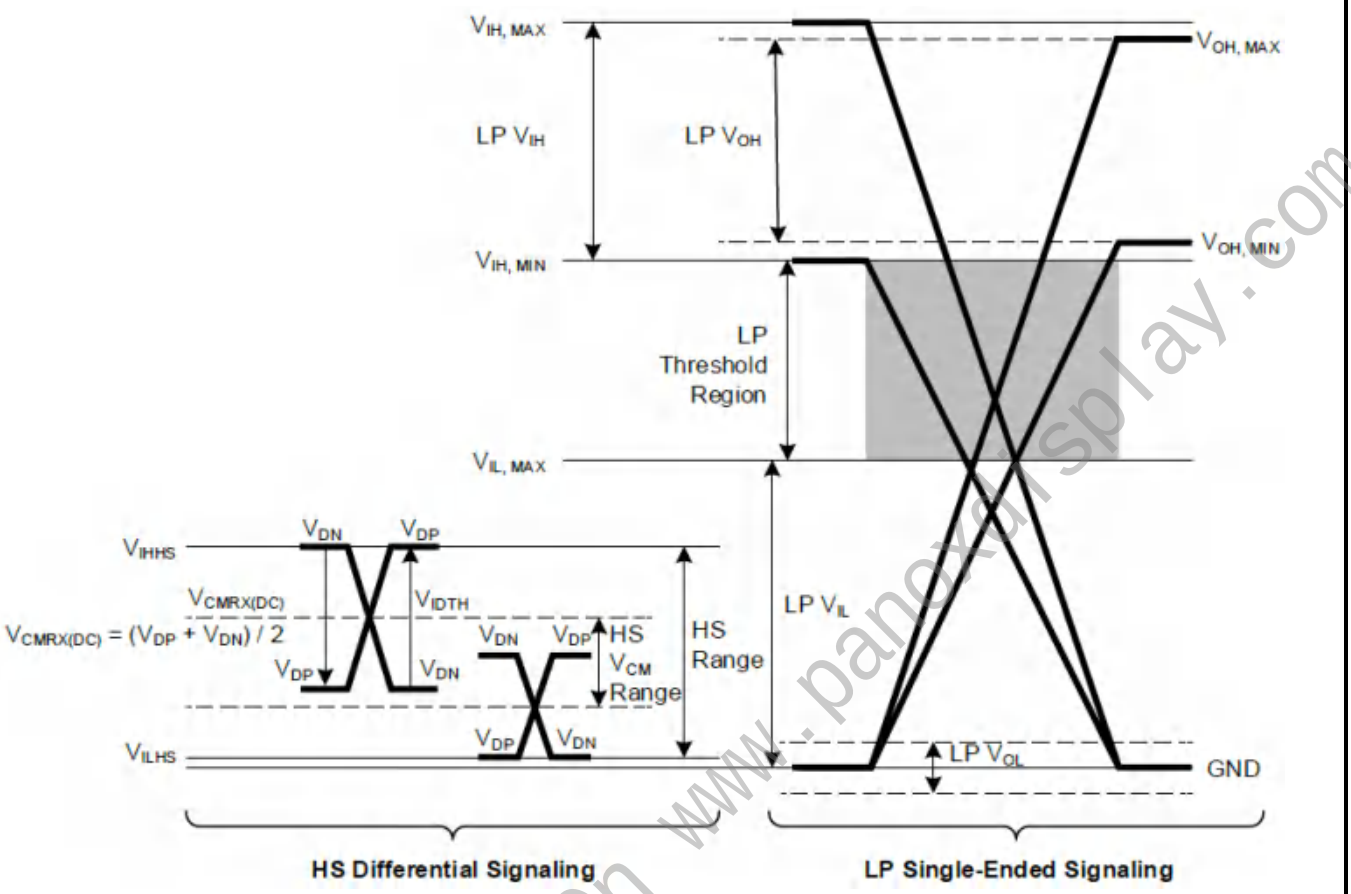


Fig. 3

<AC Characteristics>
MIPI DSI HS-RX Clock and Data-Clock Specifications
Table7

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum	Footnote
DSICLK frequency	fDSICLK	MHz	IOVCC = DPHYVCC = 1.65 ~ 1.95V	250	–	750	1
DSICLK cycle time	tCLKP	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	1.33	–	4	1
DSI data transfer rate	tDSIR	Mbps	IOVCC = DPHYVCC = 1.65 ~ 1.95V	500	–	1500	1
Data to clock setup time	tSETUP	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate ≦ 1000 Mbps	0.15	–	–	1, 3
		ns		0.15	–	–	1, 2, 3
		UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate > 1000 Mbps	0.2	–	–	1, 3
		ns		0.13	–	–	1, 2, 3
Clock to data hold time	tHOLD	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate ≦ 1000 Mbps	0.15	–	–	1, 3
		ns		0.15	–	–	1, 2, 3
		UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V DSI transfer rate > 1000 Mbps	0.2	–	–	1, 3
		ns		0.13	–	–	1, 2, 3

1. Minimum 110 mV/-110 mV HS differential swing is required for display data transfer.
2. tSETUP/tHOLD times are measured without HS-TX jitter.
3. Minimum tSETUP/tHOLD Time is 0.15 UI or 0.20 UI. This value may change according to the DSI transfer rate.

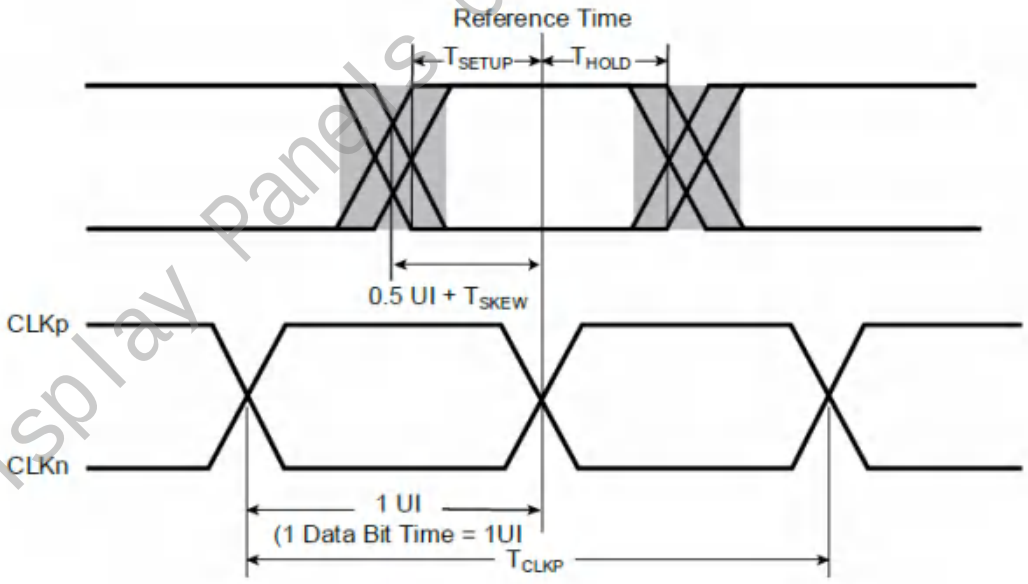


Fig. 4

MIPI DSI LP-RX/TX Clock and Data-Clock Specifications

Table8

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	40 ns + 4 • UI	—	85 ns + 6 • UI
$T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence	$T_{HS-PREPARE} + T_{HS-ZERO}$	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	145ns + 10 • UI	—	—
Time to drive flipped differential state after last payload data bit of a HS transmission burst[1, 2]	$T_{HS-TRAIL}$	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	max (n • 8 • UI, 60 ns + n • 4 • UI)	—	—
Time to drive LP-11 after a HS burst	$T_{HS-EXIT}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	100	—	—
Time to drive LP-00 after a turnaround request	T_{TA-GO}	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	4 • T_{LPTX}		
Time that the new TX waits after the LP-10 state before transmitting the bridge state (LP-00) during a link turnaround	$T_{TA-SURE}$	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	1 • T_{LPTX}		2 • T_{LPTX}
Time that the new TX drives the bridge state (LP-00) after accepting control during a link turnaround	T_{TA-GET}	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	5 • T_{LPTX}		
Length of any low-power state period	T_{LPX}	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	50	—	—
Ratio of $T_{LPX(MASTER)}$/$T_{LPX(SLAVE)}$ between the master and slave sides	Ratio T_{LPX}	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	2/3	—	3/2
Time that the transmitter continues sending HS clock after the last associated data lane has transitioned to LP mode[3]	$T_{CLK-POST}$	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	60 ns + 52 UI	—	—
$T_{CLK-PREPARE}$ +time for lead HS-0 drive period before starting the clock	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	300	—	—
Time that the HS clock is driven prior to any associated data lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V	8	—	—
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	38	—	95
Time to drive HS differential state after last payload clock bit of an HS transmission burst	$T_{CLK-TRAIL}$	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	60	—	—
Time from the start of THS-TRAIL period to the start of the LP-11 state[2]	T_{EOT}	—	IOVCC = DPHYVCC = 1.65 ~ 1.95V	—	—	105 ns + n • 12 • UI
Length of the low-power TX period when using the DSI-2 clock[4, 5]	T_{LPTX1}	UI	IOVCC = DPHYVCC = 1.65 ~ 1.95V	—	1/fTXCLK	—
Length of the low-power TX period when using the internal OSC clock[4, 5]	T_{LPTX2}	ns	IOVCC = DPHYVCC = 1.65 ~ 1.95V	—	8/fosc	—

1. If a > b then max (a, b) = a, otherwise max (a, b) = b
2. Where n = 1 for forward direction HS mode.
3. R63455 works with this specification, although the last part of the internal process remains when the clock lane enters LP-11 and R63455 works without the remaining process if tCLK-POST is more than 512 UI.
4. R63455 uses the DSI clock from the host processor if the DSI-2 clock lane is active, and uses the internal oscillator clock if the DSI-2 clock lane is stopped.
5. See section "DSI-2 Control Setting (B6h)" (D-PHY) in this document for more information about the DSITXDIV register function.

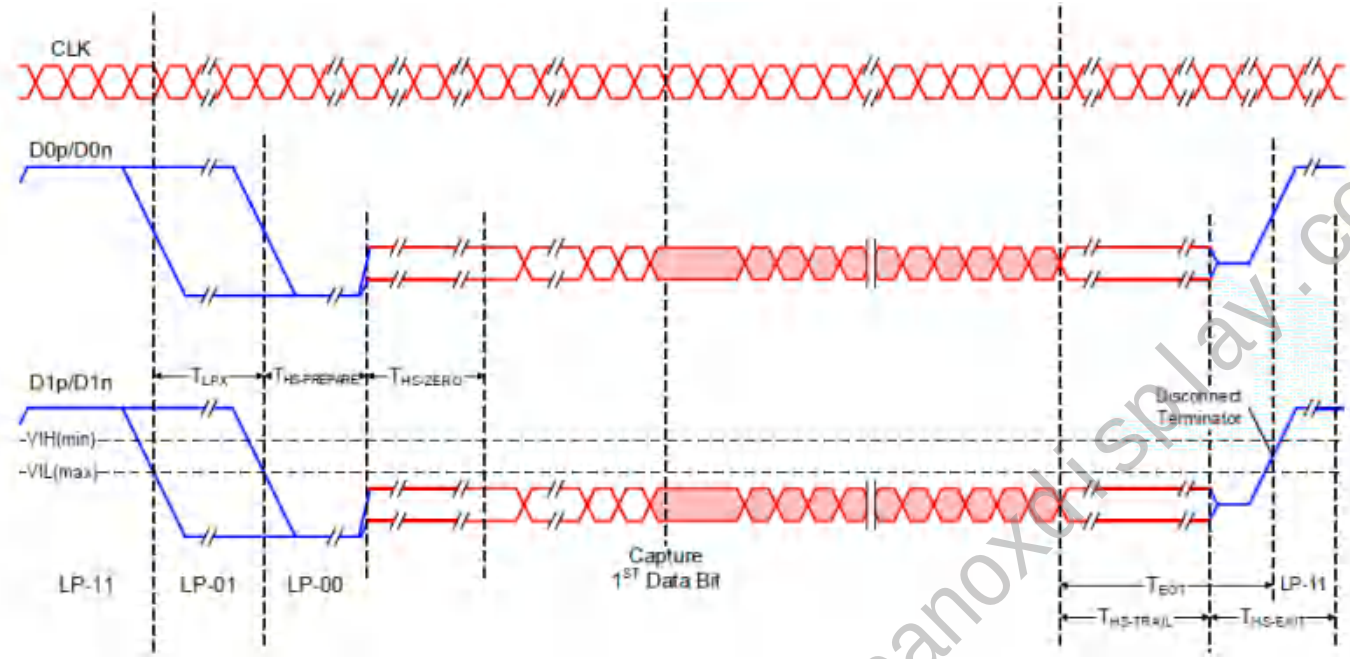


Fig. 5

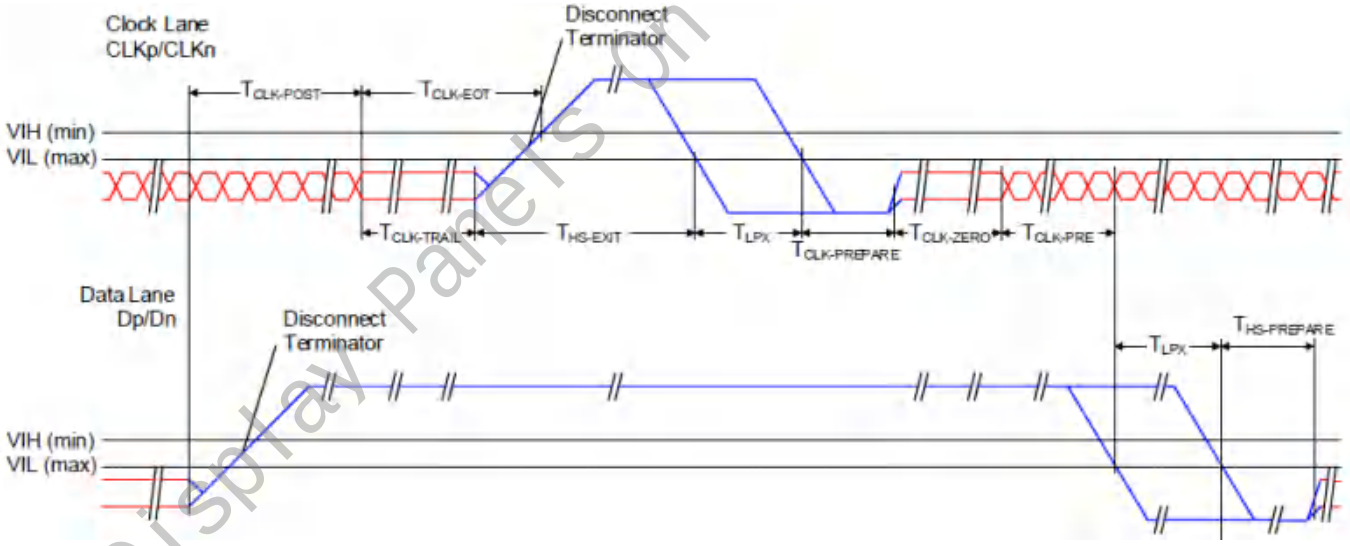


Fig. 6

8-2. Reset Timing Characteristics

Table9

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Reset low-level width1	tRW1	µs	Power supply on	3000	–	–
Reset low-level width2	tRW2	µs	Operation	1000	–	–
Reset low-level width3	tRW5	ms	Power supply off	25	–	–
Reset to MIPI command	tRT1	ms	Sleep in	20	–	–
Noise reject width	tRESNR	µs	–	–	–	1

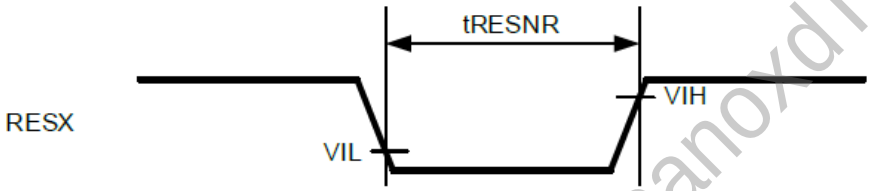


Fig. 7 Reset reject pulse width

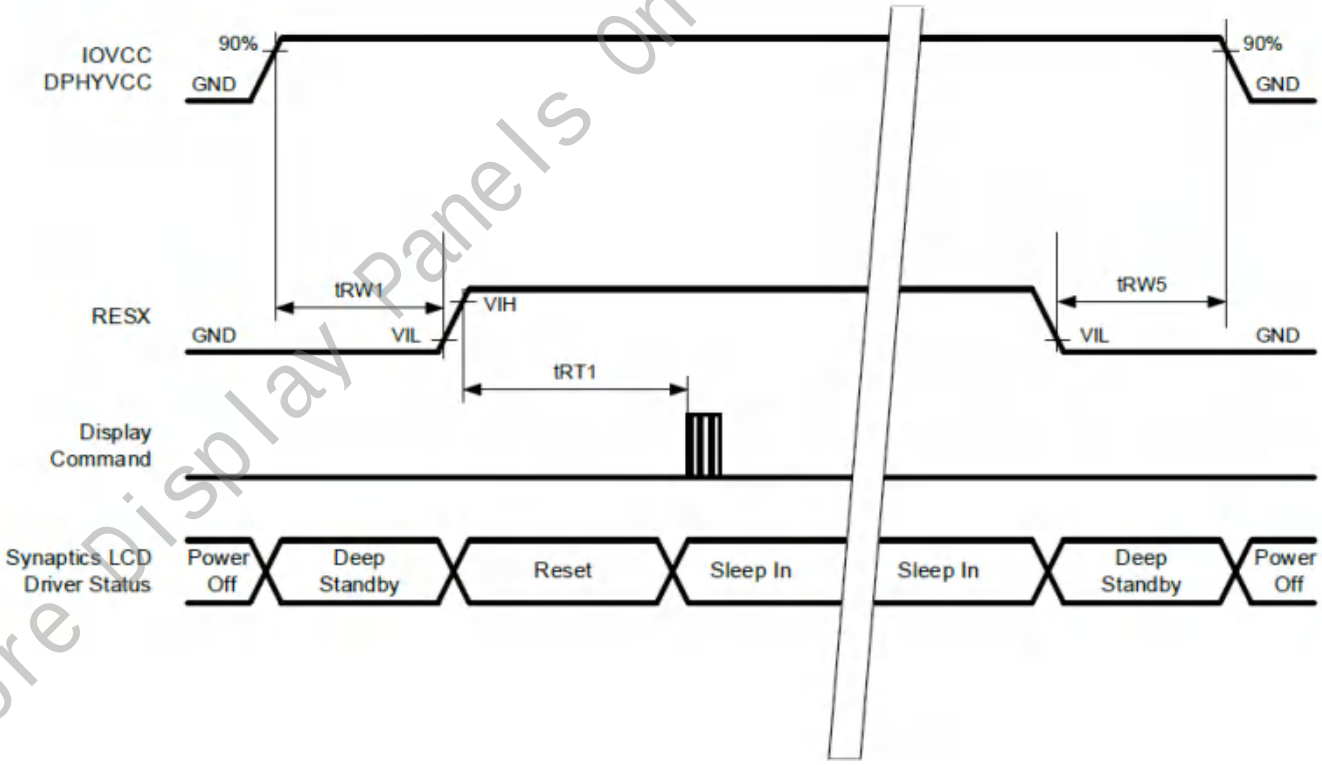


Fig. 8 Reset timing characteristics at power supply on

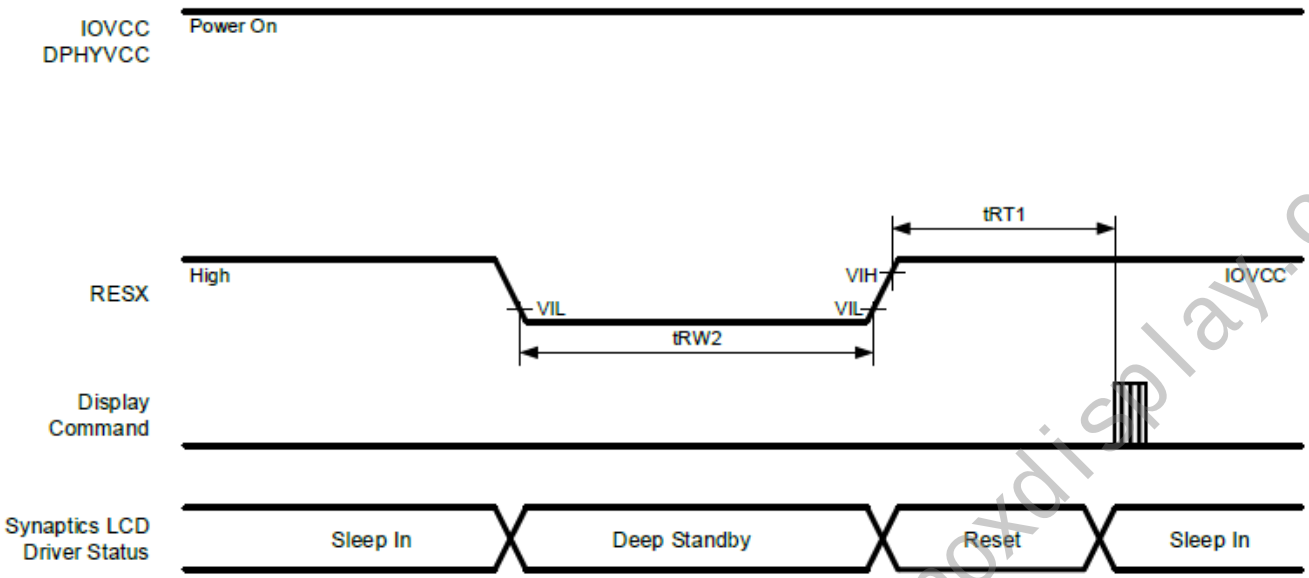


Fig. 9 Reset timing in Sleep in

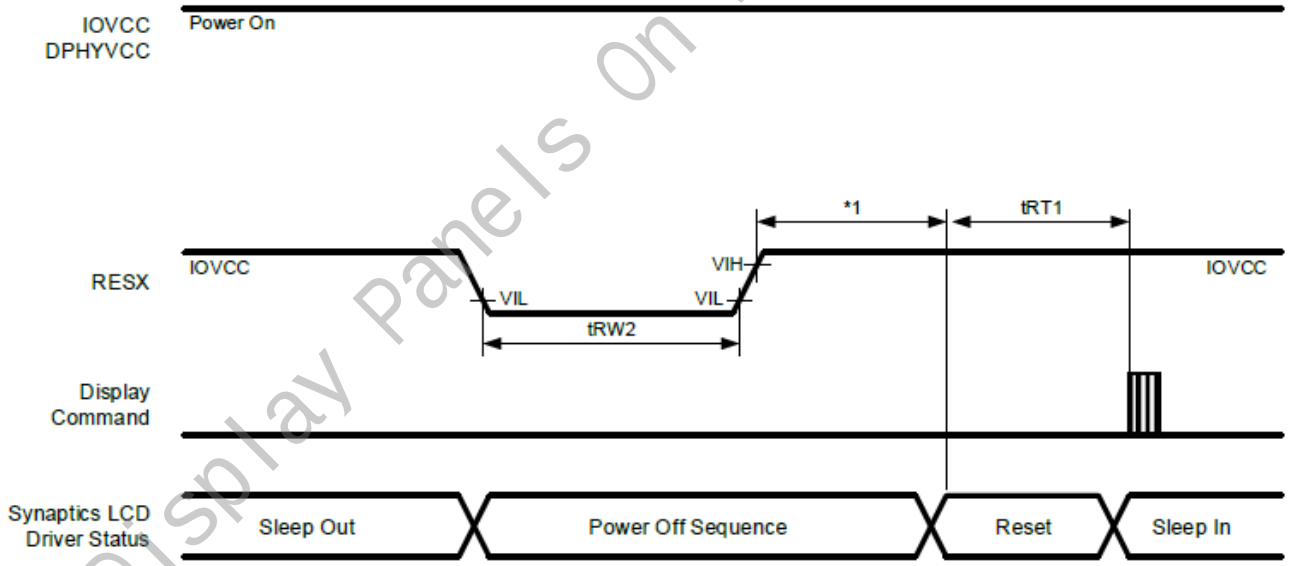


Fig. 10 Reset timing in Sleep out

8-3. Display Timing

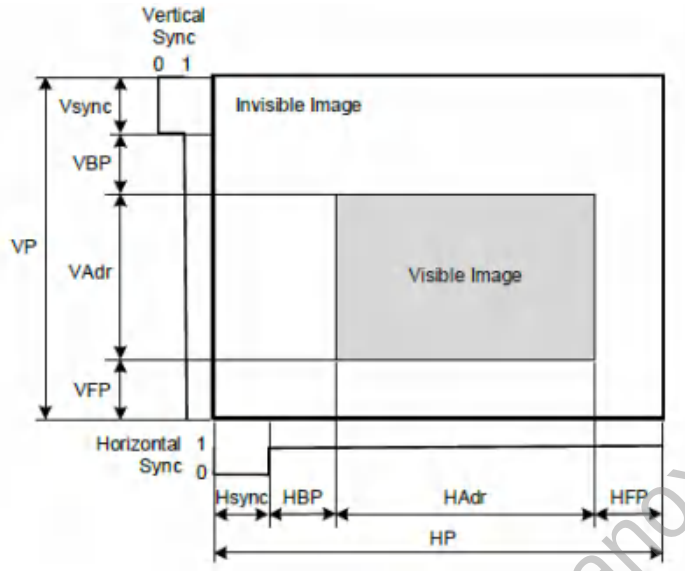


Fig. 11

< Interface Display timing >

Table10 I/F: Mipi 8lane w/Video Through +DSC Mode (1/3 Compression), Dots Size: 1920xRGBx3664

Item	Min.	Typ.	Max.	Unit
DSI MIPI lanes (D-PHY)	-	8	-	lane
MIPI rate per lane	-	-	1100	Mbps
Slice width	-	480	-	pixel
Slice height	-	(16)	-	H
H resolution	-	1920		pixel
V resolution	-	3664		H
VFP	4	2460	-	H
VBP (including Vsync width)	3	20	-	H
V active	-	3664	-	H
1H Time	-	2.26	-	us
Frame rate	-	72	-	Hz

< B/L Impulse Driving timing (72Hz frame / TBDms scanning driving) >

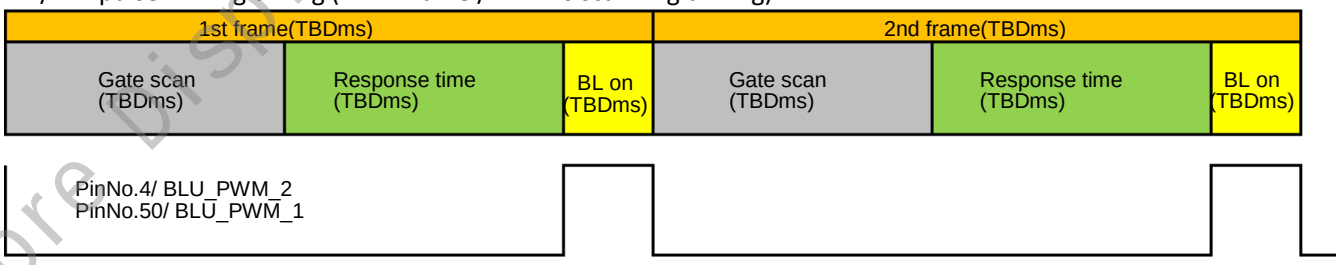


Fig. 12

9. Power Sequence

Below shows timing diagram of power on off sequence.

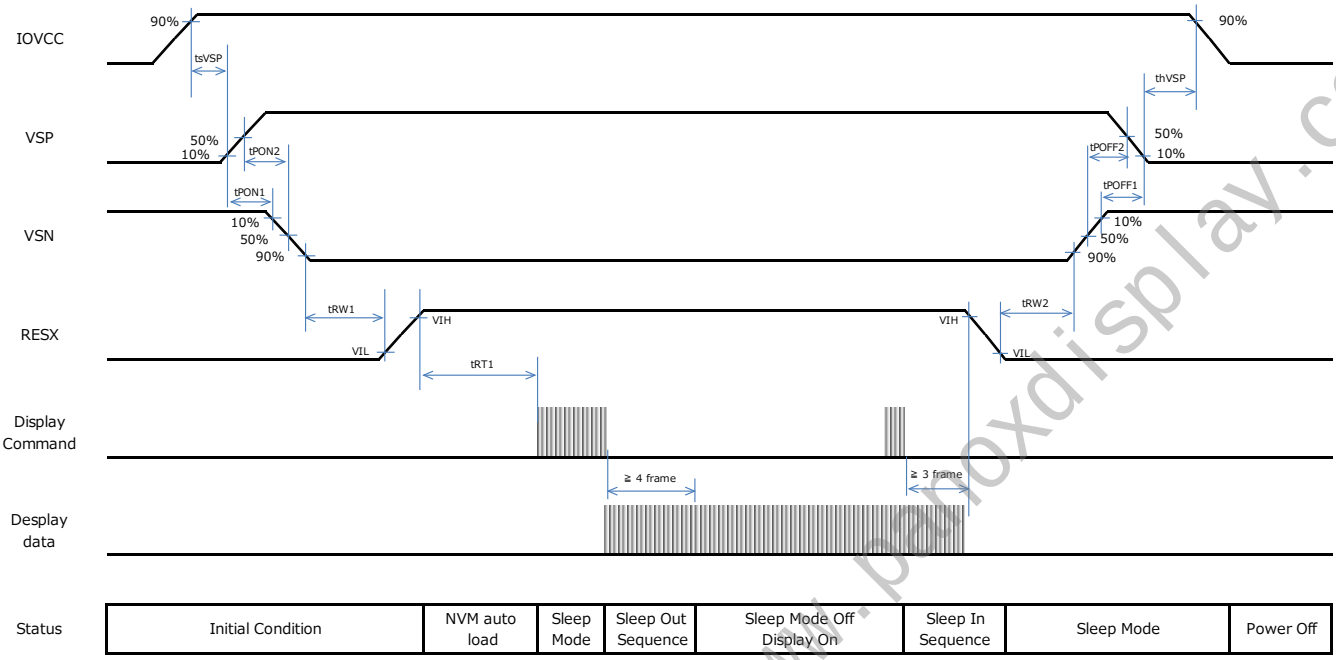


Fig. 13

<Power supply timing characteristics>

Table11

Item	Symbol	Min	Max	Unit
VSP-VSN delay time (10% to 10%)	tPON1	0	-	µs
VSP-VSN delay time (50% to 50%)	tPON2	0	-	µs
System power on to VSP ON time	tsVSP	1	-	ms
VSN-VSP delay time (10% to 10%)	tPOFF1	0	-	µs
VSN-VSP delay time (50% to 50%)	tPOFF2	0	-	µs
VSP OFF to system power OFF time	thVSP	0	-	µs

<Reset timing characteristics>

Table12

Item	Symbol	Min	Max	Unit
Reset low-level width1	tRW1	2	-	ms
Reset low-level width2	tRW2	25	-	ms
Reset to MIPI command	tRT1	20	-	ms

9-1. Power ON Sequence

Table 13: Recommended Power On Sequence

Step	State	Action/Command	I/F (Data Type)			Comman	Date
1	Initial Condition	RESX = L					
2		Power Supply ON : IOVCC					
3		- Wait ≧1ms					
4		Power Supply ON : VSP					
5		- Wait ≧0ms					
6		Power Supply ON : VSN					
7		- Wait ≧2ms					
8		RESX = H					
9	NVM Auto Load	- Wait ≧20ms					
10	Sleep Mode On	Manufacture Command Access Protect	DS	Generi	6'h2	**CMD**	8'hB0
11						P1	8'h00
12		Display Mode	DS	Generi	6'h2	**CMD**	8'hB7
13						P1	8'h12
14		Generic pin output setting 2	DS	Generi	6'h2	**CMD**	8'hB9
15						P1	TBD
16						P2	TBD
17						P3	TBD
18						P4	TBD
19						P5	TBD
20						P6	TBD
21						P7	TBD
22						P8	TBD
23						P9	TBD
24						P10	TBD
25						P11	TBD
26						P12	TBD
27						P13	TBD
28						P14	TBD
29						P15	TBD
30						P16	TBD
31		NVM Load setting	DS	Generi	6'h2	**CMD**	8'hD
32						P1	8'h00
33		Manufacture Command Access Protect	DS	Generi	6'h2	**CMD**	8'hB0
34						P1	8'h03
35	Sleep Mode On	get_compression_mode	DS	DCS	6'h3	**CMD**	8'h03
36						P1	TBD
37		set_display_on	DS	DCS	6'h0	**CMD**	8'h29
38		exit_sleep_mode	DS	DCS	6'h0	**CMD**	8'h11
39	mipi data tranfer	Start mipi data tranfer (including					
40	Sleep Out Sequence	- Wait ≧ 4-Frame data					
41	Sleep Mode Off Display On						

9-2. Power OFF Sequence

Table 14: Recommended Power Off Sequence

Step	State	Action/Command	I/F (Data Type)			Command	Data
1	Sleep Mode Off	Set_display_off	DSI	DCS	6'h05	**CMD**	8'h28
2		Enter_sleep_mode	DSI	DCS	6'h05	**CMD**	8'h10
3	mipi data tranfer input	Input mipi dummy display data after “Enter sleep mode" (including Vsync/Hsync)					
4	Sleep In Sequence	- Wait ≧ 3-Frame dummy display data					
5	Sleep Mode On	RESX = L					
6		- Wait ≧25ms					
7		Power Supply OFF : VSN					
8		- Wait ≧0ms					
9		Power Supply OFF : VSP					
10		- Wait ≧0ms					
11		Power Supply OFF : IOVCC					
12	Power Off						

10. Input Signals, Basic Display Colors and Gray Scale of Each Color

Table15 0: Low level voltage, 1: High level voltage

	Colors & Gray Scale	Gray Scale	Data signals Signal																							
			R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
			LSB							MSB	LSB							MSB	LSB							MSB
Basic Color	Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	-	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	-	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	-	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	-	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓								↓								↓			
	⇩	↓					↓								↓								↓			
	Brighter	GS253	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇩	GS254	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	GS255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	↓					↓								↓								↓			
	⇩	↓					↓								↓								↓			
	Brighter	GS253	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	⇩	GS254	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	GS255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	⇧	GS1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	⇧	↓					↓								↓								↓			
	⇩	↓					↓								↓								↓			
	Brighter	GS253	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	⇩	GS254	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	GS255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Each basic color can be displayed in 256 gray scales from 8 bit data signals. According to the combination of total 24 bit data signals, the 16,777,216-color display can be achieved on the screen. screen.

11. Optical Characteristic

Table16 VDDI=1.8V, AVDD=5.7V, AVEE=-5.7V, Frame Frequency = 72fps, ILED=46.8mA@10%Duty, Ta = 22°C(±3°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Contrast Ratio	CR1	θ=0°	500	650	-	-	Note11-1,2 *1)
	CR2	θ=30°	100	-	-	-	
Response Time	τ	θ=0°	-	3.5	4.0	ms	Ta=+25℃ Note11-3
			-	4.8	5.5	ms	Ta=+10℃ Note11-3
White Chromaticity	x	θ=0°	0.269	0.294	0.319	-	*1)
	y		0.289	0.314	0.339	-	
Red Chromaticity	x		0.610	0.640	0.670	-	
	y		0.301	0.331	0.361	-	
Green Chromaticity	x		0.271	0.301	0.331	-	
	y		0.571	0.601	0.631	-	
Blue Chromaticity	x		0.124	0.154	0.184	-	
	y		0.027	0.057	0.087	-	
Brightness	L	θ=0°	80	100	120	cd/m²	*1)
Luminance Non-Uniformity	-	θ=0°	-	-	30	%	Note11-4
Color Non-Uniformity	-	θ=0°	-	-	TBD	Δu'v'	*1) Note11-5
Color Uniformity	-	θ=0°	-	-	TBD	Δu'v'	*1) Note11-6
Color shift	-	θ=30°	-	-	TBD	Δu'v'	
NTSC Ratio	S	θ=0°	65.6	70.8	-	%	*1)
Gamma	γ	θ=0°	TBD	2.2	TBD	-	*1) *2)
Flicker	F	θ=0°	-	-	-30	dB	Note11-7
Crosstalk	CT	θ=0°	-	-	2	%	Note11-8

*1) To be discussed after sample evaluation.

*2) In range between gray level 200 and 254, 2.20+/-TBD

*3) The measuring method of the optical characteristics is shown by the following figure.
A measurement device is TOPCON luminance meter SR3/ SR-UL1R (Measurement angle 1°).

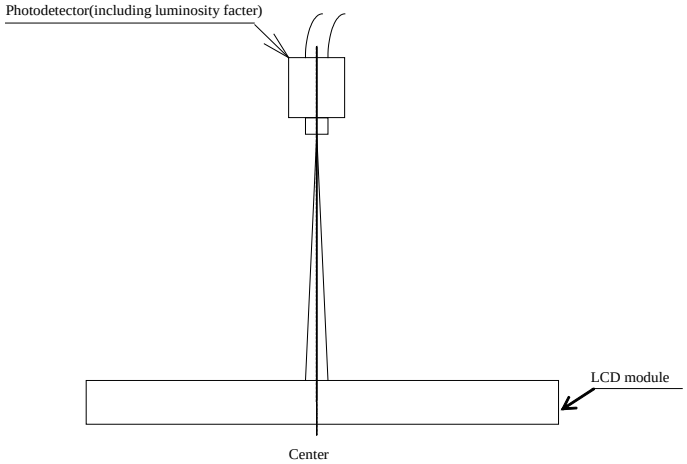


Fig. 15

Note 11-1) Contrast / NTSC / GAMMA viewing angle is defined as follows.

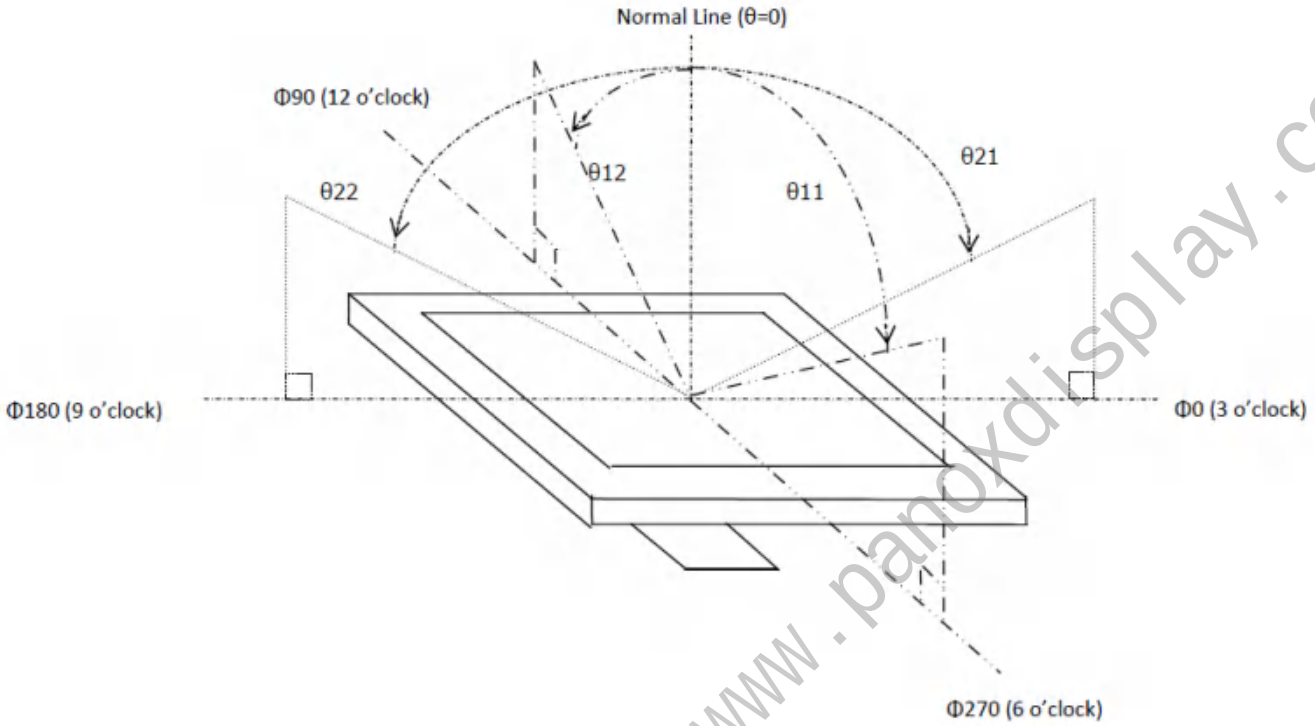


Fig. 16

Note 11-2) Definition of contrast ratio:

The contrast ratio is defined as the follows:

$$\text{Contrast Ratio (CR)} = \frac{Luminance(brightness)\ with\ all\ pixels\ white}{Luminance(brightness) with\ all\ pixels\ black}$$

Note 11-3) Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "any gray" and "any other gray"

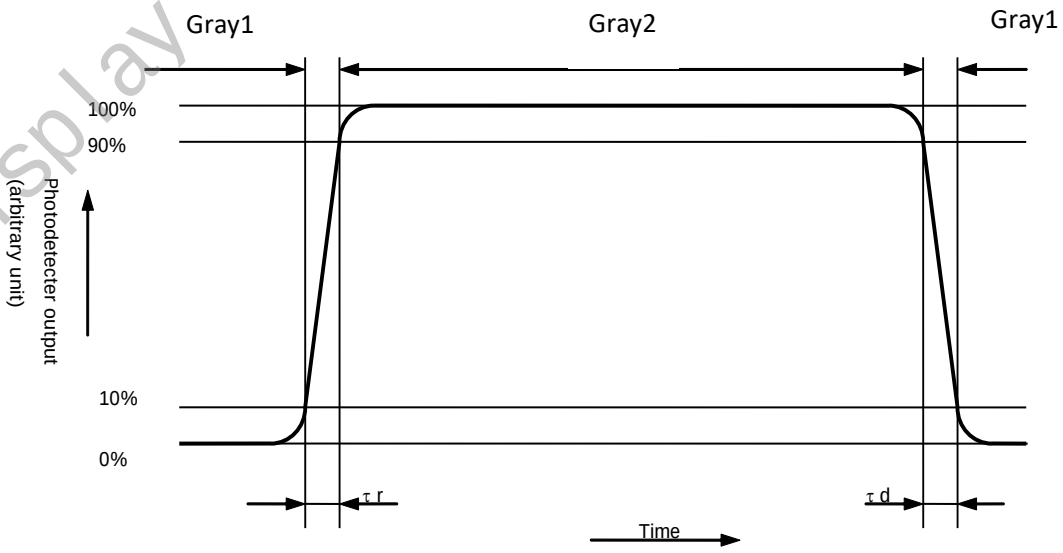


Fig. 17

Note 11-4) Luminance Non-Uniformity
Test conditions: Use instrument inspection conditions and control ambient light to avoid impact to measurement.

Test method: Use spot measurement device, such as Konica Minolta SR3/ SR-UL1R Display Color Analyzer or equivalent, to measure luminance and color at each point (9 points per eye, total 18 points) which is specified in Figure 18.

The display shall be illuminated in W127 image. The average luminance (in cd/m2) of each eye shall be calculated.

Maximum Variation is calculated using the following formula:

$$Maximum\ Variation = (Max - Min)/Average\ (\%)$$

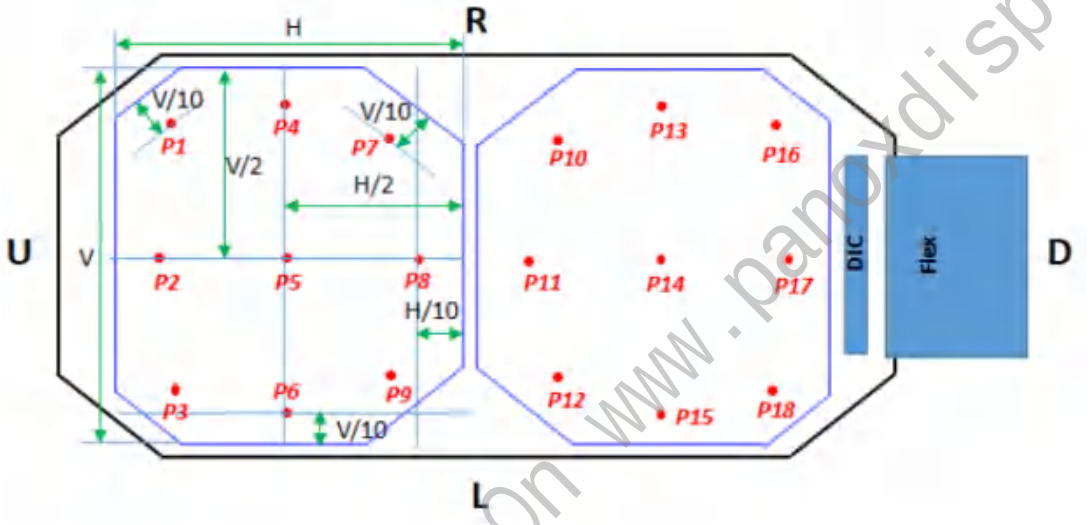


Fig. 18 Coordinates of luminance measurement points

Acceptable performance is listed in the table below for operation in all modes at the specified duty cycle.
Table 17

Tests	LL	Nom	UL	Unit	Notes
Maximum variation within each eye	-	-	30	%	Left eye: P1 ~ P9 Right eye: P10 ~ P18
Maximum variation between averages of each eye	-	-	15	%	Left eye: P1 ~ P9 Right eye: P10 ~ P18
Maximum variation between P5 and P14	-	-	15	%	

Note 11-5) Color Non-Uniformity
Test conditions: Use instrument inspection conditions and control ambient light to avoid impact to measurement.

Test method: Use spot measurement device, such as Konica Minolta SR3/ SR-UL1R Display Color Analyzer or equivalent, to measure luminance and color at each point (9 points per eye, total 18 points) which is specified in Figure 18.

The display shall be illuminated using white, red, green, blue primaries. The color (in CIE 1976 u'v' space) of each point shall be measured.

Acceptable performance is listed in the table below for operation in all modes at the specified duty cycle.
Table 18

Tests	**Display Primaries**	**LL**	**Nom**	**UL**	**Unit**	**Notes**
Maximum color variation	White 255	-	-	TBD	Δu'v'	Between any 2 random points
	Red 255	-	-	TBD	Δu'v'	
	Green 255	-	-	TBD	Δu'v'	
	Blue 255	-	-	TBD	Δu'v'	
Maximum neighboring color variation	White 255	-	-	TBD	Δu'v'	Between any 2 neighboring points
	Red 255	-	-	TBD	Δu'v'	
	Green 255	-	-	TBD	Δu'v'	
	Blue 255	-	-	TBD	Δu'v'	
Maximum color variation between P5 and P14	White 255	-	-	TBD	Δu'v'	Between P5 and P14 points
	Red 255	-	-	TBD	Δu'v'	
	Green 255	-	-	TBD	Δu'v'	
	Blue 255	-	-	TBD	Δu'v'	

Note 11-6) Color Uniformity Throughout Gray Levels
Test conditions: Use instrument inspection conditions and control ambient light. Perform measurement at each Display Center.

Test method: Use spot measurement device, such as Konica Minolta SR3/ SR-UL1R Display Color Analyzer, Radiant Vision Systems i16 or equivalent, to measure luminance and color at each Display Center which is specified in Figure 19.

The color uniformity through gray levels measures the color difference in u'v' space between the white point (when illuminated with a white 255 image) and the color point for all the specified gray levels of the display.

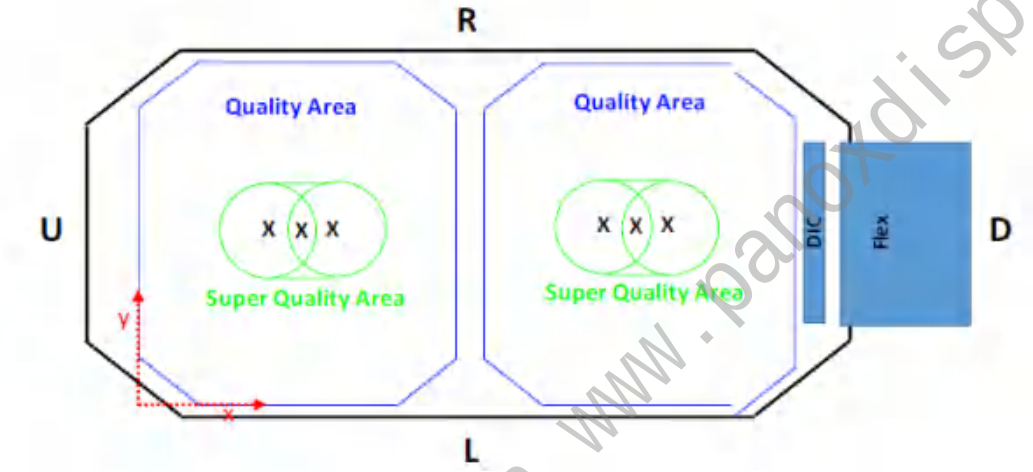


Fig. 19

Acceptable performance is listed in the table below for operation in all modes at the specified duty cycle.
Table 19

Tests	Display Primaries	LL	Nom	UL	Unit	Notes
Color Difference to white point	Gray 180	-	-	TBD	Δu'v'	Reference = W255
	Gray 127	-	-	TBD	Δu'v'	
	Gray 90	-	-	TBD	Δu'v'	
	Gray 64	-	-	TBD	Δu'v'	
	Gray 35	-	-	TBD	Δu'v'	
	Gray 25	-	-	TBD	Δu'v'	
	Gray 12	-	-	TBD	Δu'v'	

Note 11-7) Measuring systems: Konica-Minolta CA-310 or CA-410

- Temperature = 22°C (±3°C), Frame Frequency = 72Hz, LED back-light: ILED=4.4mA/Duty 100%, Environment brightness: 150±50 lx
- Measuring pattern : 1 column inversion
- Measured sample : New sample before a long term aging.
- Flicker ratio is very sensitive to measuring condition.

Note 11-8) Definition of Crosstalk

Test Method: Divide the active area of the display into 3x3 sections and display Black 0 as the background. In each measurement, two of the 3x3 sections are illuminated to display W255. Measure the brightness at the center of the panel using a measurement size less than half of the minor axis of the 3x3 center section. Conduct the three measurements as shown below.

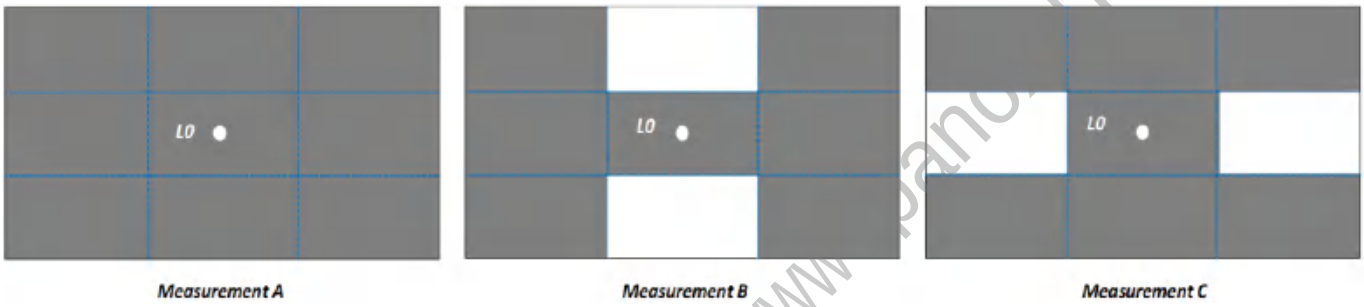


Fig. 20

Calculate the crosstalk using the following method:

$$Crosstalk\ (V) = \left|\frac{L_B - L_A}{L_A}\right| \times 100\ (\%)$$

$$Crosstalk\ (H) = \left|\frac{L_C - L_A}{L_A}\right| \times 100\ (\%)$$

12. Reliability

Table 20

No.	Test item	Conditions
1	High temperature storage test	Ta = +70°C, 240h
2	Low temperature storage test	Ta = -30°C, 240h
3	High temperature operation test	Ta = +55°C, 240h
4	Low temperature operation test	Ta = 0°C, 240h
5	High temperature and high humidity operation test	Ta = +55°C90%RH, 240h (No condensation)
6	Thermal shock, Non-operating	Ta = -30°C (20min) ~ 70°C(20min), 200 cycle
7	Electro static discharge test	Air Discharge: *8 corners and a center, ±6 kV, C=150pF, R=330Ω Contact Discharge: *7 corners and a center, ±4 kV, C=150pF, R=330Ω

Note 12-1) Ta = Ambient temperature

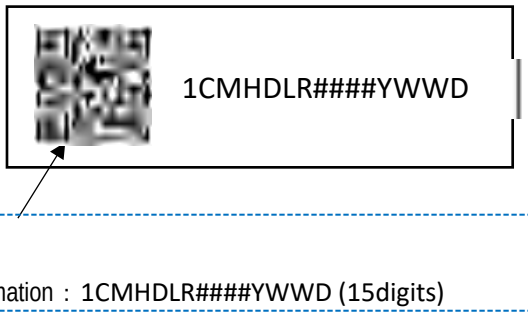
Note 12-2) Check items for other Test

In the standard condition, there shall be no practical problems that may affect the display function.

13. Indication of lot number

Attached location is shown in Fig. 27 Outline dimensions.

The lot number is shown on a label. Label Size：8mm*20mm（t≦0.1mm）



*Detail of S/N

1	: Format	/ The starting number will be “1” to indicate product
CM	: Vendor	/ Fixed value, Code assigned by AR/VR
HDL	: Part Code	/ Fixed value, Unique for part and factory
R	: Revision code	/ EVT = 1, DVT = 2, PVT = 3, MP = 4
####	: Serial number (4 digits)	/ 0001~9999
Y	: Digit Year	/ 2019 = 9, 2020 = 0, …
WW	: Digit Week	/ Week from “ISO Week Date” expressed as decimal representation (01-53)
D	: Digit Day	/ Day from “ISO Week Day” (1-7)

14. Forwarding form

(a) Piling number of cartons: 8 deep

(b) Package quality in one cartons: 120 pcs

(c) Carton size: 580mm × 365mm × 235mm

(d) Total mass of 1 carton filled with full modules: TBD

Reliability

(1)Vibration test: 1.047 Grms, Frequency range: 10~55Hz, Stroke: 1.5mm, Sweep: 10Hz~55Hz~10Hz, 1 hr each axis (X/Y/Z) in box

(2) Drop test: 60 cm height, 1 corner, 3 edges, 6 surfaces, 1 time each

Condition for storage

Environment

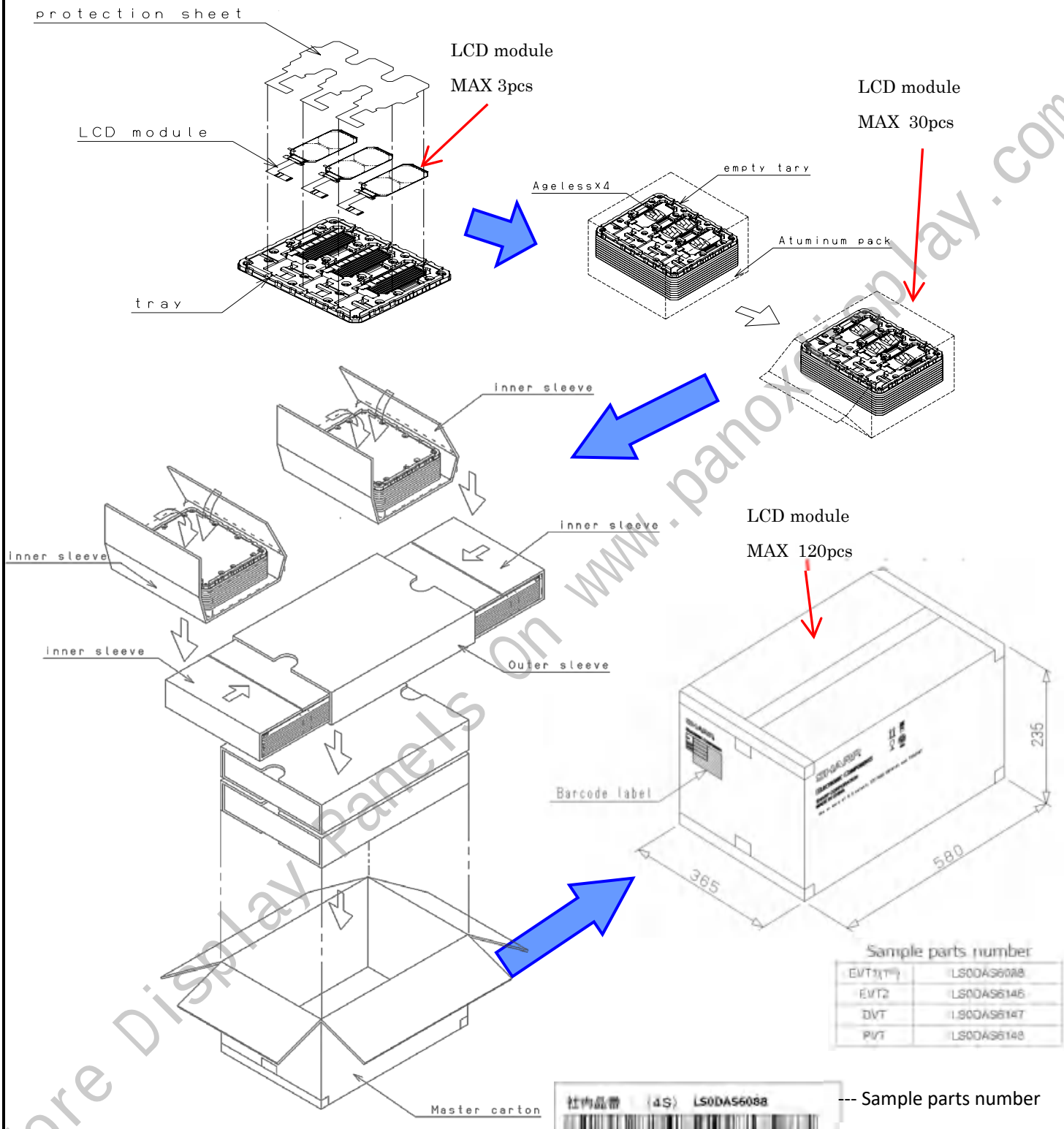
(1) Temperature: 0 to 40°C

(2) Humidity: 60%RH or less (at 40°C)

(3) Atmosphere: Harmful gas, such as acid or alkali which erodes electronic components and/or wires, must not be detected.

(4) Period: about 3 months

(5) Opening of the package: In order to prevent the LCD module from breakdown by electrostatic charges, please control the room humidity over 50%RH and open the package taking sufficient countermeasures against electrostatic charges, such as earth, etc.



Barcode label

Fig .21

15. FPC Bend Specification

15-1. Bending area of FOG:

When bending FPC, bend where specified in Condition (1) and the bend R should be more than R specified in Condition (2).

FPC is not to contact glass edge, and there should be no stress to connective area between panel and FPC.

Condition (1) FPC bend recommended area: 1.0mm-4.9mm from glass edge.

Condition (2) Minimum bend R: Inner diameter R0.6.

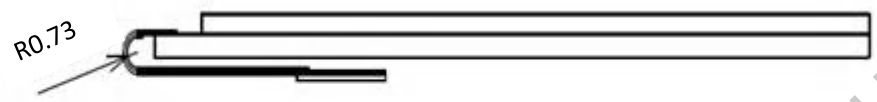


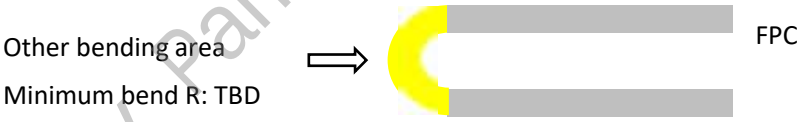
Fig. 22

[Remark 1] Do not bend backward (toward front polarizer film side).

Fig. 23

[Remark 2] Bend frequency: 10 times or less (Repeat bend condition: 180° ~ 0°)

15-2. Other bending area:



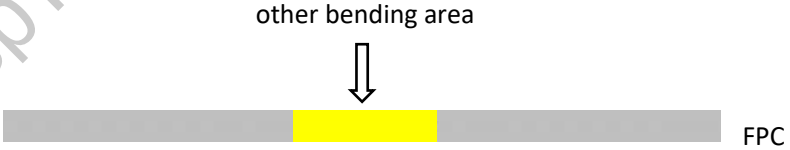


Fig. 24

[Remark 1] Bend frequency: (TBD) times or less

16. FPC Peel Strength Specification

Test device: IMADA ZP-500N

Test speed: 50mm/min

Test procedure:

1. Bending FPC by +90 degree
2. Pull up FPC to vertical direction by 50mm/min

Peel Strength: 500 gf/cm

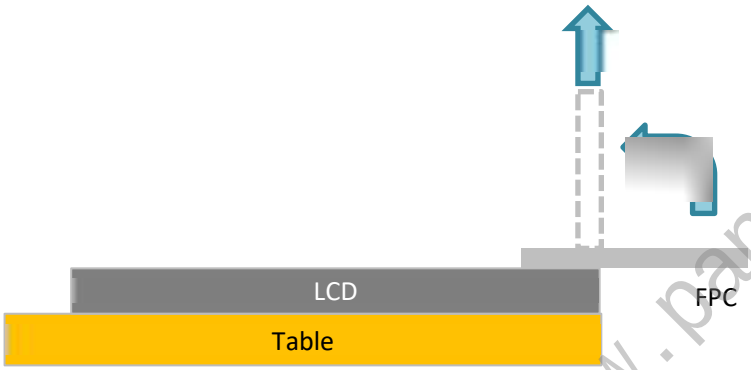


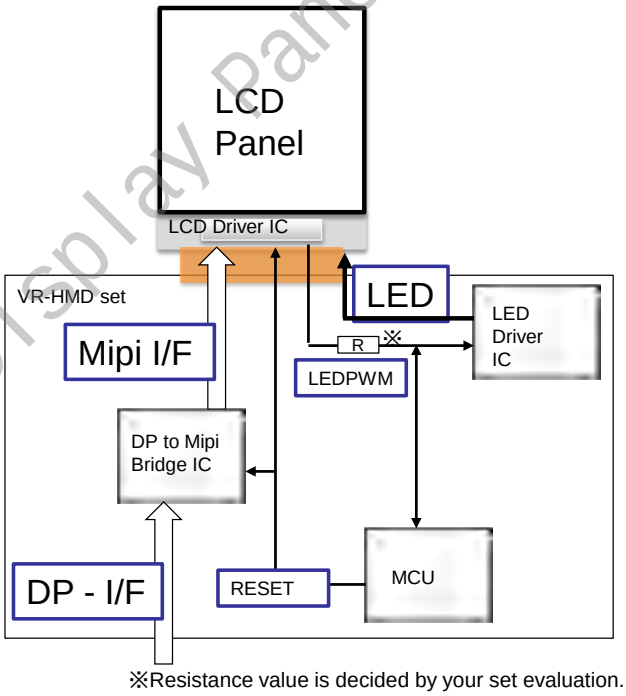
Fig. 25

16. Prevention procedure for LED heat problem

Although this phenomenon does not occur even if it operates normally,

when an unexpected abnormal condition occurs, the LED may be hot.

Precautionary counter-measures are listed as follows, so please be sure to take these methods.



※Resistance value is decided by your set evaluation.

MCU to monitor LEDPWM terminal

(PinNo.4/ BLU_PWM_2

PinNo.50/ BLU_PWM_1).

In case of continuously Hi condition

"LEDPWM = H"

↓

MCU to fix LEDPWM terminal to Low in a compulsive way.

MCU → "LEDPWM=L"

↓

To set BridgeIC• LCD Module etc

"Reset=L"

↓

To reboot

Fig.26

17. Outline dimension

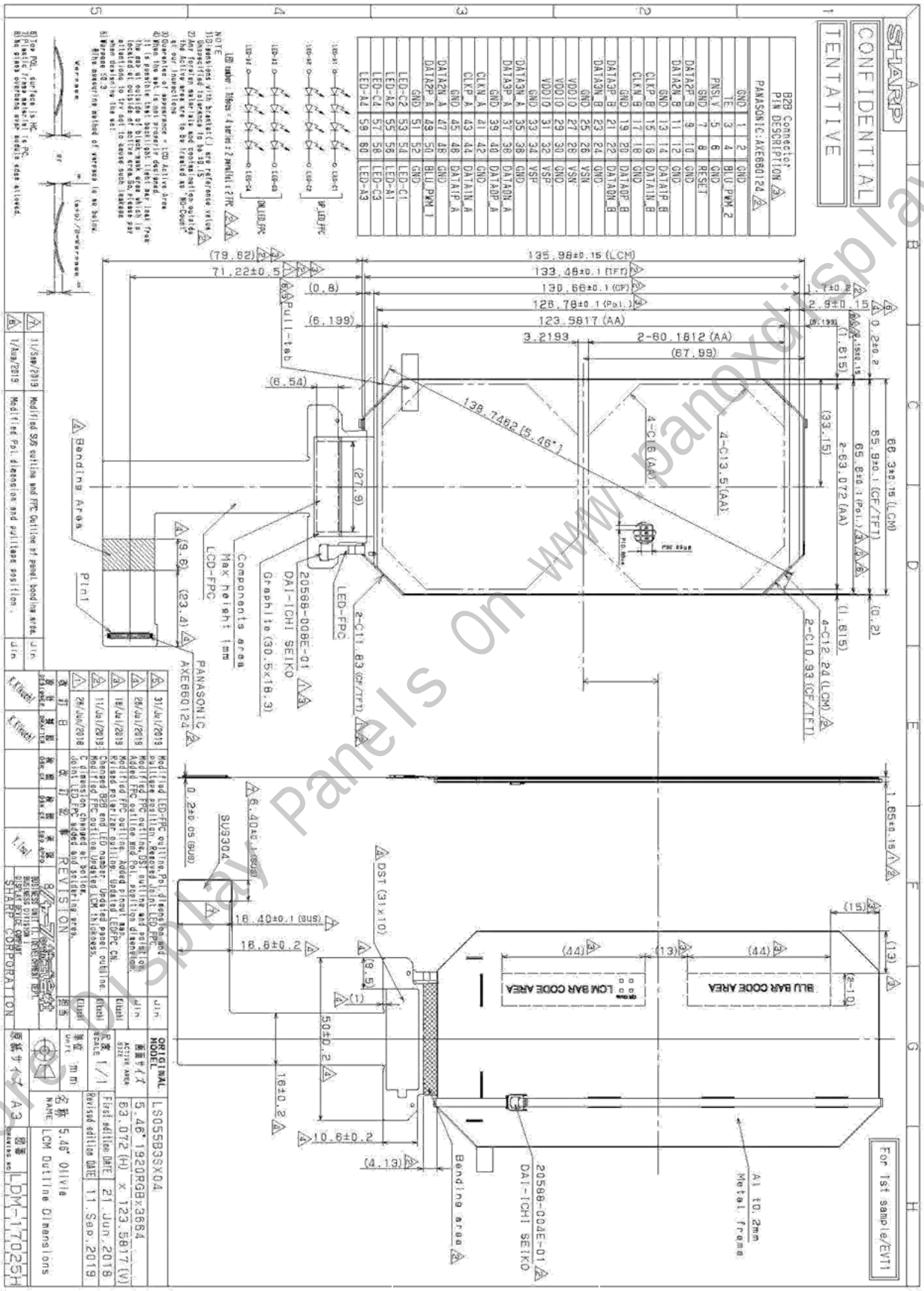


Fig. 27