Product Specification Sheet

Customer :

Model Name :

Date : **2021-5-21**

Version : **Ver 1.0**

Customer’s Approval		**CSOT**	
Signature	Date	Approved By	Date
		Reviewed By	Date
		Prepared By:	Date

Record of Revision

Version	Revise Date	Page	Content
V1.0	2021/05/21	/	-1st Version set up

Contents

1 General Description

1.1 Features

1.1.1 8.01" Flexible AMOLED Panel

1.1.2 Supported 4:3 FHD(2480×1860 pixels) Resolution

1.1.3 Green Design

1.1.4 Driving Frequency: support 60Hz ;

1.2 Specifications Summary

No.	Item	Unit	Specification	Note
1	Screen size	inch	8.01	
2	Resolution	dot	2480×1860 (SPR)	
3	Display mode	--	AMOLED	
4	Aspect Ratio	--	4:3	
5	Active area	mm	162.688*122.016	
6	Outline Dimension	mm	165.89 x 126.12	
7	Driver IC	--	RM69380	Raydium
8	Touch IC	--	FST1BA80YA2	ST
9	IC Location	--	Driver IC : COP Touch IC : FPC	
10	Touch Sensor	--	DOT	
11	Interface	--	Drive : MIPI Touch : SPI	

2 Electrical Specifications

2.1 Main FPC Pin Assignment—AMOLED Panel Input / Output Signal Interface

Connector Type : 5052744042

Pin No.	Symbol	I/O	Description	Notes
1	AVDD	P	Power Supply Input for Analog Circuit	
2	ELVSS	P	AMOLED Negative Power Supply	
3	NC1	-	- Not Connected	
4	ELVSS	P	AMOLED Negative Power Supply	
5	VCI	P	Power Supply Input for Analog Circuit	
6	ELVSS	P	AMOLED Negative Power Supply	
7	NC2	-	- Not Connected	
8	NC3	-	- Not Connected	
9	IOVCC	P	Power Supply Input for Digital Circuit	
10	GND	P	Ground	
11	VPP	P	- Not Connected or Connect to GND if not used	
12	NC4	-	- Not Connected	
13	MIPI_D2P	I	DSI-D2 Positive Differential Data Signals of MIPI	
14	AVDD_EN	O	AVDD_EN Signal for PMIC	
15	MIPI_D2N	I	DSI-D2 Negative Differential Data Signals of MIPI	
16	SWIRE	O	- Swire Signal for PMIC	
17	GND	P	Ground	
18	RESET	I	RESET FOR DIC	
19	MIPI_D1P	I	DSI-D1 Positive Differential Data Signals of MIPI	
20	ESD_FLAG	O	Error Flag For Detect IC Status	
21	MIPI_D1N	I	DSI-D1 Negative Differential Data Signals of MIPI	
22	TE	I	DIC TE Signal	
23	GND	P	Ground	
24	ID	I	Hardware Detect ID	
25	MIPI_CLKP	I	DSI-CLK Positive Differential Data Signals of MIPI	
26	TP_RST	I	Touch Reset Pin	
27	MIPI_CLKN	I	DSI-CLK Negative Differential Data Signals of MIPI	
28	TP_SPI_MOSI	I	Touch SPI Interface , Data Pin	
29	GND	P	Ground	
30	TP_SPI_MISO	I/O	Touch SPI Interface , Data Pin	
31	MIPI_D0P	I/O	DSI-D0 Positive Differential Data Signals of MIPI	
32	TP_SPI_CS	I/O	Touch SPI Interface , Chip Select	

Pin No.	Symbol	I/O	Description	Notes
33	MIPI_D0N	I/O	DSI-D0 Negative Differential Data Signals of MIPI	
34	TP_SPI_SCK	I/O	Touch SPI Interface , Clock Pin	
35	GND	P	Ground	
36	TP_INT	I/O	TP Interrupt	
37	MIPI_D3P	I	DSI-D3 Positive Differential Data Signals of MIPI	
38	TP_1V8	P	Power Supply Input for TP Digital Circuit	
39	MIPI_D3N	I	DSI-D3 Negative Differential Data Signals of MIPI	
40	TP_3V3	P	Power Supply Input for TP Analog Circuit	
41	ELVDD	P	AMOLED Positive Power Supply	
42	ELVDD	P	AMOLED Positive Power Supply	
43	ELVDD	P	AMOLED Positive Power Supply	
44	GND	P	Ground	
45	GND	P	Ground	
46	GND	P	Ground	

Note : I (Input); O (Output); P (Power); I/O (Input /Output);

2.2 Absolute Maximum Ratings

2.2.1 Module Panel Absolute Maximum Ratings

Item	Symbol	Value		Unit	Remark
		Min.	Max.		
Digital Power Supply	VDDIO	-0.3	3.6	V	Note1
Analog Power Supply	VCI	-0.3	5.5	V	
Power Supply For Analog Circuit.	AVDD	-0.3	9.0	V	
ELVDD Power Supply	ELVDD	-0.3	6	V	Note2
ELVSS Power Supply	ELVSS	-9.5	0.3	V	
Operating Temperature(Ambient)	Top	-	-	℃	Refer to RA test result
Storage Temperature(Ambient)	Tstg	-	-	℃	
Humidity	Hstg	-	-	%RH	

Note1 : If the module exceeds the absolute maximum ratings, it may be damaged permanently.

Note2 : PMIC （NT50379WHB） Supply ;

3 Electrical Characteristics

3.1 Display DC Characteristics &Current Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
ELVDD	ELVDD	-	4.55	4.60	4.65	V	Controlled By DDIC VINA=VINP=2.9V to 4.8V; No load
ELVSS	ELVSS	-	-3.27	Normal : -3.30	-3.33	V	
			-4.04	HBM : -4.00	-3.96		
AVDD	AVDD	-	7.52	7.60	7.68	V	
VCI	VCI	-	2.65	3.00	4.80	V	-
VDDIO	VDDIO	-	1.65	1.80	1.95	V	-
Current Consumption	AVDD	Frame f=60Hz Normal/430nits White pattern	34.69	38.08	40.92	mA	Note1
	VCI		10.31	10.58	10.92	mA	
	VDDIO		114.6	117.97	121.86	mA	
	ELVDD		423.25	451.78	451.78	mA	
	ELVSS		-423.01	423.01	451.46	mA	
	AVDD	Frame f=60Hz HBM/600nits White pattern	34.74	37.48	40.65	mA	
	VCI		10.23	10.52	10.93	mA	
	VDDIO		115.03	118.73	122.68	mA	
	ELVDD		597.62	619.09	635.23	mA	
	ELVSS		597.41	618.89	635.15	mA	

Note1 : Average of 30pcs Module Panel

3.2 Touch DC Characteristics &Current Consumption

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
AVDD	TP_VDD	2.7	3.3	3.6	V	
VDDIO	TP_VDDIO	1.65	1.8	1.95	V	
Power Consumption	Active With no finger	72.0	77.3	78.9	mW	Note1
	Active With one finger	81.5	81.7	81.9	mW	
	Idle Mode	5.7	9.9	12.3	mW	
	Sleep Mode	0.4	0.4	0.4	mW	
	Gesture Mode	5.0	7.2	8.4	mW	

Note1： Average of 30pcs Module Panel

3.3 Touch SNRpp

	Pattern	Signal (Peak)	Noise (Peak) note1	SNRpp
远端	黑画面	1017.8	35.4	29.2
	白画面	976	17.25	35.0
	1*1 zebra	989.4	40.4	27.8
	3*3 zebra	1006.4	33.6	29.5
	4*4 zebra	1016	41.6	27.8
	10W10B (自选)	1005	46	26.8
	Note1：Noise 为 3minute 无手指触摸全屏最大 noise			
中间	Pattern	Signal (Peak)	Noise (Peak) note1	SNRpp
	黑画面	967	35.4	28.7
	白画面	1004.3	17.25	35.3
	1*1 zebra	998	40.4	27.9
	3*3 zebra	1013.8	33.6	29.6
	4*4 zebra	1045.5	41.6	28.0
	10W10B (自选)	1047.4	46	27.1
	Note1			
近端	Pattern	Signal (Peak)	Noise (Peak) note1	SNRpp
	黑画面	1147.2	35.4	30.2
	白画面	1144	17.25	36.4
	1*1 zebra	1144	40.4	29.0
	3*3 zebra	1166	33.6	30.8
	4*4 zebra	1130.4	41.6	28.7
	10W10B (自选)	1160	46	28.0
	Note1			

Note1： Average of 5pcs Module Panel

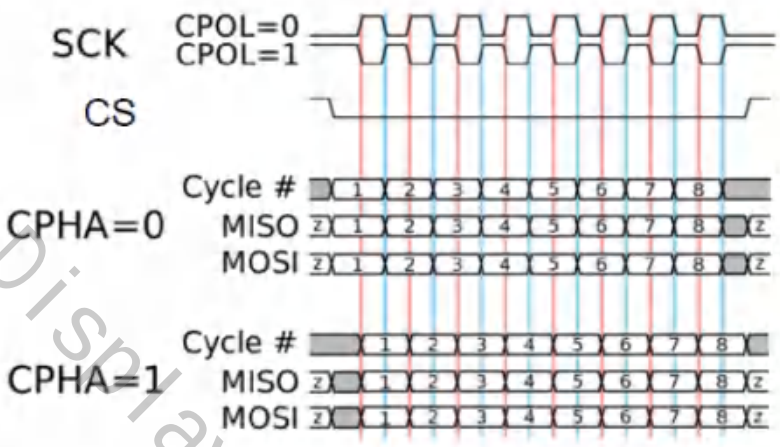
3.4 SPI Interface Characteristic

3.4.1 Data to Clock Timing Definitions

The SPI timing modes are defined by CPHA and CPOL. FST device supports Mode 0 of SPI where the CPOL=0 and CPHA=0. The clocking diagram of this mode is shown below. The device always operates in mode 0.

At CPOL=0 the base value of the clock is zero

For CPHA=0, data is captured on the clock's rising edge (low→high transition) and data is propagated on a falling edge (high→low clock transition).



Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

3.4.2 SPI Transactions

All transactions that are supported through the I2C interface are also supported by SPI interface

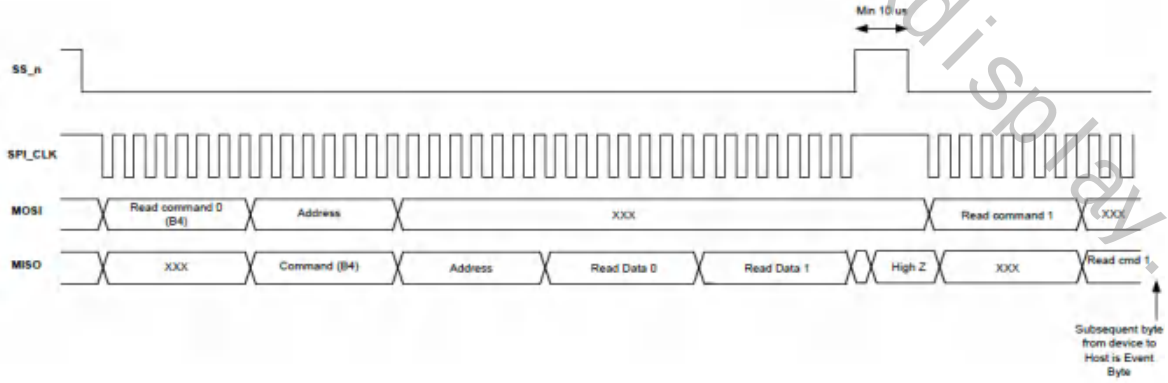
The transactions list is as follows:

- Commands (Read B4 command or Write B6 command with zero or more parameters)
- Register access through command
- Configuration during boot up • Flash loading during boot up

3.4.3 SPI Read

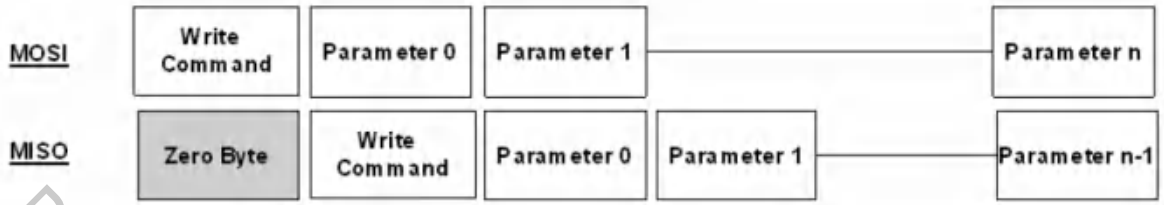
The SPI read transaction diagram is shown below.

The SPI read timing diagram is shown below. Note that there is one dummy byte before read data. The following steps need to be followed for the register read through the SPI.

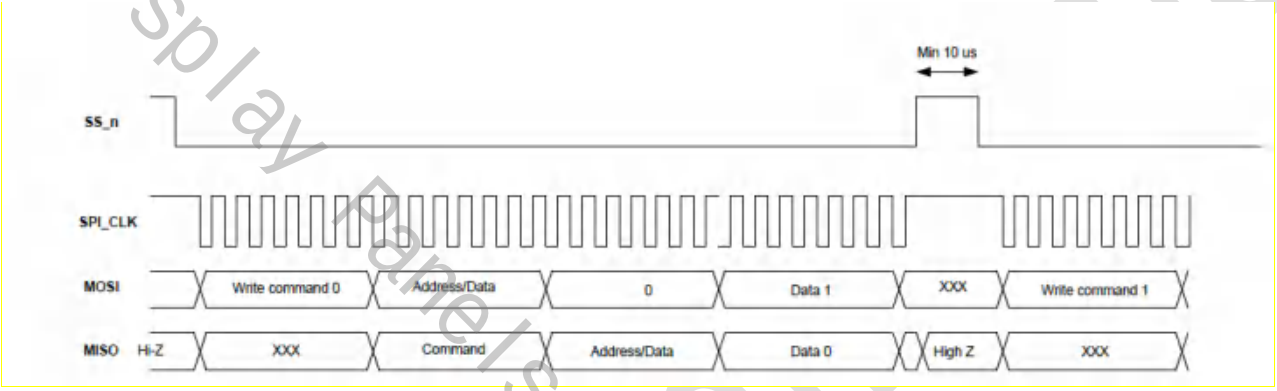


3.4.4 SPI Write

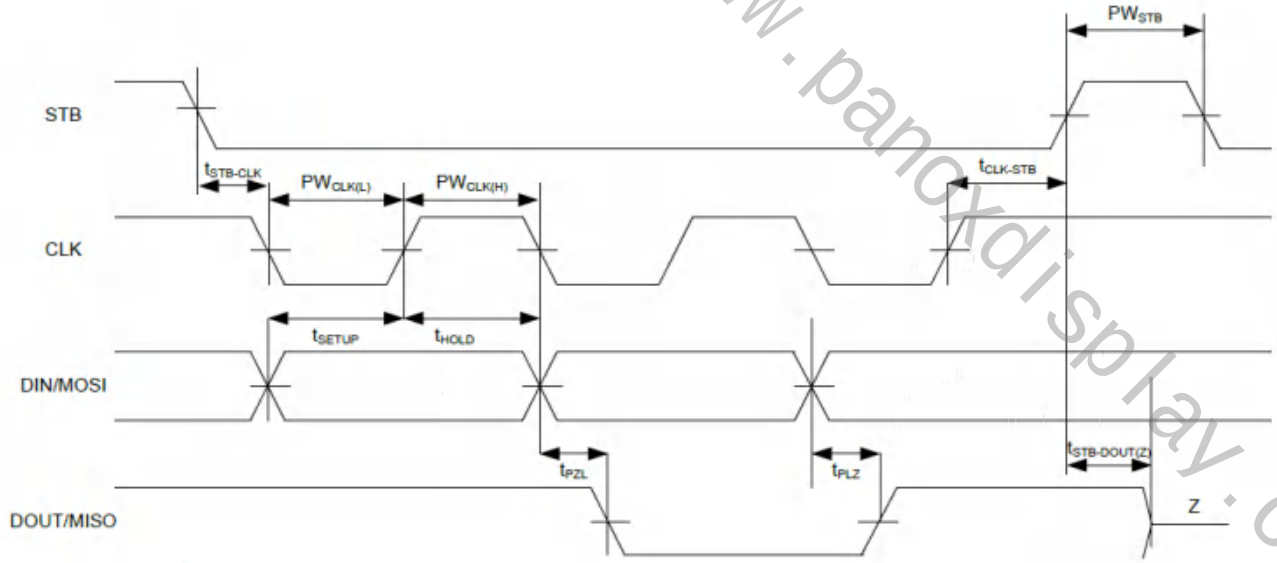
The SPI write transaction diagram is shown below.



The SPI write timing diagram is shown below. The following steps need to be followed for the register write through the SPI.



3.4.5 SPI timing definition



Symbol	Description	Timing			Unit
		Min	Typ	Max	
Fmax	Maximum CLK frequency (100pF load on Data, Clk, Stb)		12		MHz
$t_{STB-CLK}$	STB low to first clock edge	1	-	-	us
$PW_{CLK(L)}$	Clock low period	166	500	-	ns
$PW_{CLK(H)}$	Clock high period	166	500	-	ns
t_{SETUP}	Time from changing MOSI to CLK, Data set up time	20	-	-	ns
t_{HOLD}	Time from CLK to changing MOSI, Data hold time	20	-	-	ns
t_{PZL}	Launch clock to MISO data valid	-	-	330	ns
t_{PLZ}	Launch clock to MISO data valid	-	-	330	ns
$t_{CLK-STB}$	Last clock edge to STB high	1	-	-	us
PW_{STB}	STB high period	10	-	-	us
$t_{STB-DOUT(Z)}$	STB high to tri-state on MISO	1	-	-	us

1. *There is a timing dependency between the last SPI_CLK and the de-assertion of the SPI_CS. At least one internal oscillator clock cycle is recommended (i.e. ~250ns). Timings based on 1MHz.*

3.5 MIPI Interface Characteristic

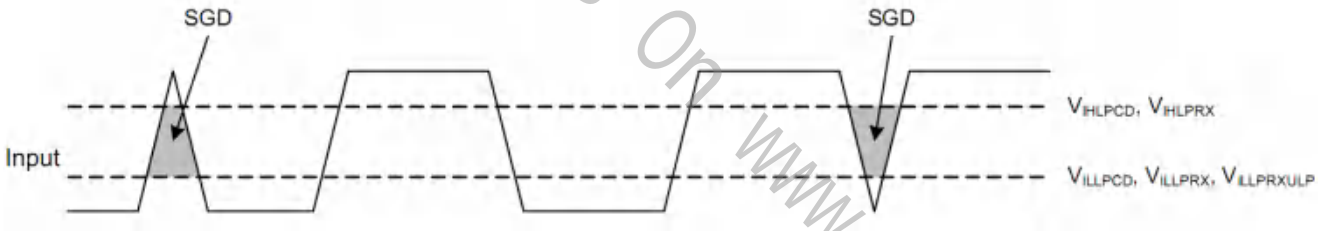
3.5.1 DC Characteristics for D-PHY LP Mode

Parameter	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level input voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level input voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input voltage	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input voltage	I_{IL}	LP-CD, LP-RX	-10	-	-	μ
Input pulse rejection	SGD	DSI2-CLK+/-, DSI2-Dn+/-	-	-	300	Vps

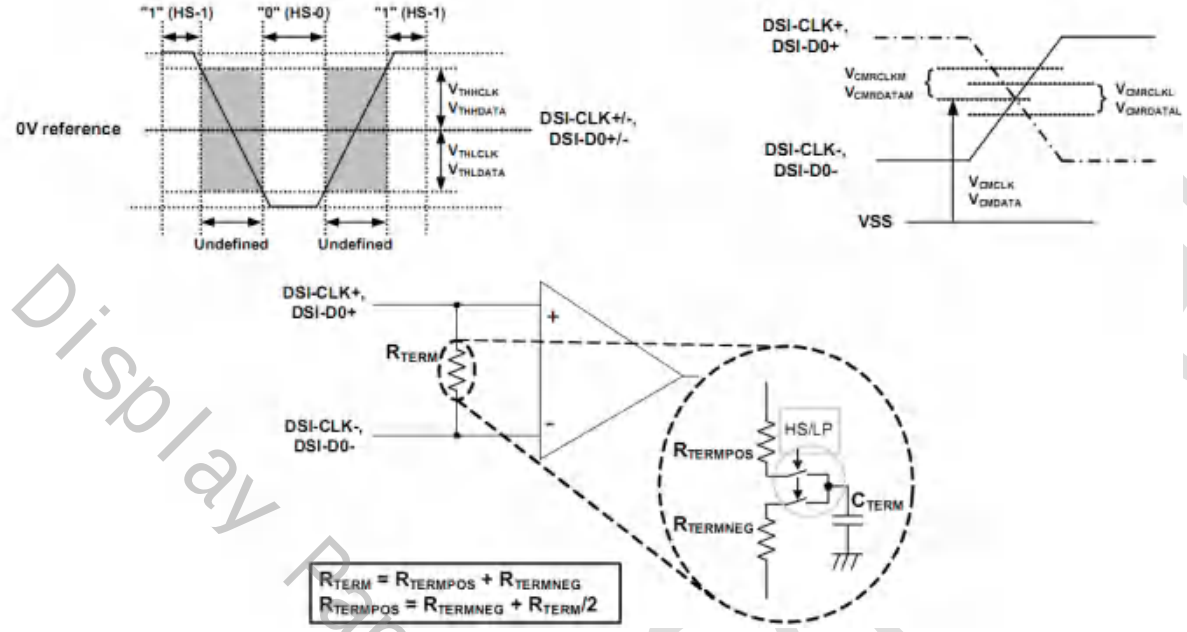
Note 1) VDDI=1.65~1.95V, DVSS=AVSS=VSSR=VSSB=VSSAM=0V, Ta= -30 to 70 ºC (to +85 ºC no damage).

Note 2) DSI2 high speed is off.

Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.



3.5.2 DC Characteristics for D-PHY HS Mode



Parameter	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
Input Voltage Common Mode Range	V_{CMCLK} V_{CMDATA}	DSI2-CLK+/-, DSI2-Dn+/- (Note2, 3)	70	-	330	mV
Input Voltage Common Mode Variation (≤ 450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI2-CLK+/-, DSI2-Dn+/- (Note4)	-50	-	50	mV
Input Voltage Common Mode Variation (≥ 450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI2-CLK+/-, DSI2-Dn+/-	-	-	100	mV
Low-level Differential Input Voltage Threshold	V_{THLCLK} $V_{THLDATA}$	DSI2-CLK+/-, DSI2-Dn+/-	-70	-	-	mV
High-level Differential Input Voltage Threshold	V_{THHCLK} $V_{THHDATA}$	DSI2-CLK+/-, DSI2-Dn+/-	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI2-CLK+/-, DSI2-Dn+/-	-40		-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI2-CLK+/-, DSI2-Dn+/-	-	-	460	mV
Differential Input Termination Resistor	R_{TERM}	DSI2-CLK+/-, DSI2-Dn+/-	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI2-CLK+/-, DSI2-Dn+/-	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI2-CLK+/-, DSI2-Dn+/-	-	-	14	pF

Note 1) VDDI=1.65~1.95V, DVSS=AVSS=VSSR=VSSB=VSSAM=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).

Note 2) Includes 50mV (-50mV to 50mV) ground difference.

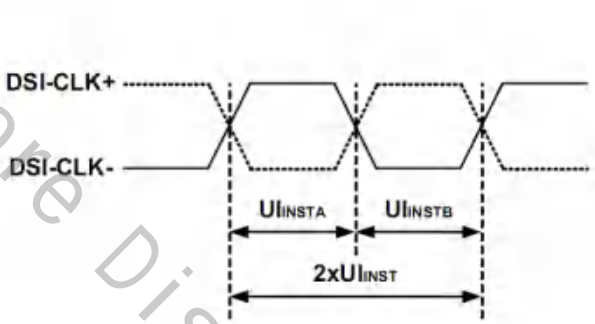
Note 3) Without VCMRCLKM / VCMRDATAM .

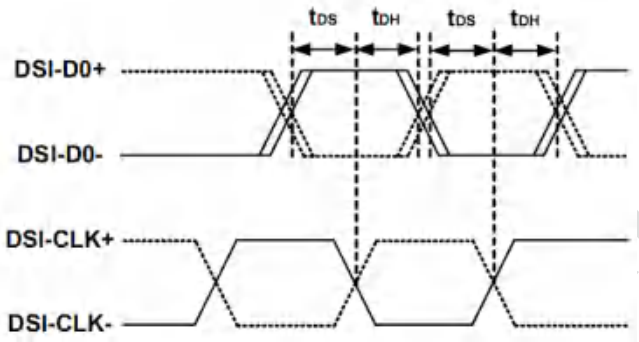
Note 4) Without 50mV (-50mV to 50mV) ground difference.

Note 5) Dn=D0, D1, D2 and D3.

3.5.3 MIPI DSI2 Timing Characteristics

3.5.3.1 D-PHY High Speed Mode





Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
DSI2-CLK+/-	$2xUI_{INST}$	Double UI Instantaneous	1.67	-	4	ns	4 Lane (Note 2)
DSI2-CLK+/-	UI_{INSTA} UI_{INSTB}	UI Instantaneous Halfs ($UI = UI_{INSTA} = UI_{INSTB}$)	0.83	-	2	ns	4 Lane (Note 2)
DSI2-Dn+/-	tDS	Data to Clock Setup Time	0.15xUI	-	-	ps	Note 1, 3
			0.2xUI		-		Note 1, 4
DSI2-Dn+/-	tDH	Data to Clock Hold Time	0.15xUI	-	-	ps	Note 1, 3
			0.2xUI		-		Note 1, 4
DSI2-CLK+/- DSI2-Dn+/-	tDRTCLK	Differential Rise Time for Clock	-	-	0.3xUI	ps	Note 1, 5
			-	-	0.35xUI		Note 1, 6
			100	-	-		Note 1, 7

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is TBD Gbps for 24-bit data format which support to 1440RGBx3360 resolution.

Note 3) Total setup and hole window for receiver of 0.3 UIINST when D-PHY is supporting maximum data rate = 1Gbps.*

Note 4) Total setup and hole window for receiver of 0.4 UIINST when D-PHY is supporting maximum data rate > 1Gbps.*

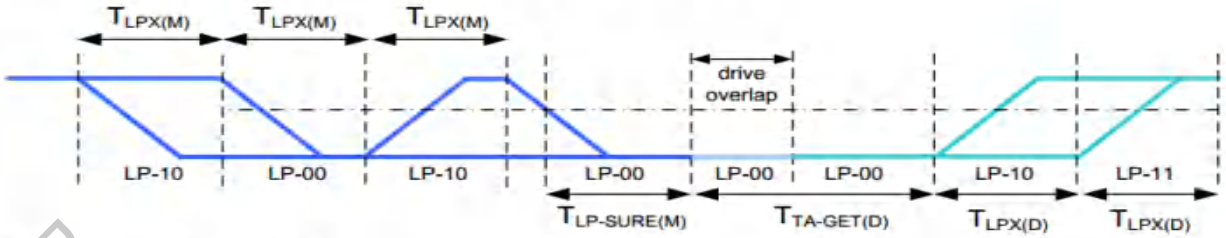
Note 5) Applicable when operating at HS bit rates ≤ 1 Gb ps (UI ≥ 1 ns).

Note 6) Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).

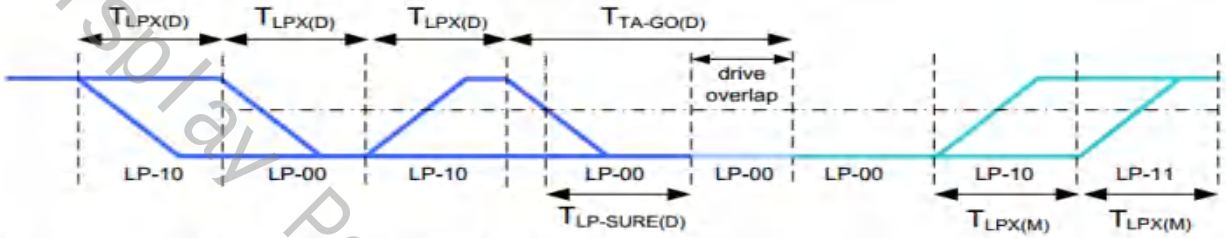
Note 7) Applicable for all HS b it rates. However, to avoid excessive radiation, b it rates ≤ 1 Gb ps (UI ≥ 1 ns), should not use values below 150 ps.

3.5.3.2 D-PHY Low Power Mode

■ Bus Turnaround Procedure (From MPU to display module)



Bus turnaround (BAT) timing



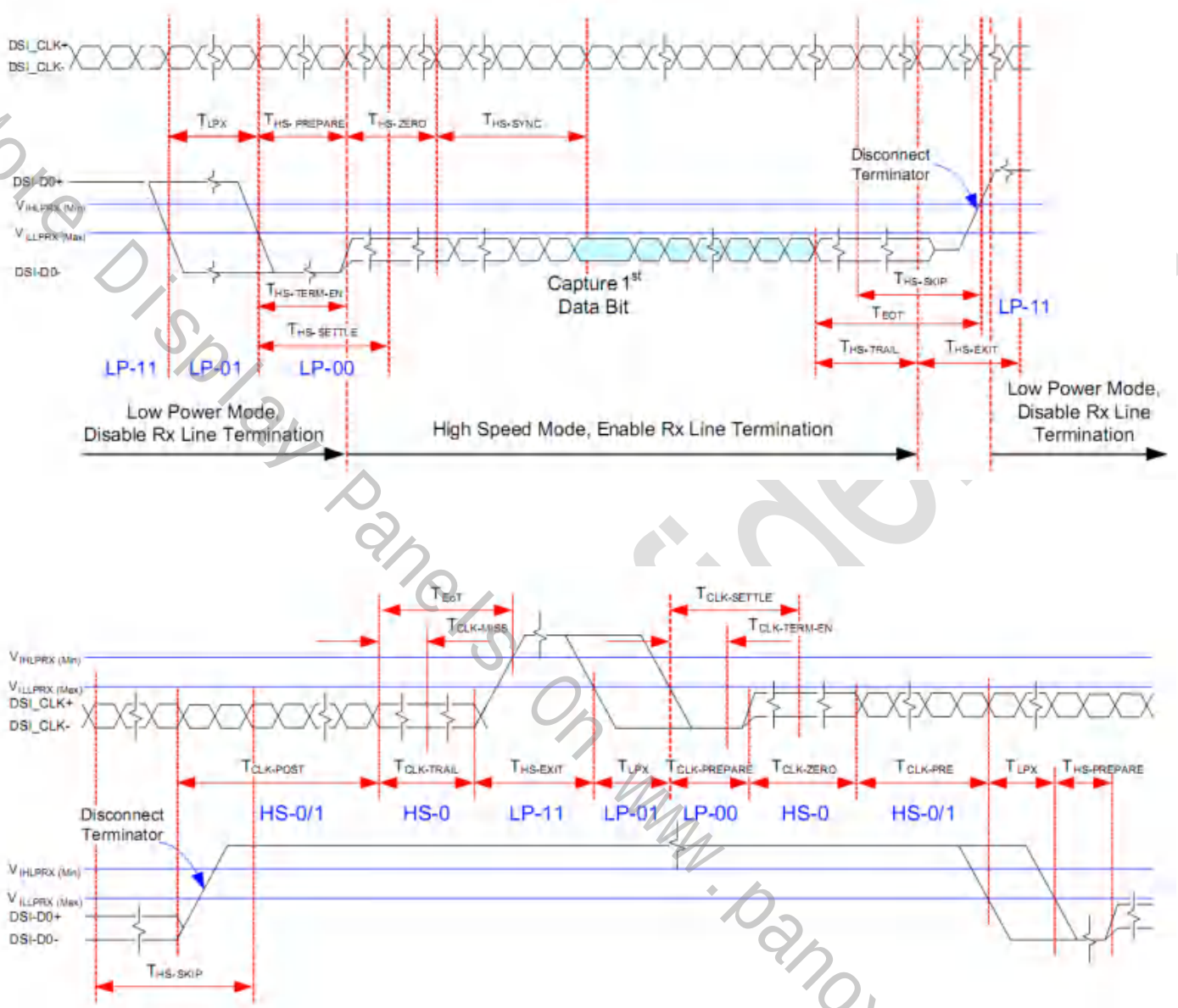
Bus turnaround (BAT) from display module to MPU timing

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
DSI2-D0+/-	T_{LPXM}	Transmitted length of any Low-Power state period of MCU to display module	50	-	150	ns	1,2
DSI2-D0+/-	$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX(M)		2*TLPX(M)	ns	2
DSI2-D0+/-	T_{LPXD}	Transmitted length of any Low state period of display module to MCU	50	-	150	ns	1,2
DSI2-D0+/-	$T_{TA-SURED}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPXD}	-	$2xT_{LPXD}$	ns	2
DSI2-D0+/-	$T_{TA-GETD}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround	-	$5xT_{LPXD}$	-	ns	2
DSI2-D0+/-	T_{TA-GOD}	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	-	$4xT_{LPXd}$	-	ns	2

Note 1) TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

Note 2) Transmitter-specific parameter.

3.5.3.3 D-PHY DSI2 Bursts



Parameter	Description	Min	Typ	Max	Unit
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL .	60ns + 52*UI			ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	300			ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	Time for Dn to reach VTERM-EN	38		ns
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	95		ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	Time for Dn to reach VTERM-EN		35 ns +4*UI	
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns

Parameter	Description	Min	Typ	Max	Unit
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns
t3-PREPARE	Time that the transmitter drivers the 3-wire LP-000 line state immediately before the start of the HS transmission.	38		95	ns
t3-TERM-EN	Time for the slave to enable the HS line termination, starting from the time point when the A, B and C wire cross VIL_MAX.	Note 5		38	ns
t3-SETTLE	Time interval during with the HS receiver should ignore any HS transitions on the line, starting from the beginning of t3-PREPARE.	95			
tHS-EXIT	Time that the transmitter drivers LP-111 following a HS burst.	100			
tLPRX	Transmitted length of any low-power state period	50			

Note 1) tLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

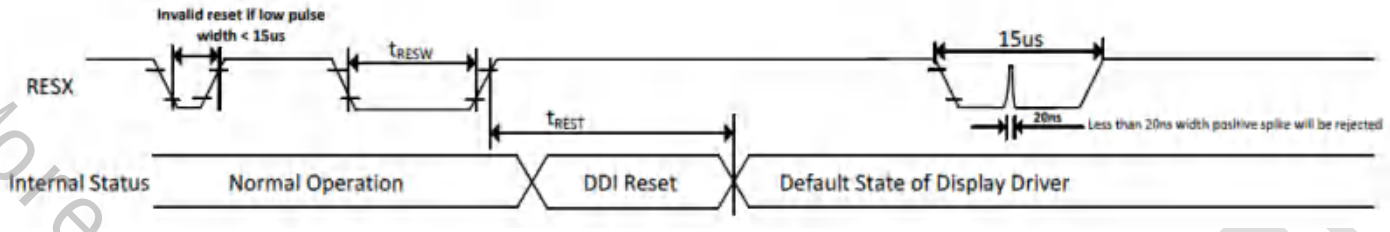
Note 2) Transmitter-specific parameter.

Note 3) Receiver-specific parameter.

Note 4) The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.

Note 5) The receiver termination impedances shall not be enable until the single-ended voltages on all of A, B and C fall below VTERM-EN.

3.5.4 Reset Input Timing



Signal	Symbol	Parameter	Min	Typ	Max	Unit	Note
RESX	tRESW	Reset "L" pulse width	15	-	-	μs	1. Shorter than 5us, Reset rejected 2. Longer than 15us, IC reset 3. Between 5us and 15us, It depends on voltage and temperature condition.
	tREST	Reset complete time	-	-	10	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5μs	*Reset Rejected*
Longer than 30μs	*Reset*
Between 5μs and 30μs	*Reset Start*

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In– mode) and then return to Default condition for H/W reset.

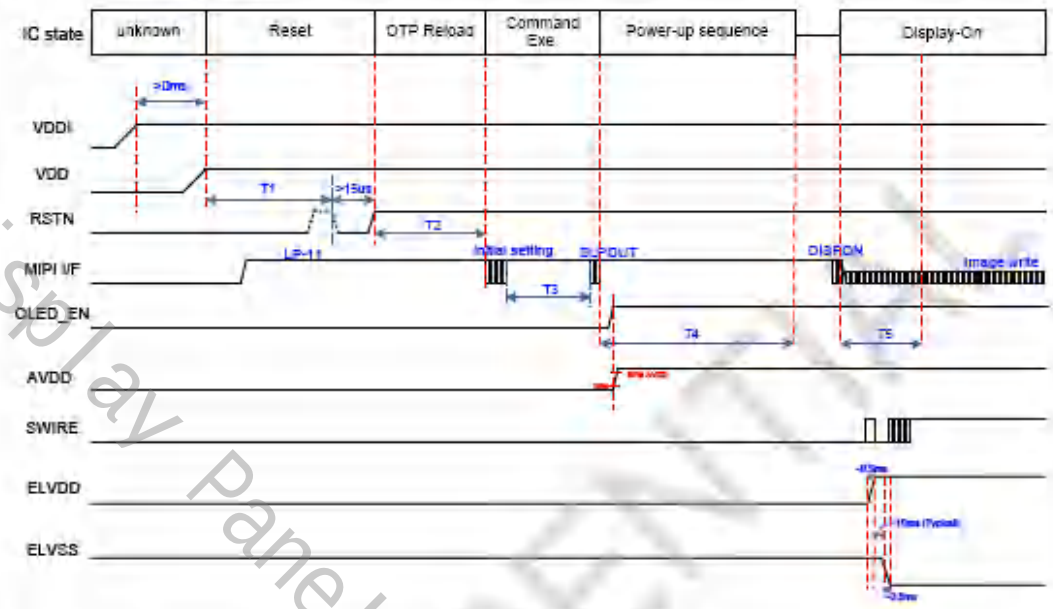
Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

3.6 Power Sequence

3.6.1 Power On sequence

❖ **Power On Sequence**



◆ **Timing Specification of Power On Sequence**

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	10	-	-	ms	Effective hardware reset period
T2	10	-	-	ms	OTP reload time
T3	0	-	-	ms	Initial code input finish to SLPOUT command input
T4	-	96	-	ms	Normal power-up sequence
T5	2	-	-	VS	Display-On Blanking region

Notes: VS means the time period of a complete display frame and are approximately 16ms if internal display timing is used.

3.6.2 Touch Power On sequence

There is no restriction of power sequence. However it is recommended to turn on 1.8V earlier than 3.3V as this allows the digital core, I2C mode and firmware to be ready before AFE (charge pump and analog voltage references). But even if 1.8V and 3.3V turn on together or 3.3V turns on earlier than 1.8V, there will be no malfunction.

Fingertip touch screen controller is sharing GPI2 pin for I2C /SPI mode selection during V1V8 power On and system reset.

Name	I2C Function	SPI Function	GPI or digital input	Reset State
GPI2/MODE	'1' for I2C during Reset	'0' for SPI during Reset	GPI2	MODE

The VCM1V65 pin will be 1.65V once the device is initialized and also VPUMP voltage will be 3.3V or configured output (6V).

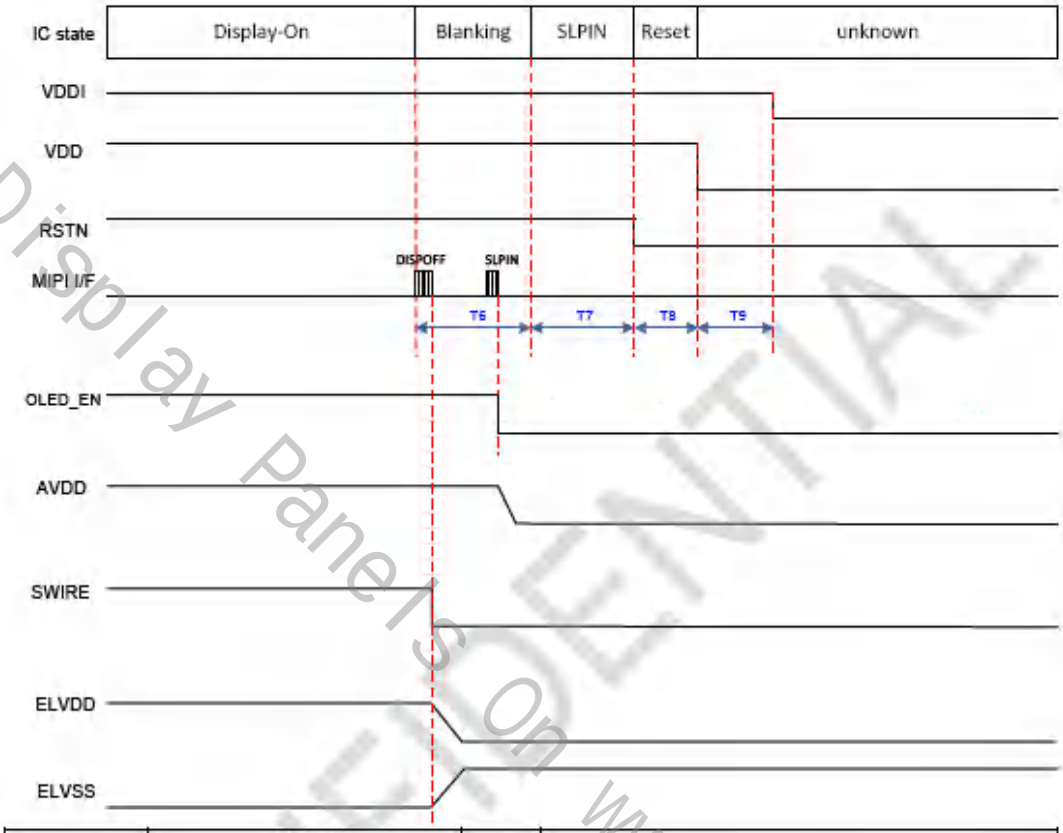
When powering up the FTM device up or down, system design should ensure that the voltages on the signal pins in the Absolute Maximum Ratings Table are observed. Failure to follow this requirement may lead to unreliable operation of or damage to the device. Open drain signals are high impedance on power up and will transition to high once the pull up resistor voltage is present.
The GPIO and GPI pins are default input state on power up and are pulled high internally and so these do not consume any leakage current.

Double Power：VDD and VDDIO

3.6.3 Power Off sequence

The power off sequence are shown below figures.

❖ **Power Off Sequence**



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T6	2	-	-	VS	Display-Off blanking region
T7	1	-	-	VS	Blanking region
T8	1	-	-	ms	Effective hardware reset period
T9	2	-	-	ms	Power off period

Notes: VS means the time period of a complete display frame and are approximately 16ms if internal display timing is used.

3.7 Touch Electrical Test Item`

3.7.1 Test Item

Test Item	Note
Init	TIC connection, F/W upgrade test
Pin Test	RST/INT pin connection test
Ito Test	Short test , Adjacent deviation test
Auto Tune	Capacity value calibration test
Mutual Check	Mutual capacity test, noise at power on test
Self Check	Self capacity test
Check Lockdown	Lockdown information test

3.7.2 Test Environment

1. Operator must wear the anti-ESD ring before handing.

2. The grounding condition of test fixture is well.

3. The plasma fan must be kept open during the test.

4. Do not touch the screen surface during the test, such as the fingers, the suction nozzle.

3.8 OP manual

3.8.1.Model Information

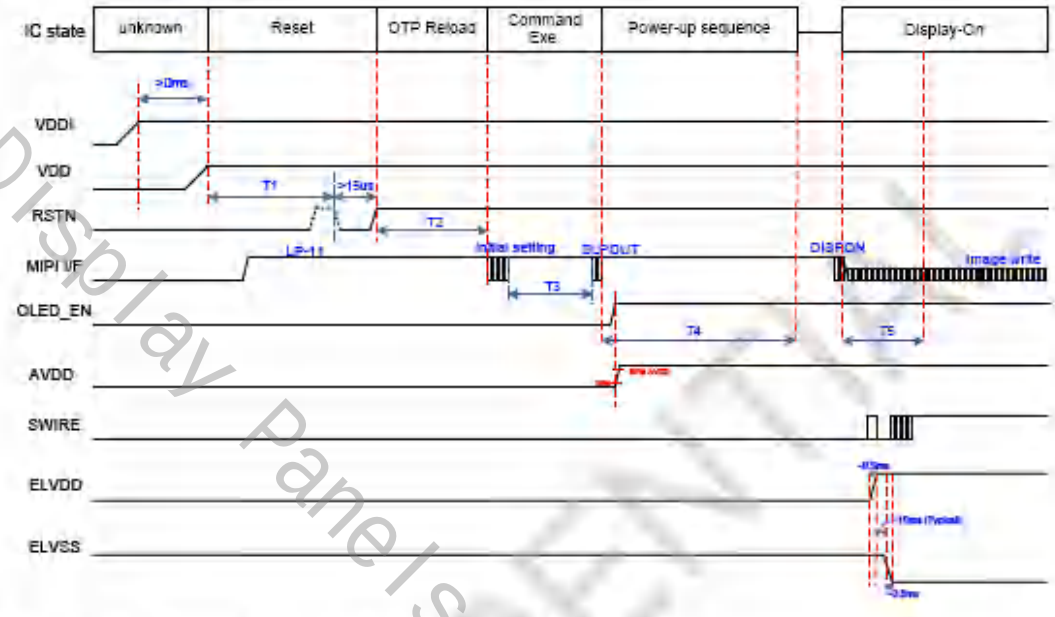
Feature		Spec	Remark
Display Spec	Screen Size (inch)	8.01	
	Display Mode	AMOLED	
	Resolution(dot)	2480x1860(WxH)	SPR
	Color Depth	16.7M	
	Interface	MIPI 4 LANE	
Electronic	Driver IC	RM69380 (COG)	
	Power IC	NT50379	
MIPI Speed	---	822 Mbps	
Frequency		60Hz	
Input Voltage (TYP.)	VCI	3.0V	
	VDDIO	1.8V	
	AVDD	7.6V	Ctrl by DDIC Via Swire
	ELVDD	4.6V	
	ELVSS	HBM:-4.0V Normal Mode:-3.3V AOD:-2V	

3.8.2 Operation Sequence

3.8.2.1 Power On Sequence

提供 sequence 和上电时序图，并备注各信号间 Delay 时间要求，如下：

❖ **Power On Sequence**



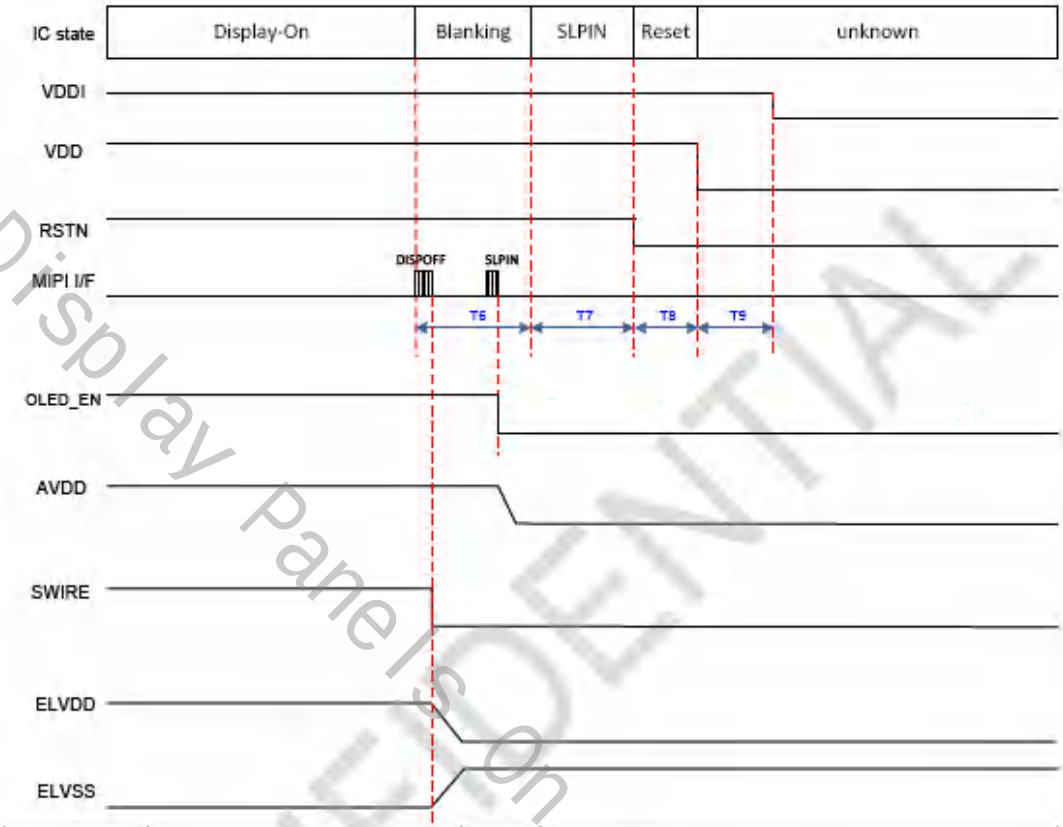
◆ **Timing Specification of Power On Sequence**

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	10	-	-	ms	Effective hardware reset period
T2	10	-	-	ms	OTP reload time
T3	0	-	-	ms	Initial code input finish to SLPOUT command input
T4	-	96	-	ms	Normal power-up sequence
T5	2	-	-	VS	Display-On Blanking region

Notes: VS means the time period of a complete display frame and are approximately 16ms if internal display timing is used.

3.8.2.2 Power off Sequence

❖ **Power Off Sequence**



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T6	2	-	-	VS	Display-Off blanking region
T7	1	-	-	VS	Blanking region
T8	1	-	-	ms	Effective hardware reset period
T9	2	-	-	ms	Power off period

Notes: VS means the time period of a complete display frame and are approximately 16ms if internal display timing is used.

3.8.2.3 Sleep in Sequence

Order	Sequence	Remark
1	Display On Status	
2	Display Off(28h)	
3	Wait >40ms	
4	Sleep In (10h)	
5	Sleep In Status	

3.8.2.4 Sleep Out Sequence

Order	Sequence	Remark
1	Sleep In Status	
2	Sleep Out (11h)	
3	Wait>100ms	
4	Display On (29h)	
5	Display On Status	

3.8.2.5.Deep Standby On/Off

Order	Sequence	Remark
1	Display Off (28h)	
2	Sleep In (10h)	
3	Wait >100ms	
4	Enter Deep Standby Mode(4Fh=0x01)	
5	MIPI Drive to LP-00 or Enter ULPM	
6	In Deep Standby Mode	

3.8.2.6 双击唤醒上电时序

熄屏模式下，TIC 一直处于 Idle 或 Sleep 模式，均在上电状态，双击后，上报双击事件，由系统点亮屏幕，屏幕上电时序参考 3.1。

3.8.2.7.双击唤醒下电时序

检测到无点击，屏幕按照 3.2 power off 时序下电，TIC 将一直处于工作模式。

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T10	-	-	-	ms	可由整机系统设定
T11	500	-	-	ms	可由整机系统设定
T12	-	-	-	ms	可由整机系统设定

3.8.3.Common Setting

3.8.3.1 VESA On/Off

Register	R/W	Values	Description
0xFE	W	0x00	Page 00
0xFA	W	0x01	VESA On
0xFA	W	0x01	VESA Off

3.8.3.2 TE OUT(Vsync On/Off)

Register	R/W	Values	Description
0x3500	W	00h	TE On And Output V-sync
	W	01h	TE On And Output H-sync
0x3400	W		TE Off

3.8.3.3 HBM & Dimming On/Off

Command	R/W	Values	Description
0xFE	W	0x00	Page 00
0x51	W	0x07,0xFF	Normal Mode
0x51	W	0x0F,0xFF	High Brightness Mode

Dimming Function

Command	R/W	Values	Description
0xFE	W	0x00	Page 00
0x53	W	0x20	Dimming Off
0x53	W	0x28	Dimming On

3.8.3.4 Error Flag 寄存器设定

Command	R/W	Values	Description
0xFE	W	0x40	Page 40
0x5D	W	0x00	Normal L
0x5D	W	0x80	Normal H

3.8.3.5 Demura On / Demura Off

Demura On

Command	R/W	Values	Description
0xFE	W	0x22	Page 22
0x5F	W	0x00	Demura On
0xFE	W	0x64	Page 64
0x24	W	0x00	Deburn In On

Demura Off

Command	R/W	Values	Description
0xFE	W	0x22	Page 22
0x5F	W	0x02	Demura Off
0xFE	W	0x64	Page 64
0x24	W	0x01	Deburn In Off

3.8.3.6 Round On/Off

Round On

Command	R/W	Values	Description
0xFE	W	0x40	Page 40
0x8A	W	0x82	Round On

Round Off

Command	R/W	Values	Description
0xFE	W	0x40	Page 40
0x8A	W	0x02	Round Off

3.8.4 AOD Mode

3.8.4.1 AOD On Sequence(Normal→AOD)

Command	R/W	Values	Description
0xFE	W	0x00	Page 00
0x39	W		Enter AOD Mode

3.8.4.2 AOD Off Sequence(AOD→Normal)

Command	R/W	Values	Description
0xFE	W	0x00	Page 00
0x38	W		Exit AOD Mode

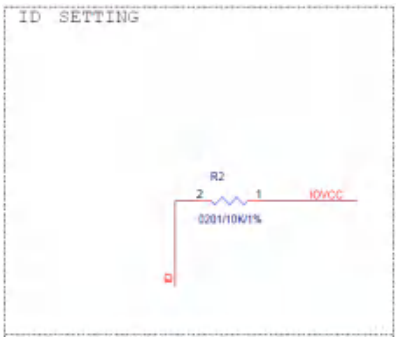
3.8.5 VIDEO TRIM(OSC Learning Setting)

Command	R/W	Values	Description
0xFE	W	0xA0	Page A0
0x46	W	0x0A	
0xFE	W	0xD4	Page D4
0x1C	W	0x01	
0x21	W	0x03	
0x22	W	0x81	
0x23	W	0x03	
0x24	W	0xE8	
0x1E	W	0x00	
0x1F	W	0x04	
0x20	W	0x04	
0x14	W	0x83	00:Disable 83:Enable

Note：Video trim 设置 Base On MIPI 速率 864.8Mbps，OSC 晶振 120.5MHz，MIPI 速率变更后需重调

3.8.6 ID Setting(Read)

3.8.6.1 硬件识别：



3.8.6.2 生产批次 ID

Read ID

Command	R/W	Values	Description
0xFE	W	0xC2	Page C2
0x00	R/W		P1.0:0x40 P1.1:0x50 P2.0:0x90 MP:0xC0

3.8.6.3 白点和 ID

Command	R/W	Values	Description
0xA100	R		Read Page C2 01~08h
注：读取 9 个 byte，第 1~2 byte 为亮度值 Lv,第 3~5 byte 为色坐标 x,第 6~8 byte 为色坐标 y，数据格式如下表格（表格中数据仅为参考）			

Command	Values							
0x01C2~0x08C2	Parameter	1st	2nd	3rd	4th	5th	6th	7th	8th
	HEX	0x01	0xAE	0x03	0x00	0x00	0x03	0x01	0x05
	DEC	430		3	0	0	3	1	5
	Color Coordinate	430nit		Wx:0.300			Wy:0.315		

3.8.7 ELVDD Compensation Control

Compensation On

Command	R/W	Values	Description
0xFE	W	0xA0	Page A0
0x4F	W	0xE0	Compensation On

Compensation Off

Command	R/W	Values	Description
0xFE	W	0xA0	Page A0
0x4F	W	0x20	Compensation Off

3.8.8 IR drop

GIR ON

Command	R/W	Values	Description
0xFE	W	0x40	Page 40
0xBD	W	0x05	Compensation ON

GIR OFF

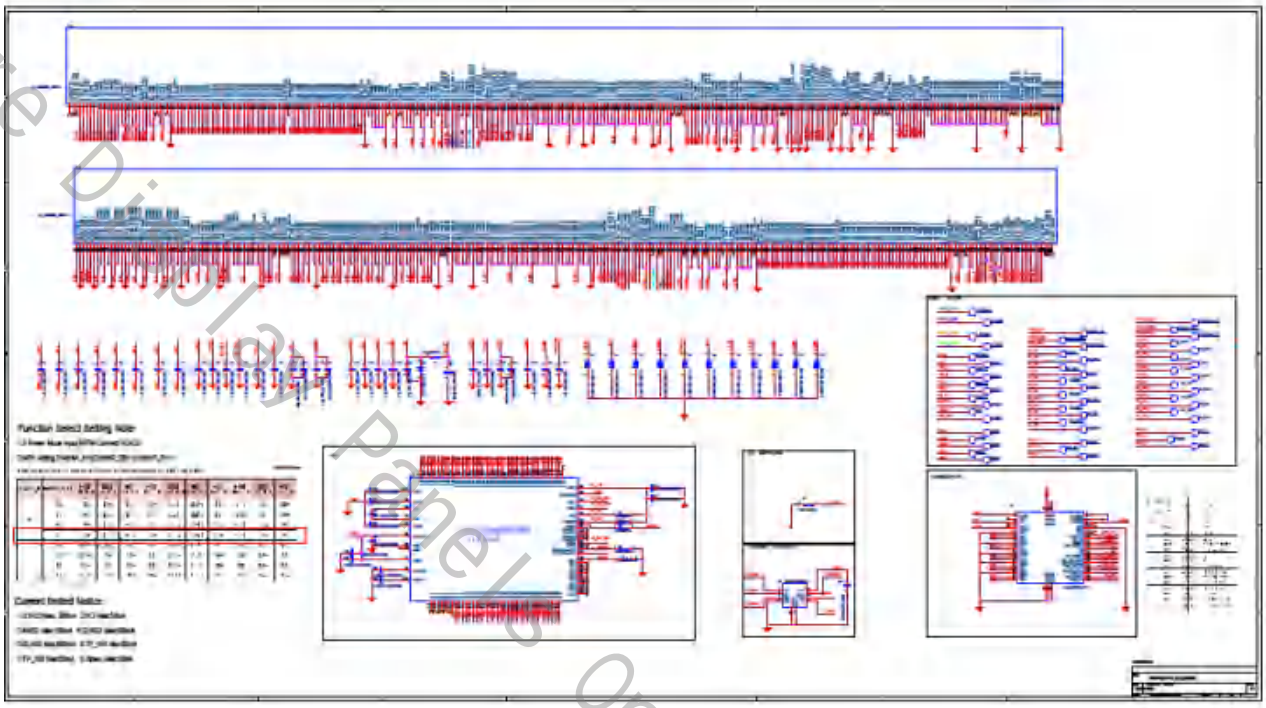
Command	R/W	Values	Description
0xFE	W	0x40	Page 40
0xBD	W	0x00	Compensation OFF

Appendix

其他需要补充的文档说明

3.9 FPC & BOM

3.9.1 FPC schematic



3.9.2 BOM list

Item	名称	插件位置	规格描述	数量	单位
1	贴片电容	C1,C2,C3,C4,C8,C11,C12,C13,C14,C19,C20,C25,C33	0201/1.0uF/16V/X5R	13	PCS
2	贴片电容	C15,C21,C22,C40	0201/2.2uF/10V/X5R	4	PCS
3	贴片电容	C6,C18	0402/4.7uF/10V/X5R	2	PCS
4	贴片电容	C5,C27,C38	0201/4.7uF/6.3V/X5R	3	PCS
5	贴片电容	C9	0402/2.2uF/16V/X5R	1	PCS
6	贴片电容	C10,C16,C17,C26	0402/2.2uF/25V/X5R	4	PCS
7	贴片电容	C23	0402/4.7uF/16V/X5R	1	PCS
8	贴片电容	C24	0201/22nF/6.3V/X5R	1	PCS
9	贴片电容	C7,C29,C35,C36	0402/10uF/10V/X5R	4	PCS
10	贴片电容	C30,C31,C32,C37,C39	0201/0.1uF/10V/X5R	5	PCS
11	贴片电容	C34	0201/0.1uF/16V/X5R	1	PCS
12	贴片电容	C41,C42	0201/150pF/50V/C0G	2	PCS
13	贴片电容	C43	0201/150pF/50V/C0G	1	PCS
14	TVS	D1,D2,D3,D4,D6,D7,D8,D9	TVSNM3V3CESGP-A	8	PCS
15	TVS	D5	TVSNM8VCESGP-A	1	PCS
16	Schottky	D10	KS52130F2-HXC	1	PCS
17	贴片电阻	R1,R5	0201/0R/1%	2	PCS
18	贴片电阻	R2,R3,R4	0201/10K/1%	3	PCS
19	贴片电阻	R6,R7	0201/100K/1%	2	PCS
20	TIC	U2	FST1BA80YA2BF	1	PCS
21	连接器	U3	5052744042(Molex)	1	PCS
22	FLASH	U4	GD25LQ32DNIGR	1	PCS

Note 1) The Following Capacitor Must Use Especial Model For Module Audio Noise Issue

Item	名称	插件位置	规格描述	数量	单位
1	贴片电容	C9	0402/2.2uF/16V/X5R (ZRB157R61C225KE11#)	1	PCS
2	贴片电容	C10,C26,C16,C17	0402/2.2uF/25V/X5R (ZRB157R61E225KE11#)	4	PCS
3	贴片电容	C29,C35，C36	0402/10uF/10V/X5R (ZRB15XR61A106ME01#)	3	PCS

4 Optical Specification

Item	Symbol	Condition	Values			Unit	Notes
			Min.(≥)	Typ.	Max.(≤)		
Color shift	Δu′ v′	Up/Down/Right/Left θ=30°	/	/	3.5	JNCD	Note1 Note2
		Up/Down/Right/Left θ=45°	/	/	5.5		
		Up/Down/Right/Left θ=60°	/	/	6		
Contrast ratio	CR	@0 degree	600,000 : 1	/	/	/	
Viewing angle	CR	@80 degree	1000 : 1	/	/	/	
HBM mode color chromaticity equal to normal mode	RGBWΔx	CIE1931 x	-0.005	0	0.005	/	HBM : 600nit
	RGBWΔy	CIE 1931 y	-0.005	0	0.005	/	
AOD mode color chromaticity equal to normal mode	RGBWΔx	CIE1931 x	-0.008	0	0.008	/	
	RGBWΔy	CIE 1931 y	-0.008	0	0.008	/	
'Color chromaticity (CIE1931)	Wx	CIE1931 x	0.290	0.300	0.310	/	
	Wy	CIE 1931 y	0.305	0.315	0.325		
	Rx	CIE1931 x	0.663	0.683	0.703		
	Ry	CIE 1931 y	0.297	0.317	0.337		
	Gx	CIE1931 x	0.213	0.243	0.273		
	Gy	CIE 1931 y	0.69	0.72	0.75		
	Bx	CIE1931 x	0.104	0.134	0.164		
	By	CIE 1931 y	0.026	0.056	0.065		
Color Gamut	/	DCI P3	98(>)	100	/	%	CIE1931
Luminance (complete machine)	L	/	387	430	473	nits	
HBM Luminance (complete machine)	L	/	540	600	660	nits	
AOD Luminance (complete machine)	L	/	54	60	66	nits	
Reflectivity	reflectivity	/	/	/	6	%	Re: min5.20% max5.41% ave5.28% a: min1.53 max1.87 ave1.67 b: min-2.63 max-178 ave-2.06 @DVT4
	a	L*a*b	-2.5	0	2.5	/	
	b	L*a*b	-3.0	0	3.0	/	
Response time (first frame on+off)	/	/	/	/	2	ms	
The brightness of first frame	/	/	80	/	/	%	GIR off
Color uniformity	U%	/	/	/	2	JNCD	@W255，W128，W64
Luminance uniformity	U%	/	80	/	/	%	

Crosstalk	/	IEC	/	/	2	%	
Item	**Symbol**	**Condition**	**Values**			**Unit**	**Notes**
			Min.(≥)	**Typ.**	**Max.(≤)**		
'IR-Drop	/	|(R+G+B) - W|/W	/	/	6	%	
Lifetime@T95	/	/	400	/	/	Hr	W Pattern
	Δu′ v′	/	/	/	0.004	/	
Gamma	/	L5~L232	2.0	2.2	2.4	/	HBM：600nit
		L233~L240	1.9	2.2	2.5	/	
		L5~L232	2.0	2.2	2.4	/	100nit < L255≤430nit
		L233~L240	1.9	2.2	2.5	/	
		L13~L227	2.0	2.2	2.4	/	10nit < L255≤100nit
		L228~L235	1.9	2.2	2.5	/	
		L25~L222	2.0	2.2	2.4	/	2nit≤L255≤10nit
		L223~L230	1.9	2.2	2.5	/	
		L13~L227	2.0	2.2	2.4	/	AOD：60nit
		L228~L235	1.9	2.2	2.5	/	
Color shift of white pattern in different DBV register value	Δu′ v′	Condition1	/	/	0.004	/	L255 满足左侧需求
	CCT	Condition2	/	/	400	K	
Image Sticking	/	The Time to < 1 JND(0.004)	/	20	25	s	Panel Add Cu
	/	18*6 checker pattern 10min，to G128	/	58	65	min	

Note1：Internal control, to ensure that large Angle of view to the direction of green.

Note2：视角超规部分以主观限样为准；

Test Conditions:

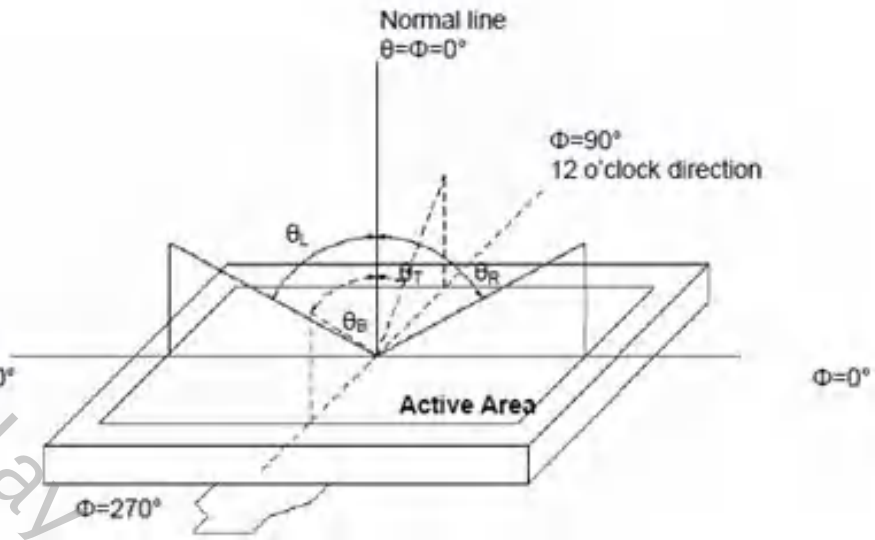
Condition1： max(duv of (DBV level min- max))-min (duv of(DBV level min- max))，DBV level 1=2nits；

Condition2： max(CCT of (DBV level min- max))-min(CCT of(DBV level min- max))，DBV level 1=2nits；

Condition3： The ambient temperature is 25℃,in dark room

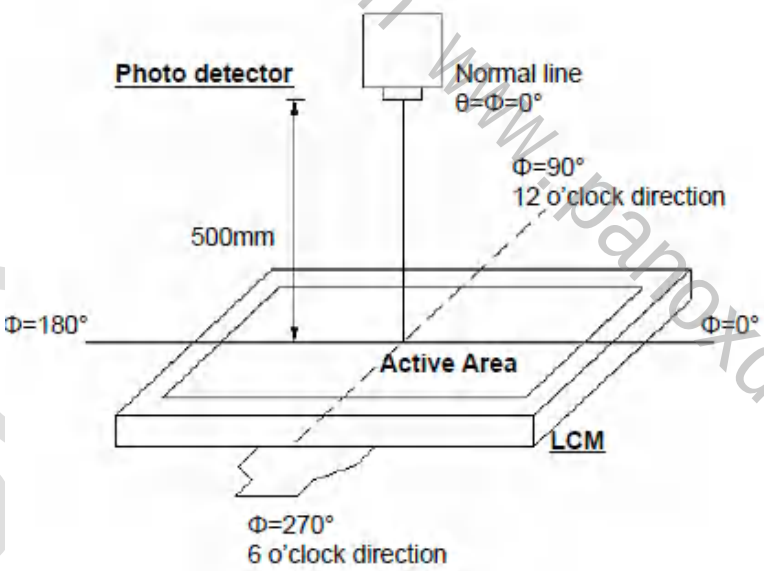
Condition4： The test systems refer to Note 2.

Note 1 : Definition of viewing angle range



Note 2 : Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the OLED screen. (Viewing angle is measured by CS2000A/Height :500mm , Response time is measured by Eldim optiscope200, other items are measured by CS2000A/ spot diameter 8mm /Height: 500mm.)



Note 3 : Definition of contrast ratio

Contrast ratio (CR) = Luminance measured when OLED on the "White" state/ Luminance measured when OLED on the "Black" state

Note 4 : Definition of color chromaticity

White/Red/Green/Blue Color coordinates measured at center point of OLED.

Note 5 : Definition of Luminance

White 255 Gray measured at center point of OLED.

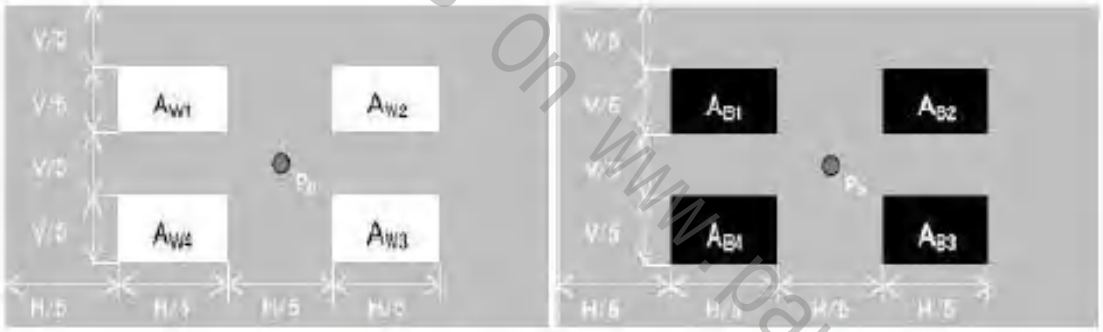
Note 6 : Definition of cross-talk

Measure luminance at the position,P_0

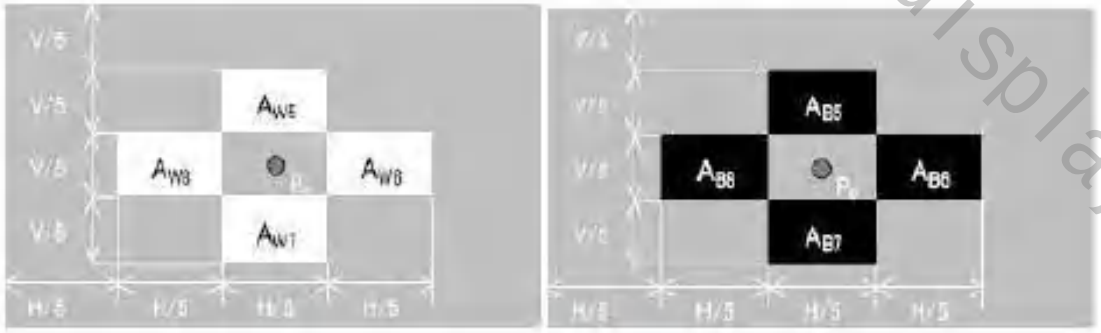
Calculate cross-talk as below equation

$$crosstalk = \frac{|L_{Wi\_ON} - L_{W\_OFF}|}{L_{W\_OFF}} \times 100\% \quad (i = 5\ to\ 8)$$

$$crosstalk = \frac{|L_{Bi\_ON} - L_{B\_OFF}|}{L_{B\_OFF}} \times 100\% \quad (i = 5\ to\ 8)$$



(a) L_{W_OFF}, L_{B_OFF} measuring pattern



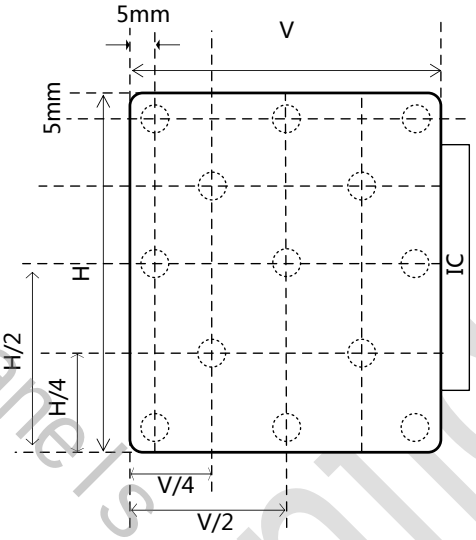
(b) L_{W_ON}, L_{B_ON} measuring pattern

Note 7 : Definition of Luminance Uniformity and color uniformity

Measure the luminance of gray level 255 &128&64 at 13 points

Luminance Uniformity = $\frac{Lmin}{Lmax}$ *100%

Color Uniformity=max[sqrt ((ui-uj)^2 + (vi-vj)^2)],i=1,2,3…13,j=1,2,3…13

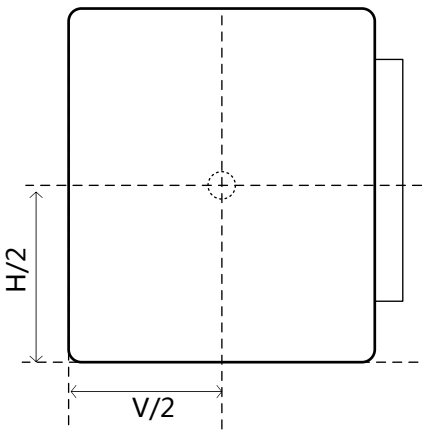


Note 8 : Definition of Lifetime

Lifetime Measure Steps :

- Light on W Aging pattern for 0.5h befor lifetime measure
- 0h ——W Aging pattern,measure pt.① initial luminance & $\Delta U'V'$
- 0~1h ——W Aging pattern
- 1h ——W Aging pattern,measure pt ① luminance & $\Delta U'V'$
- Loop step below progress ….to 400h

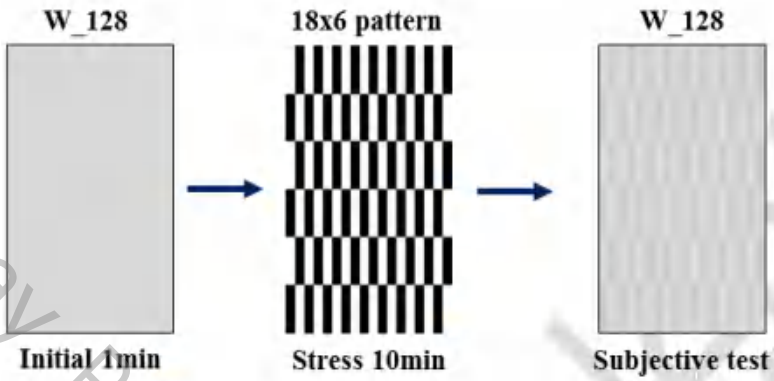
Aging pattern



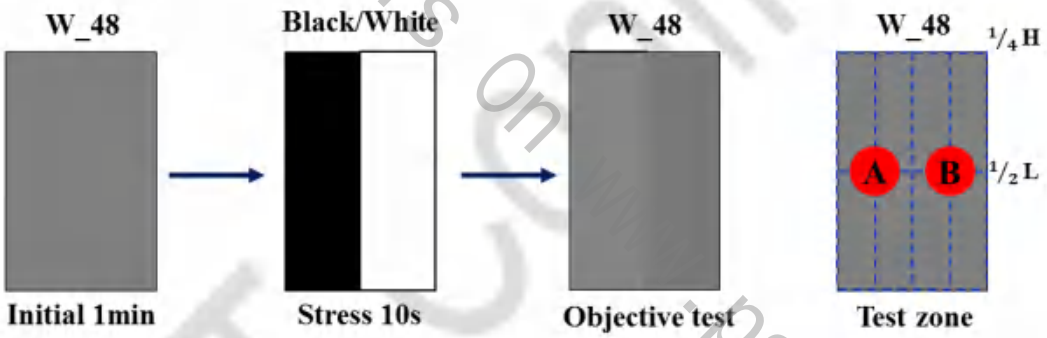
Note 9 : Definition of Image sticking

9.1 Subjective test

1. Test environment temperature is 25℃.
2. Light on W128 pattern for 1min , then change to 18*6 checker pattern for 10min , at last change to W128 pattern and record the time of duration.



9.2 Objective test



Step:

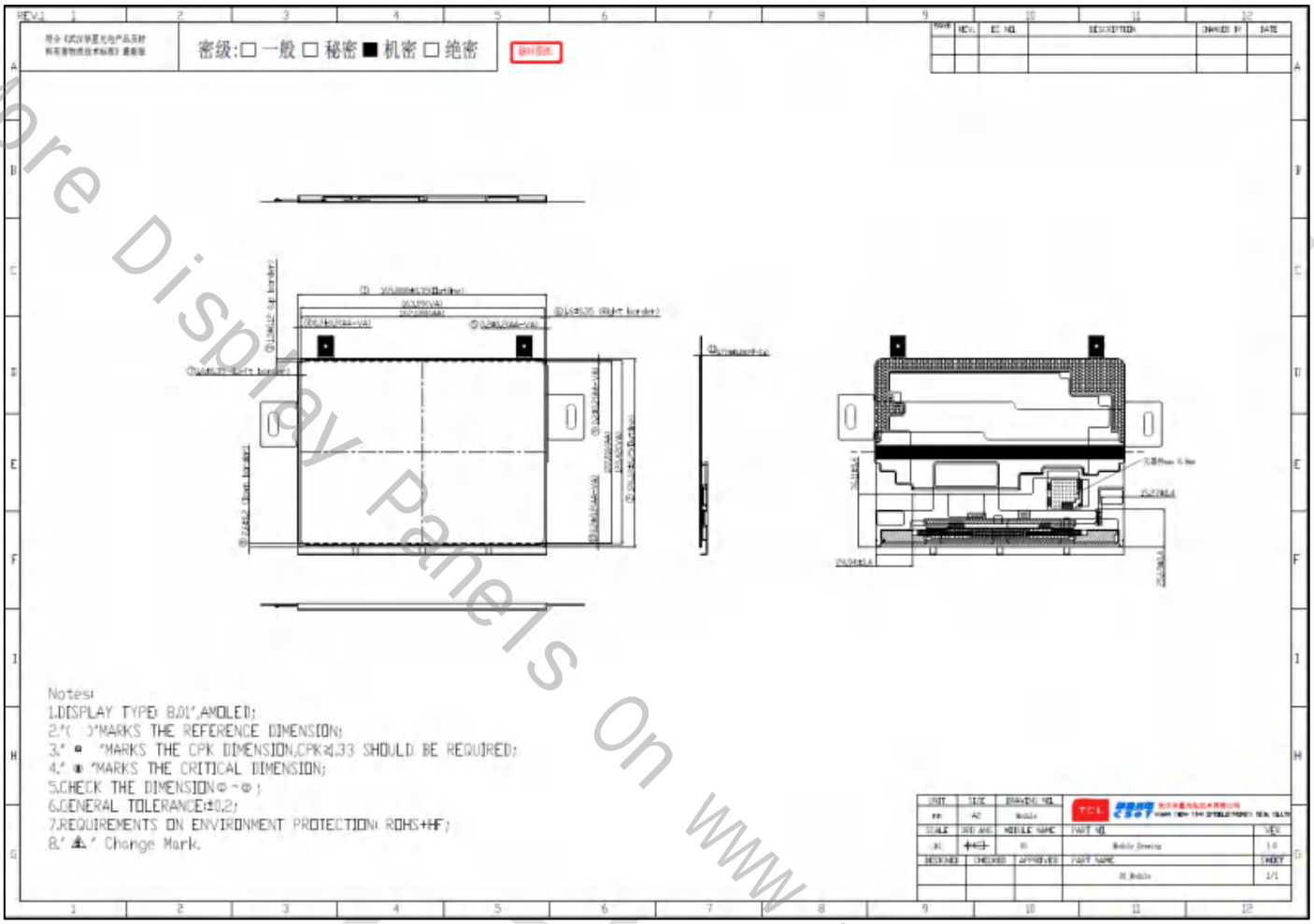
1. Test environment temperature is 25℃.
2. light on 48 gray pattern for 1min , than Change to a black/white pattern for 10s , at last change the pattern back to 48 gray for 1min.
3. Using CA-P410 measures the luminance once a second of test zone in the whole process.
4. Calculate the Michelson contrast value X with formula below :

$$X = \left(\frac{L_{A(t)} - L_{B(t)}}{L_{A(t)} + L_{B(t)}} - \frac{L_{A(Initial\ average)} - L_{B(Initial\ average)}}{L_{A(Initial\ average)} + L_{B(Initial\ average)}}\right)/1JND$$

$$1\ JND = 0.4\%$$

5 Mechanical Characteristics

5.1 Outline Drawing



Drawing_module

5.2 Dimension Specifications

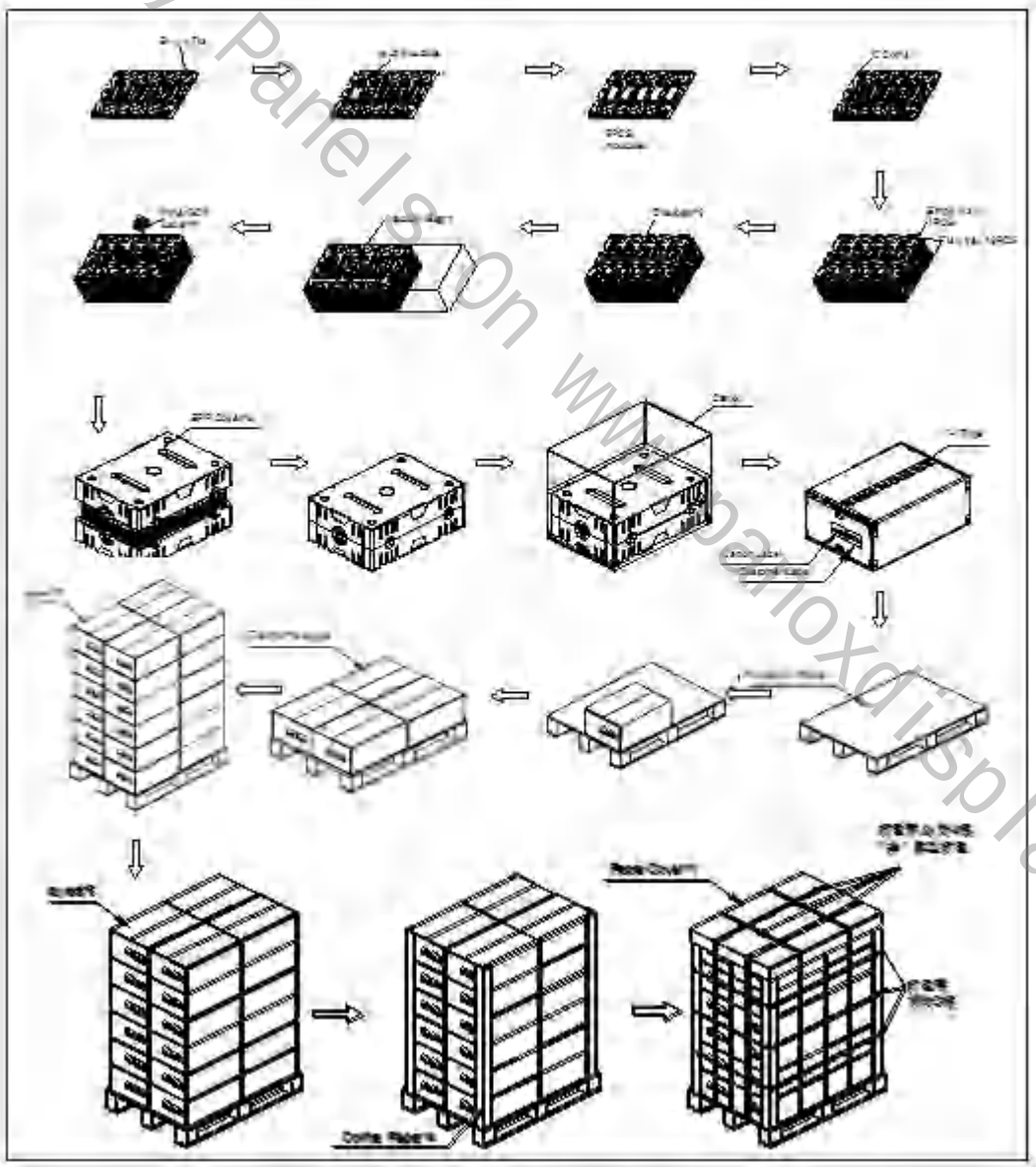
Item	Min.	Typ.	Max.	Unit	Note
Width	125.87	126.12	126.37	mm	
Height	165.74	165.89	166.04	mm	
Depth	0.698	0.778	0.858	mm	
Weight	41.5	46.5	51.5	g	

5 Package Drawing

6.1 Packing Specifications

Item	Specification	Remark
Carton(Box) Packing	20pcs	
Carton(Box) Packing Size	560x390x227mm	
Carton(Box) Packing Weight	6.5kg	For Reference
Pallet Packing	480pcs	
Pallet Packing Size	1140x800x1492mm	
Pallet Packing Weight	170kg	For Reference

6.2 Packing Method



6.3 quality guarantee period

Item	Spec.
quality guarantee period	Six month
Storage environment	Temperature 25 ± 5 ℃, humidity 50% ± 20%

7 RA Requirements

No.	Test Item	Test Condition	Spec
1	High Temperature High Humidity Operation	60℃, 90%RH ,240h	外观,功能,TP OK
2	High Temperature Operation	70℃,240H	外观,功能,TP OK
3	Low Temperature Operation	-30℃,240H	外观,功能,TP OK
4	High Temperature Storage	80℃,240H	外观,功能,TP OK
5	Low Temperature Storage	-40℃,240H	外观,功能,TP OK
6	Thermal Shock	(-40℃/60min<->85℃/60min)，32cycles	外观,功能,TP OK
7	ESD Test	Contact，±6KV；Air，±8KV	外观,功能,TP OK
8	On off test	25℃±2℃，On 3s，Off 3s，1500 times	外观,功能,TP OK
9	正面点压测试	取 9 个点以 2±0.5N 压力进行 80 万次点击，点击速率 1S/次	外观,功能,TP OK
10	表面硬度	750g 速度 60mm/min，移动 2-3cm，划 5 条线，每划一次将铅笔芯转动 60 度	6B 铅笔测试 5 条，出现 0~1 条压痕或划痕判定 OK，2 条及以上压痕或划痕判定为 NG，记录测试数据，不做 fail 判定
11	耐摩擦	施加 1kg 的负载，以 40cycle/min 的速度，以 40mm 的行程，压头大小:10mm*10mm，在非油墨面的表面来回磨擦 2000 个往复	初始水滴角>110 度，测试后肉眼判定无明显痕迹（摩擦后水滴角≥100 度），记录测试数据
12	落笔	晨光 K35 笔重 13g，点位跌落高度从 1cm 起，并以 1cm 为 step 递增，重复测试同一点位，直至 panel 出现外观及功能性不良，	样品表面无破损、样品无功能性不良 记录测试结果
13	落球	刚球重 32.65g，直径为 20mm，点位跌落高度从 1cm 起，并以 1cm 为 step 递增或递减，重	样品表面无破损、样品无功能性不良

		复测试同一点位，直至 panel 出现外观及功能性不良，	记录测试结果
14	Static Folded （Room temperature）	240h	外观,功能,TP OK
15	Static Folded (60°C/90%)	60°C/90% 240h	外观,功能,TP OK
16	Dynamic Folding (Room temperature)	200K	外观,功能,TP OK
17	Dynamic Folding (70°C)	70°C 100K	外观,功能,TP OK
18	Dynamic Folding (-10°C)	-30°C 50K	外观,功能,TP OK
19	Dynamic Folding (60°C/90%)	60°C/90% 100K	外观,功能,TP OK
20	Package Test	50℃ 80%RH, Storage 2hr Vibration Test : Frequency 5Hz , Amplitude 20mm. Direction : X,Z ; X and Z each 60min. Package Drop Test (Direction) : 1Angle , 3Edge , 6Face; Drop height refer to the table as below. 包装总重量 / 跌落高度（CM） 10KG以下 / 80 10KG~20KG / 60 20KG~30KG / 50 30KG~40KG / 40	外观,功能,TP OK

8 General Precautions

Please pay attention to the following items when you use the folding OLED Module(Panel):

8.1 Do not twist or bend the module(panel) and prevent the unsuitable external force for display during assembly.

8.2 Adopt measures for good heat radiation. Be sure to use the module(panel) with in the specified temperature.

8.3 Avoid alcohol, oil and dust mixing during assembly.

8.4 Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module(panel).

8.5 Less EMI: it will be more safety and less noise.

8.6 Please operate module(panel) in suitable temperature. The response time & brightness will drift by different temperature.

8.7 Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.

8.8 Please be sure to turn-off the power when connecting or disconnecting the circuit.

8.9 PF scratches easily, please handle it carefully.

8.10 Display surface never likes dirt or stains.

8.11 A dew drop may lead to destruction. Please wipe off any moisture before using module(panel).

8.12 Sudden temperature changes cause condensation, and it will cause polarizer damaged.

8.13 High temperature and humidity may degrade performance. Please do not expose the module(panel) to the direct sunlight and so on.

8.14 Acetic acid or chlorine compounds are not friends with AMOLED display module(panel).

8.15 Static electricity will damage the module(panel), please do not touch the module(panel) without any grounded device.

8.16 Please avoid any static electricity damage (ESD) during producing and operating.

8.17 Do not disassemble and reassemble the module(panel) by self.

8.18 Be careful do not touch the rear side directly.

8.19 No strong vibration or shock. It will cause module(panel) broken.

8.20 Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.

8.21 Do not store the module in surroundings containing organic solvent or corrosive gas.

8.22 Be careful of injury from a broken display module (panel).

8.23 Please avoid the pressure adding to the surface (front or rear side) of module(panel), because it will cause abnormal display.

8.24 Do not bend the module(panel) by hand before assembly, It will cause module(panel) damage.

8.25 Do not irradiate the module(panel) directly with UV, otherwise it will cause abnormal display.

8.26 The module(panel) cannot be bent with protective film, otherwise it may cause abnormal display.

8.27 In the process of module(panel) assembly, the process protective film should be pasted, but there should be no attached bubbles, otherwise the bubbles will have the risk of imprint transfer.