Doc. Number:

☐ Tentative Specification
■ Preliminary Specification
☐ Approval Specification

MODEL NO.: PO139FN01F

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____
Note

_____
Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

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REVISION HISTORY

Version	Date	Page	Description
Ver 1.0	Aug,2017	All	Spec Ver.1.0 was first issued..

1. PURPOSE

PO139FN01F is a color active matrix of Organic Light-Emitting Diode (AMOLED), which uses Low Temperature Poly-silicon (LTPS) as switching devices. This panel has a 1.39 inches diagonally measured active display area with 400 x 400 resolutions. This product is composed of a LTPS-AMOLED panel, Polarizer, driver IC(COF) and FPCa. The following describes the features of this product.

2. FEATURES

1.39” (diagonal) inch configuration

400xRGBX400 resolution

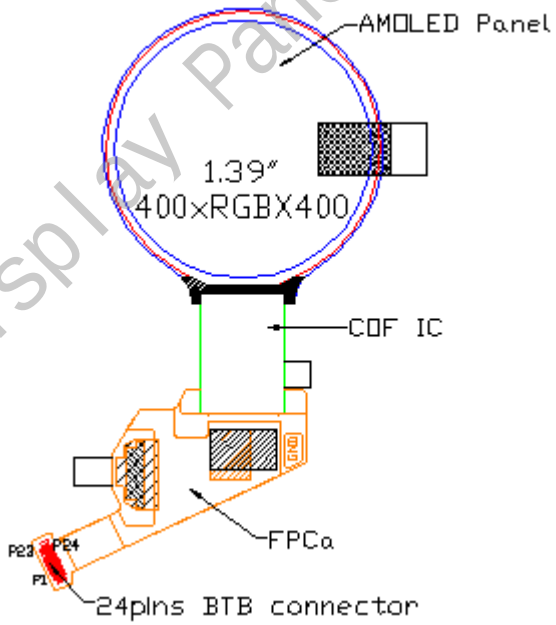
287 PPI

3. GENERAL RULES OF SINGLE PANEL

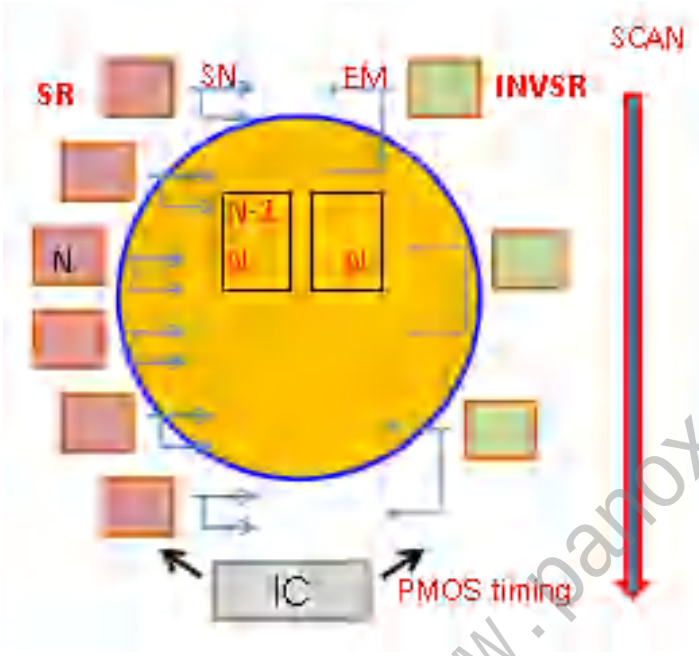
3-1 Physical Specification

No.	Item	Specification	Unit
1	Screen Size	1.39 (Diameter)	inch
2	Display Resolution	400 x 400	pixel
3	Pixel Pitch	0.0885 (H) x 0.0885 (V)	mm
4	Active Area	35.4mm (Diameter)	mm
5	Outline Dimension	38.6 (H) × 40.5(V) × 0.7typ,0.8max (T) w/o FPCa	mm
6	Pixel Configuration	RGB-SBS	--
7	Color Depth	8/8/8	colors
8	Display Type	Color OLED	--
9	Interface Type	MIPI	--
10	Surface Treatment	NA	--
12	Weight	1.5	g

3-2 Module Appearance



3-3 Panel Scan Direction



4. ABSOLUTE MAXIMUM RATING

(Ta = 25 ± 2℃)

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VCI	-0.3	5.5	V	Power for digital circuit
Interface supply voltage	VDDIO	-0.3	5.5	V	Power for Interface circuit
ELVDD power supply	ELVDD	-	5.0	V	Power for OLED
ELVSS power supply	ELVSS	-5.0	-	V	Power for OLED
Storage temperature	Tstg	-30	+70	℃	
Operating Temperature	Topr	-20	+60	℃	

Note:

(1) All of the voltages listed above are with respective to GND= 0V

(2) Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

5. ELECTRICAL CHARICTERISTICS

5-1. Operating Conditions:

(Ta = 25 ± 2℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Driver driving voltage	VCI	2.7	2.8	3.6	V	(1)
	VDDIO	1.65	1.8	3.3	V	(1)
OLED driving voltage	ELVDD	4.55	4.6	4.65	V	(1)
	ELVSS	-2.35	-2.4	-2.45	V	(1)

Note:

(1) The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during the operation. To prevent the noise, a bypass capacitor must be inserted into the line closed to the power pin.

5-2. Power Consumption:

(Ta = 25 ± 2℃)

Display Mode	Item	Symbol	Spec	
			Typ	Max
			Current(mA)	Current(mA)
100% Pixel On (Normal mode)	Current of VDDIO	Ivddio	3.0	-
	Current of VCI	Ivci	6.1	-
	Current of ELVSS	Ielvss	20.5	-
50% Pixel On (Normal mode)	Current of VDDIO	Ivddio	3.0	-
	Current of VCI	Ivci	6.1	-
	Current of ELVSS	Ielvss	10.3	-
ALL Pixel Off (Normal mode)	Current of VDDIO	Ivddio	3.0	-
	Current of VCI	Ivci	6.0	-
	Current of ELVSS	Ielvss	0.0	-
ALL Pixel Off (Standby mode)	Current of VDDIO	Ivddio	-	0.0
	Current of VCI	Ivci	-	<2uA
	Current of ELVSS	Ielvss	-	0

Note:

(1) **Power supply**：VDDIO=1.8V VCI=2.8V

(2) **Frame Frequency**：Fframe =60Hz @25degC, Brightness 300nits MIPI CMD mode

(Ta = 25 ± 2℃)

Display Mode	Item	Symbol	Spec	
			Typ	Max
			Current(mA)	Current(mA)
10% Pixel On (Idle mode)	Current of VDDIO	Ivddio	0.6	-
	Current of VCI	Ivci	2.6	-
	Current of ELVSS	Ielvss	0.2	-

Note:

(1) **Power supply**：VDDIO=1.8V VCI=2.8V

(2) **Frame Frequency**：Fframe =15Hz @25degC, Brightness 30nits MIPI CMD mode

6. DC CHARACTERISTICS

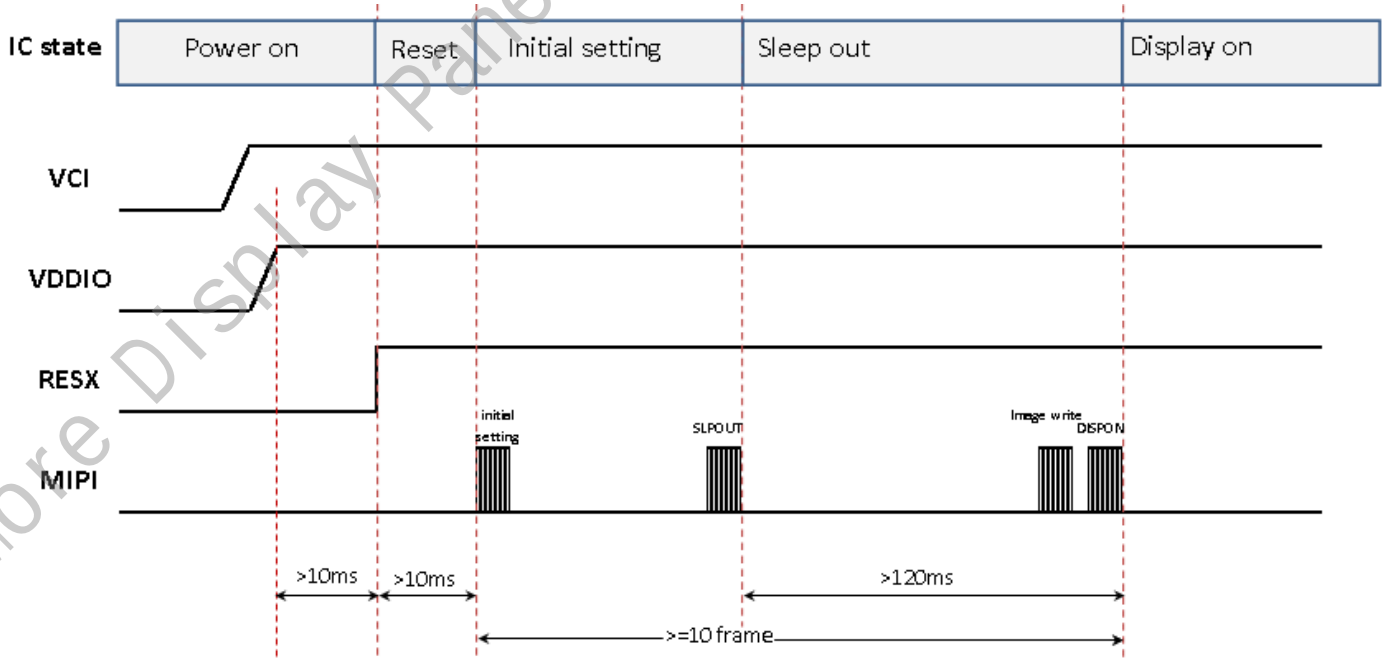
6.1 Parameter

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
High Level Input Signal Voltage	VIH	VDDIO=1.65~3.3V	0.8xVDDIO	-	VDDIO	V	
Low Level Input Signal Voltage	VIL	VDDIO=1.65~3.3V	0	-	0.2xVDDIO	V	
High Level Output Signal Voltage	VOH	VDDIO=1.65~3.3V	0.8xVDDIO	-	VDDIO	V	
Low Level Output Signal Voltage	VOL	VDDIO=1.65~3.3V	0-8	-	0.2xVDDIO	V	

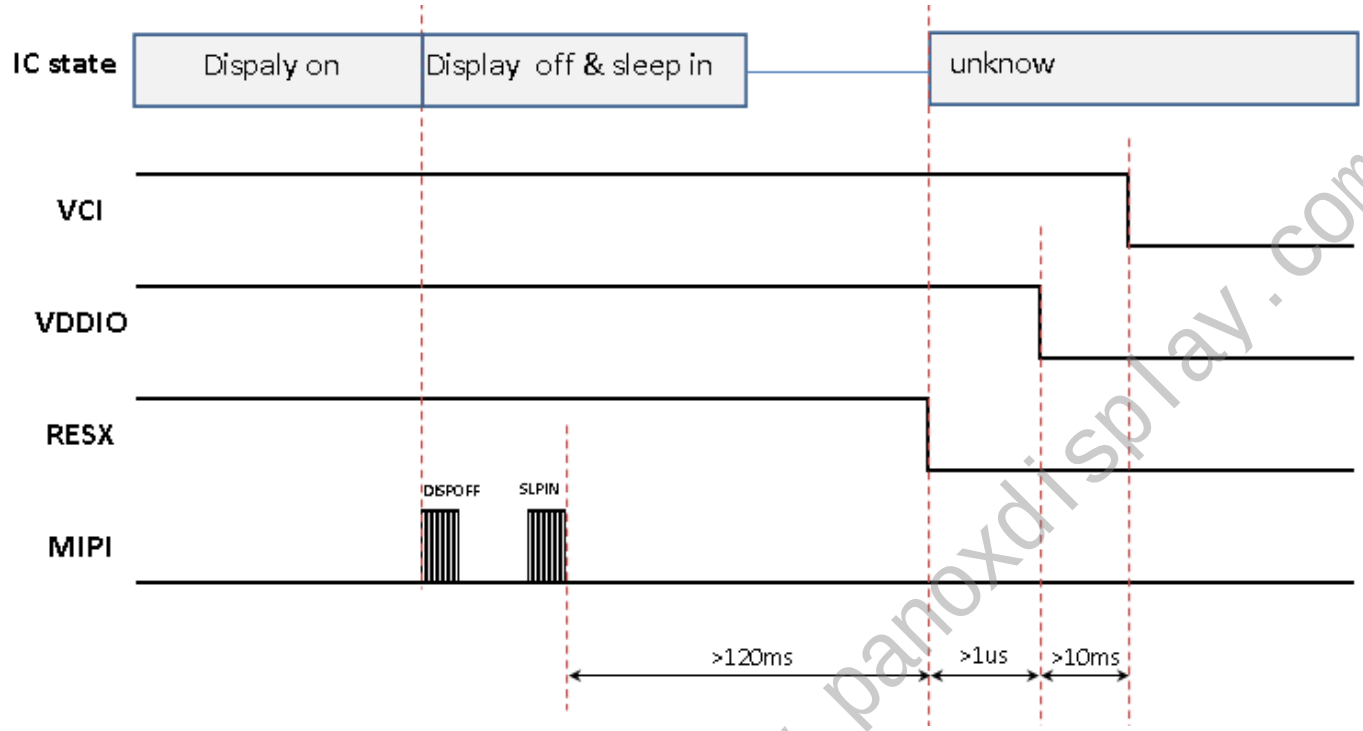
(Ta = 25 ± 2℃)

6.2 Operating Power Sequence

Power on sequence

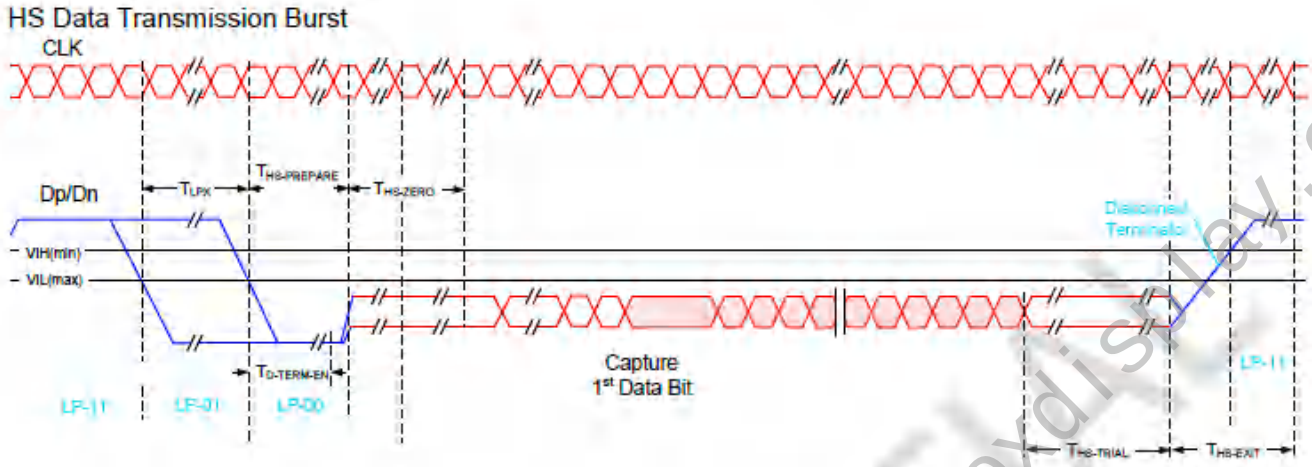


Power off sequence

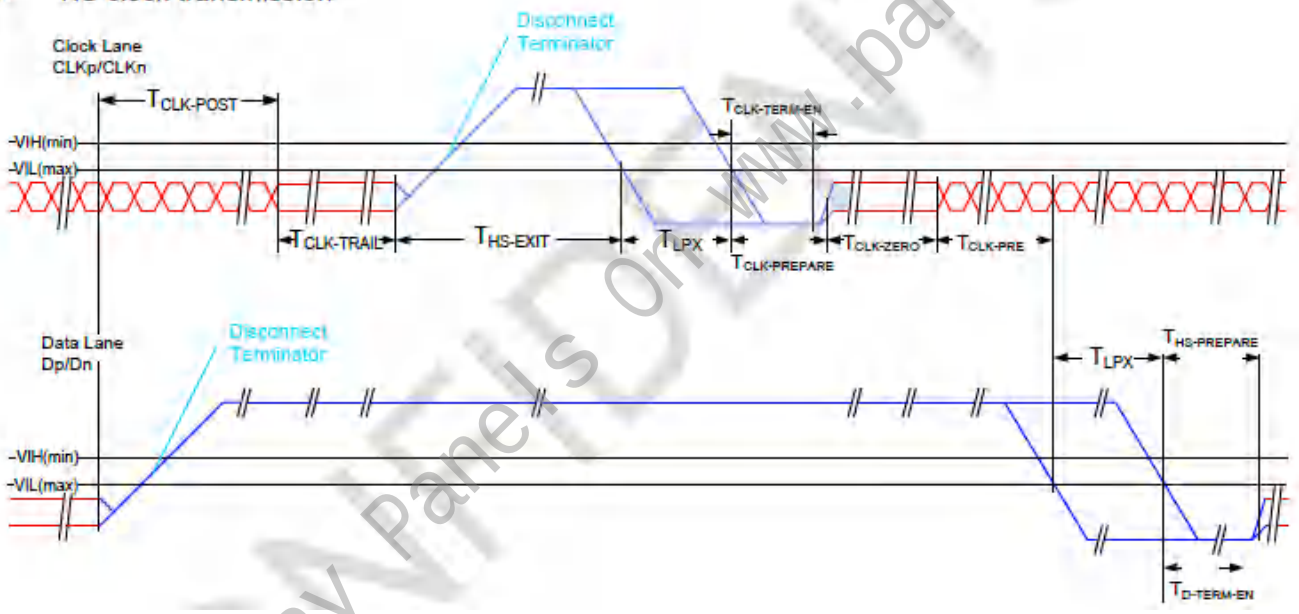


7. AC CHARCTERISTICS

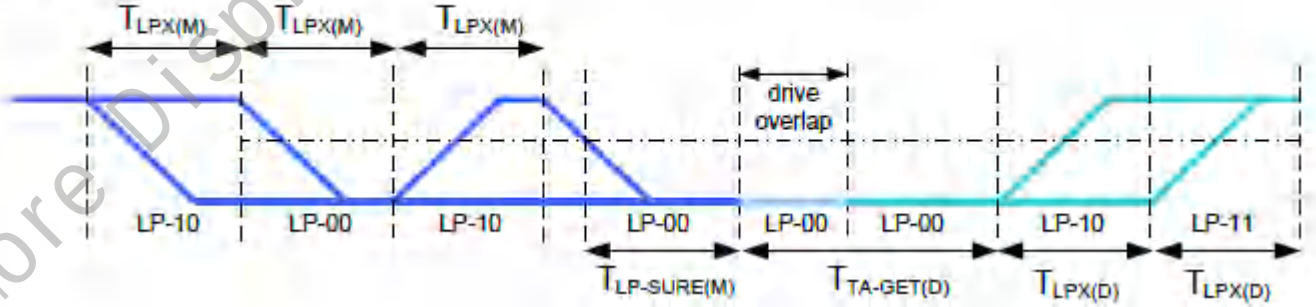
7.1. MIPI Interface Characteristics



➢ HS clock transmission



Turnaround Procedure

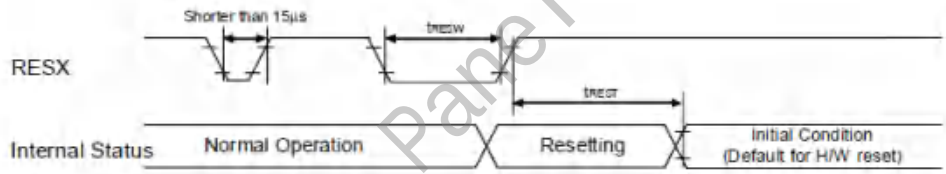


Timing Parameters: Parameter	Description	Min	Typ	Max	Unit
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL .	60ns + 52*UI			ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	300			ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	Time for Dn to reach VTERM-EN		38	ns
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	Time for Dn to reach VTERM-EN		35 ns +4*UI	
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		60 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns

THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns+4*UI			ns
TLPX(M)	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns
TTA-SURE(M)	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX(M)		2*TLPX(M)	ns
TLPX(D)	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns
TTA-GET(D)	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5*TLPX(D)			ns
TTA-GO(D)	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	4*TLPX(D)			ns
TTA-SURE(D)	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX(D)		2*TLPX(D)	ns

7.2. Display RESET Timing Characteristics

Reset input timing



IOVDD=1.65 to 1.95V, VDD=2.8 to 3.1V, AGND=DGND=0V, Ta=-40 to 85° C

Timing Parameters

Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRESW	*1) Reset low pulse width	RESX	10	-	-	-	us
tREST	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-			120	When reset applied during Sleep out mode	ms

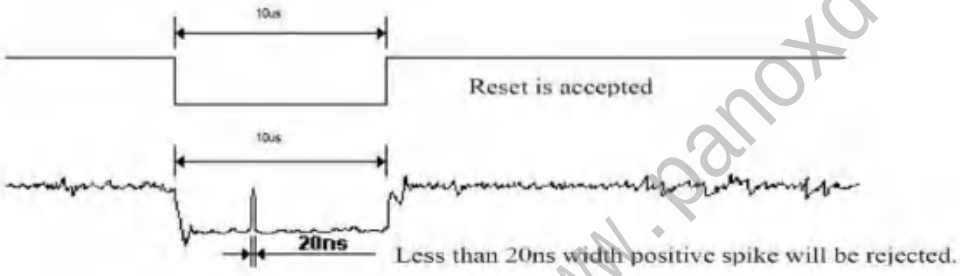
Note 1. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 s	Reset Rejected
Longer than 10 s	Reset
Between 5 s and 15 s	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. OPTICAL CHARCTERISTICS

(Ta = 25 ± 2℃,)

Item	Symbol		Condition	MIN	TYP	MAX	Unit	Remarks
Viewing Angle CR>1600	Top		-	80	-	-	Degree	Note 8-3
	Bottom			80	-	-		
	Left			80	-	-		
	Right			80	-	-		
Response Time	Tr+Tf		Θ=0°	-	<4	-	ms	Note 8-8
Contrast Ratio	CR		Θ=0°	-	10,000	-	-	Note 8-3
Luminance	L		Θ=0°	250	300	-	cd/m^2	Note 8-5
NTSC	-		-	85	100	-	%	Note 8-7
Uniformity	-		-	80	-	-	%	Note 8-6
Chromaticity	White	x	Θ=0°	0.27	0.30	0.33	-	Chromaticity
		y		0.28	0.31	0.34		
	Red	x		0.64	0.67	0.70		
		y		0.30	0.33	0.36		
	Green	x		0.19	0.24	0.29		
		y		0.65	0.70	0.75		
	Blue	x		0.09	0.13	0.17		
		y		0.025	0.065	0.105		
Gamma	-		-	1.9	2.2	2.5		

Above measuring is panel only.

Note 8

8.1 Definition of viewing angle range

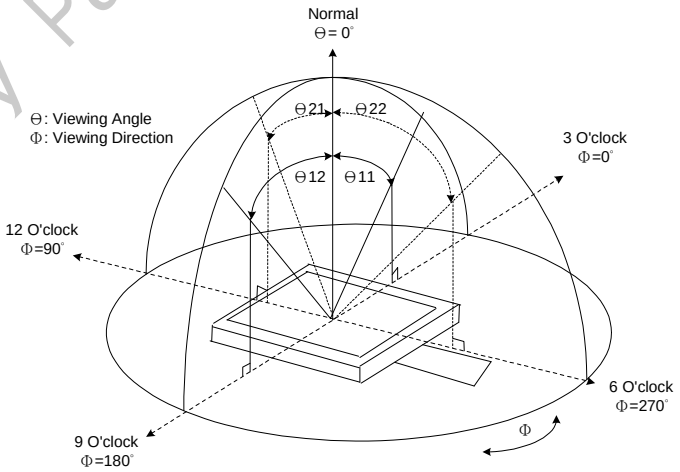


Fig. 8-1 Definition of viewing angle

8.2 Measuring setup:

The module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting for 20 minutes in a windless room.

8.2.1 Driving voltage

ELVDD= 4.6V, ELVSS=-2.4V

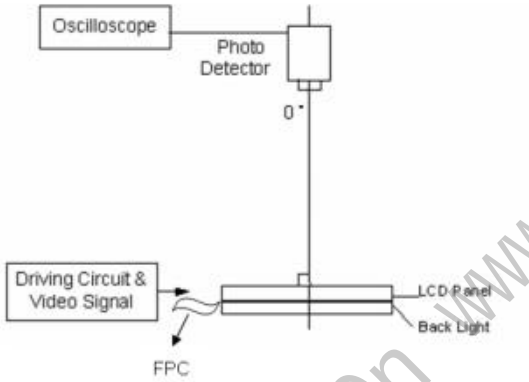
8.2.2 Ambient temperature: Ta=25℃

8.2.3 Testing point: measure in the display center point and the test angle Θ=0°

8.2.4 Testing Facility

Environmental illumination: ≤ 1 Lux

A. System A (DMS 900 series)



B. System B (SR3)

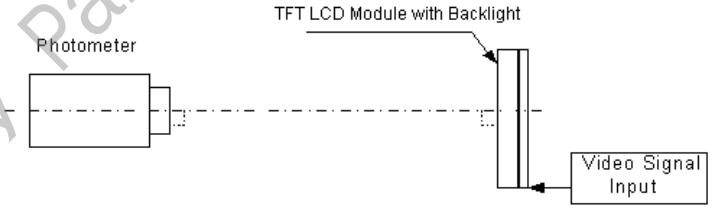


Fig. 8-2 Optical measurement system setup

8-3: Contrast ratio

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

8-4: Chromaticity and NTSC

Test Point: Display Center

8-5: Luminance

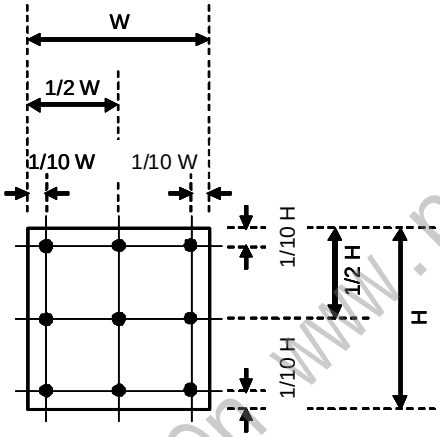
The measurement shall be done at the center of the display with a full white image.

8-6: Uniformity

The luminance of 9 points as the black dot in the figure shown below is measured and the uniformity is defined as the formula:

*

$$\text{Uniformity} = \frac{\text{The minimum luminance among 9 points}}{\text{The maximum luminance among 9 points}}$$

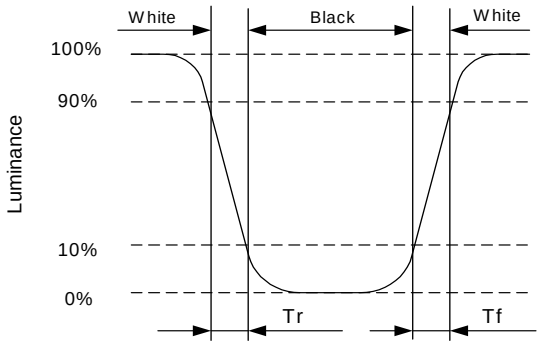


Active Area (W x H)

8-7: Chromaticity and NTSC

Test Point: Display Center

8-8: Definition of response time: (Measure System A_Photometer)



9. INTERFACE PIN CONNECTION

Main FPC Pin assignment — AMOLED Panel Input/Output Signal Interface

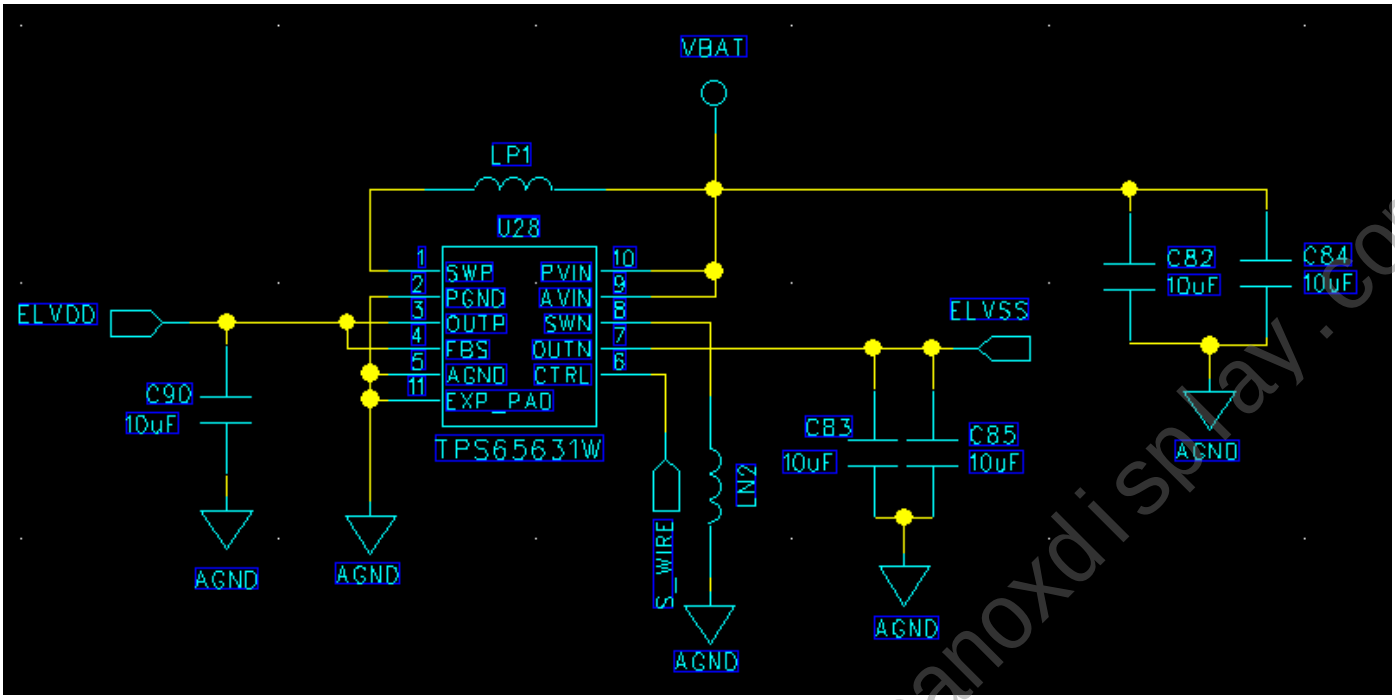
FPCA recommended connector: 504248-2410 (Molex)

Main board recommended connector: 504208-2410 (Molex)

Pin No	Symbol	I/O	Function	Remark
1	GND	P	GND	
2	RESX	I	Device reset signal (0 : Enable ; 1: Disable)	
3	HSSI_D0_N	I/O	MIPI data negative signal	
4	SWIRE	O	SWIRE signal for PWR IC control	
5	HSSI_D0_P	I/O	MIPI data positive signal	
6	MTP_PWR	P	MTP(need to indicate to connect GND or NC)	
7	GND	P	GND	
8	TE	O	Vsync(vertical sync)signal output from panel to avoid tearing effect	
9	HSSI_CLK_N	I	MIPI negative clock signal	
10	GND	P	GND	
11	HSSI_CLK_P	I	MIPI positive clock signal	
12	GND	P	GND	
13	GND	P	GND	
14	GND	P	GND	
15	VDDIO	P	Power supply for Interface system	
16	VCI	P	Power supply for analog	
17	GND	P	GND	
18	GND	P	GND	
19	ELVSS	P	AMOLED power Negative	
20	ELVDD	P	AMOLED power positive	
21	ELVSS	P	AMOLED power Negative	
22	ELVDD	P	AMOLED power positive	
23	ELVSS	P	AMOLED power Negative	
24	ELVDD	P	AMOLED power positive	

Note: I = input ; O = output ; P = Power ; I/O = input / output

Power IC Application Circuit



Note: OLED Power IC (TPS65631W)

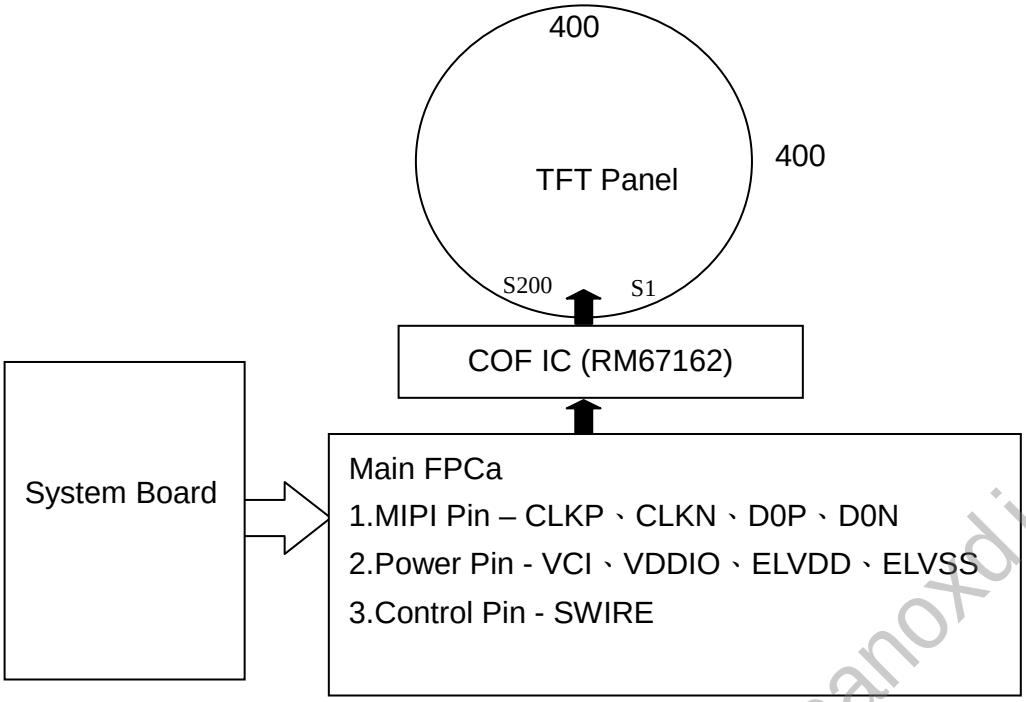
Input: VBAT (2.9 ~ 4.4V)

Output: ELVDD, ELVSS

Display Initial Setting

Recommended power on initial sequence								
Step	**Instruction**	**Delay time**	**R/W**	**MIPI Data Type**	**Address**		**Data hex.**	**Description**
					MIPI	**Others**		
1	Turn on VCI							VCI=2.8V
2	Turn on VDDIO							VDDIO=1.8V
3	Delay	no limit						
4	REST pin low	20us						
5	REST pin high							
6	Delay	5ms						
7			W	0x15	FE	FE00	00	
8			W	0x15	35	3500	01	
9	Sleep out		W	0x05	11	1100	00	
10	Delay	300ms						
11	Display on		W	0x05	29	2900	00	

10. BLOCK DIAGRAM

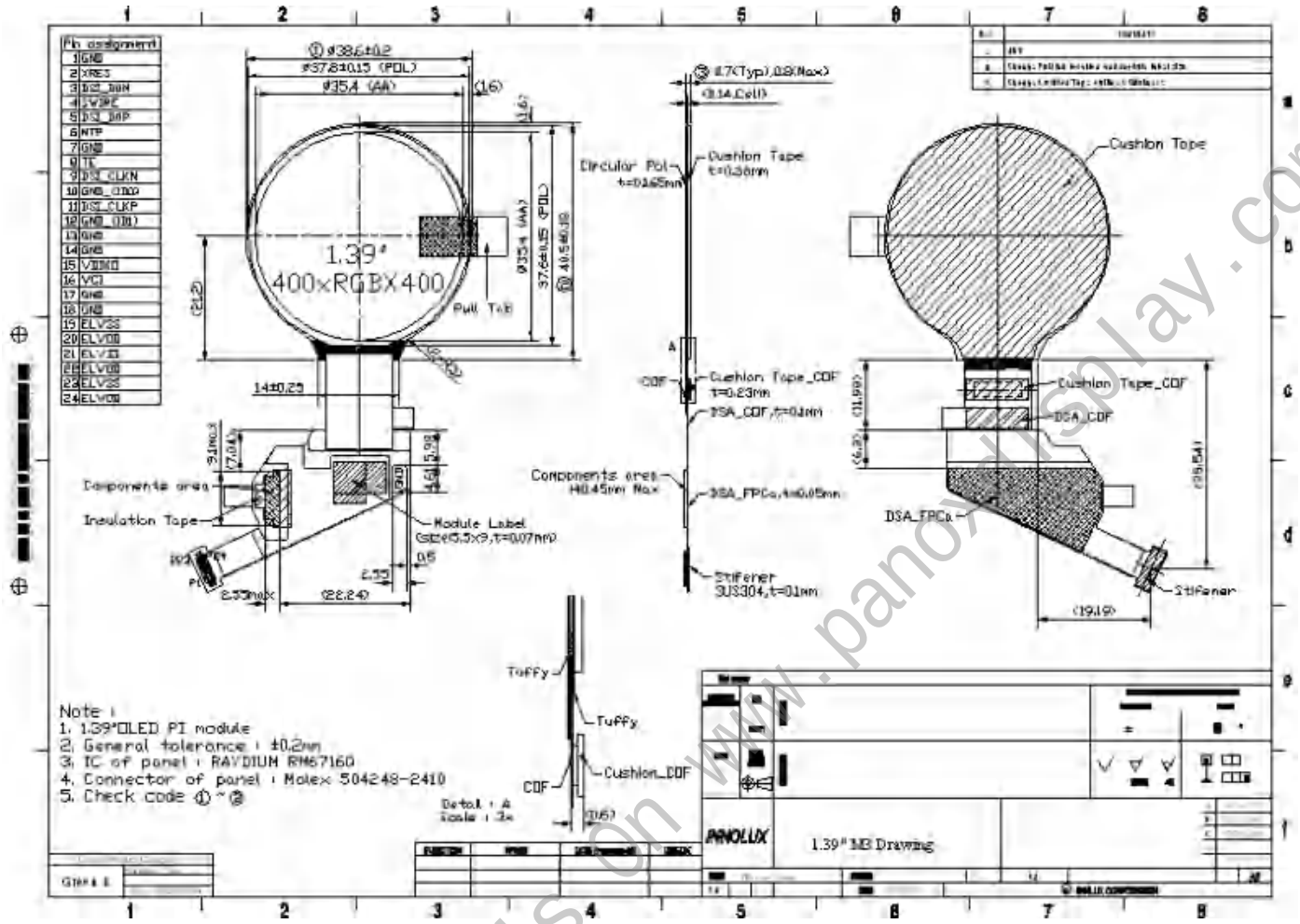


11.QUALITY ASSURANCE

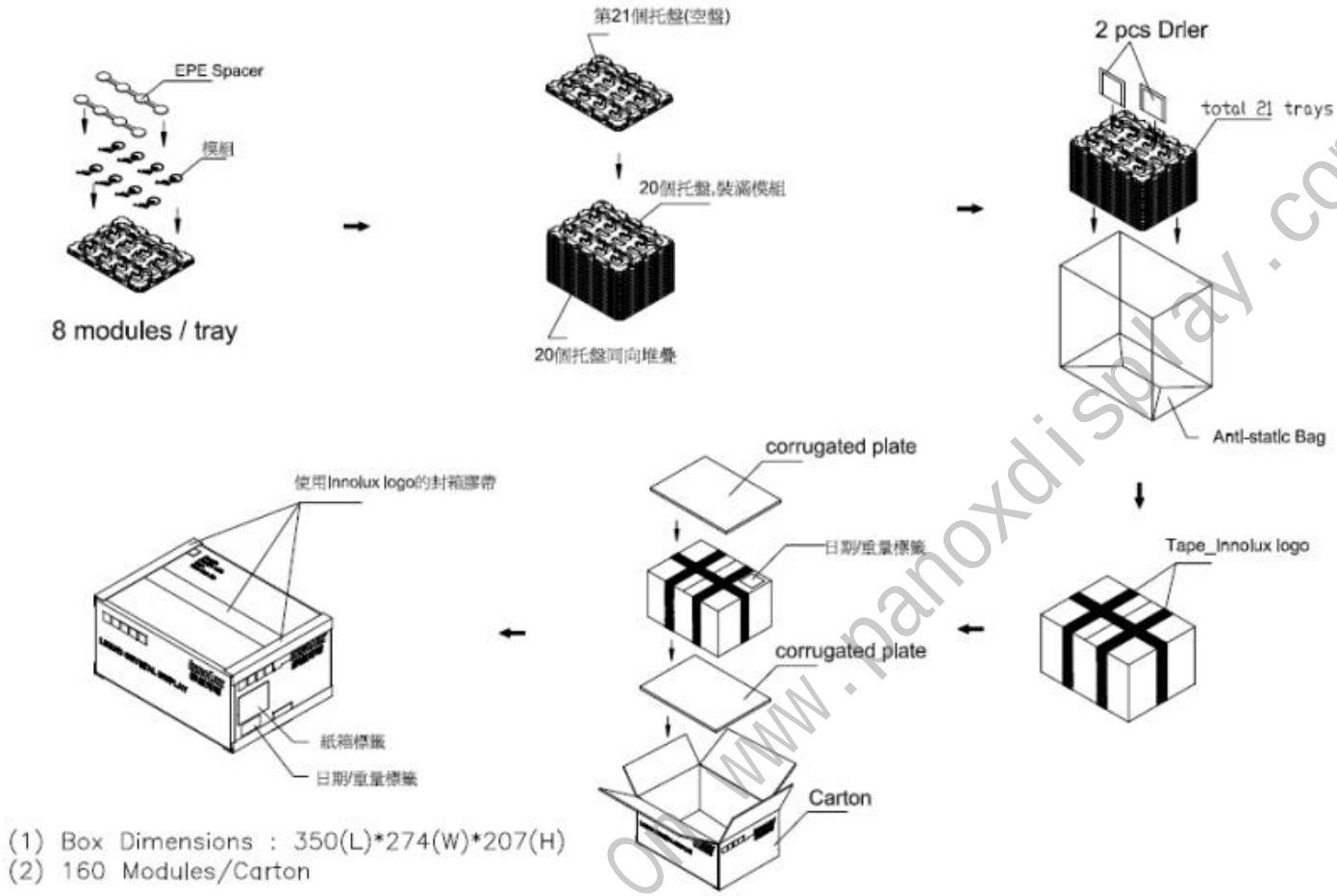
No	Test Item	Condition	Remark
1	High Temperature Operation	Ta=60℃, 240Hrs	Note1, Note2
2	High Temperature Storage	Ta=70℃, 240Hrs	Note1, Note2
3	Low Temperature Operation	Ta=-20℃, 240Hrs	Note1, Note2
4	Low Temperature Storage	Ta=-30℃, 240Hrs	Note1, Note2
5	High Temperature & High Humidity Operation	Ta=60℃, RH=90%, 240Hrs	Note1, Note2
6	Thermal Shock	-30℃(30min)←→70℃(30min), 100Cycles	Note1, Note2
7	Vibration Test - Non Operation	1.5G / 10-500Hz, 30mins/cycle, 1cycle for each X, Y, Z	Note2

Note1: The test samples have recovery time for 2 hours at room temperature before the function check. In the standard conditions, there is no display function NG issue occurred.
Note2: After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

12. OUTLINE DRAWING



13. PACKAGE FORM



1.39" Module (PO139FN01F) delivery packing method

(1). Module packed into tray cavity (with Module display face up) and covered byEPE.

(2). Tray stacking with 20 layers and with 1 empty tray above the stacking tray unit.
2pcs desiccant put above the empty tray

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4). Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton. Put 1pc cardboard above the package unit.

(5). Carton tapping with adhesive tape.

14. PRECAUTIONS

14.1 Adopt measures for good heat radiation. Be sure to use the module(panel) with in the specified temperature.

14.2 Avoid to display the fixed pattern in a long period, otherwise, it will cause image sticking.

14.3 Please operate module(panel) in suitable temperature. The performance will drift by different temperature.

14.4 Avoid dust or oil mist during assembly.

14.5 Follow the correct power on/off sequence while operating for preventing abnormal display or permanent damage to display.

14.6 Please be sure to turn-off the power when connecting or disconnecting the circuit.

14.7 High temperature and humidity may degrade performance. Please keep module away from direct sunlight or fluorescent light,

14.8 Avoid acetic acid or chlorine touch the AMOLED display module(panel).

14.9 Storage the modules(panel) in suitable environment with regular packing.

14.10 Polarizer scratches easily, please handle it carefully.

14.11 Sudden temperature changes cause condensation, and it will cause polarizer damaged.