

Product Specification

SPECIFICATION FOR APPROVAL

() Preliminary Specification

(◆) Final Specification

Title	13.3" QXGA OLED
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Customer	Lenovo
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	POF133F2048E
Suffix	EPA1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

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Product Specification

Contents

No	ITEM	Page
	COVER	1
	CONTENTS	2
	RECORD OF REVISIONS	3
1	GENERAL DESCRIPTION	4
2	ABSOLUTE MAXIMUM RATINGS	5
3	ELECTRICAL SPECIFICATIONS	6
3-1	OLED ELECTRICAL CHARACTERISTICS	6
3-2	EL ELECTRICAL CHARACTERISTICS	7
3-3	INTERFACE CONNECTIONS	8
3-4	eDP SIGNAL TIMING SPECIFICATIONS	9
3-5	SIGNAL TIMING SPECIFICATIONS	14
3-6	SIGNAL TIMING WAVEFORMS	14
3-7	COLOR INPUT DATA REFERENCE	15
3-8	POWER SEQUENCE	16
3-9	TOUCH GENERAL SPECIFICATIONS	17
4	OPTICAL SPECIFICATIONS	18
5	MECHANICAL CHARACTERISTICS	21
6	RELIABILITY	24
7	INTERNATIONAL STANDARDS	25
7-1	SAFETY	25
7-2	ENVIRONMENT	25
8	PACKING	26
8-1	DESIGNATION OF LOT MARK	26
8-2	PACKING FORM	26
8-3	PACKING ASSEMBLY	27
8-4	PALLET ASSEMBLY	28
9	PRECAUTIONS	29
	APPENDIX A. LGD PROPOSAL FOR eDP INTERFACE DESIGN GUIDE	31
	APPENDIX B. LGD PROPOSAL FOR SYSTEM DESIGN	39
	APPENDIX C. ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA	42

Product Specification

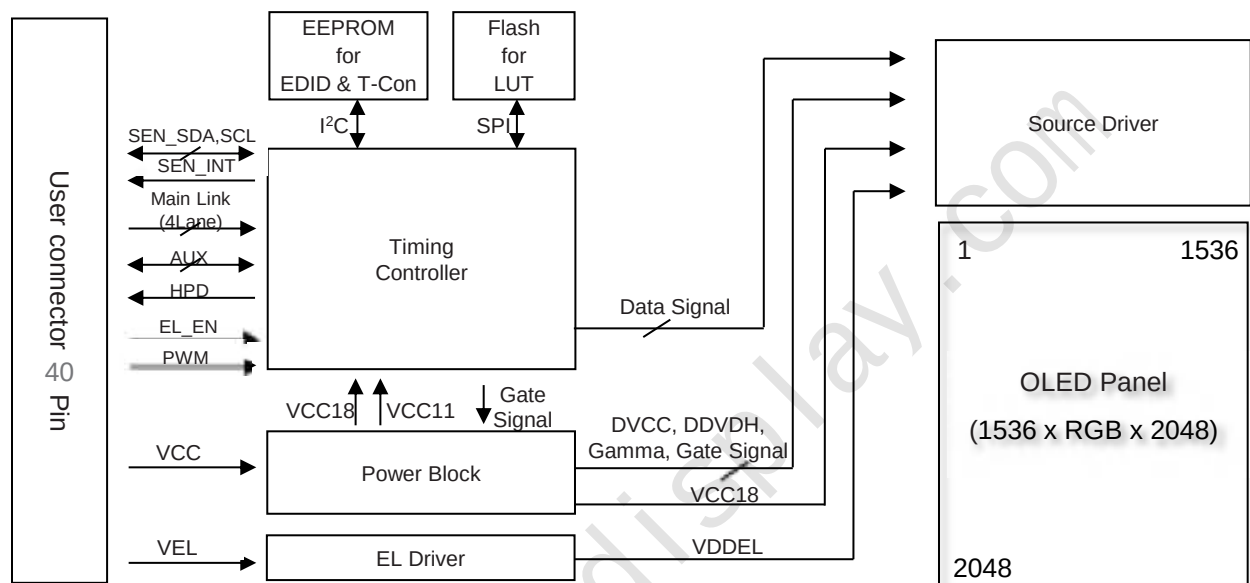
Record of Revisions

Revision No	Revision Date	Page	Before	After	EDID version
0.0	Apr. 24. 2019	All	First Draft (Preliminary Specification)	-	0.1
0.1	Jul. 12. 2019	14	f_{CLK} (214.6), t_{VP} (2108), t_{VBP} (47)	f_{CLK} (215.0), t_{VP} (2112), t_{VBP} (51) ; To optimize refresh rate 60Hz	
		16	T16 = 10ms	T16 = 40ms ; ; For EL Discharging	
		18	- Color Gamut 100% -	Update Color Tolerance to ± 0.02 , 0.03 Color Gamut 111% Update Viewing Angle to Max 0.07 @45°	
		19	-	Update Condition of Gray Scale	
		39-41	Check sum "BB"	Check sum "8F"	0.2
0.2	Nov. 21. 2019	9	-	Update PWM input Capacitor	
		16	-	Update T_D	
		4, 18	-	Add Luminance @ OPR 100%	
		18	-	Update Color Coordinates (R,G,B)	
		18	Color Gamut111% (NTSC Only) Viewing angle Spec @45° only	Update Color Gamut 95% (Adobe, DCI-P3) Update Viewing Angle Spec @60°	
		22,23	-	Need to Update	
		25	-	Update Safety	
		26	-	Label Information	
		39-41	Check sum "8F"	Check sum "17"	0.3
0.3	Jan. 16. 2020	4,6	Logic Power 1.6W	Logic Power 1.65W	
		18	Rx : 0.693, Gx : 0.185, By : 0.057	Rx : 0.695, Gx : 0.176 By : 0.056	
		22,23	-	Update Dimension	
		25	-	Update Label (Barcode L1KG→L2KG, Add MADE IN KOREA, Note1.YEAR)	
0.4	Jan. 21 2020	7	-	Add VEL Ripple Spec.	
		18	-	Update Luminance Max.	
		38-40	Check sum "17"	Check sum "EB" ; Update Color Coordinates & Year	0.4
0.5	Mar. 11 2020	4,6	Logic Power 1.65W	Logic Power 1.7W	
		7	-	Update PWM resolution	
		22,23	-	Update Dimension	
		25	-	Update Standards-Environment	
1.0	Apr. 22 2020	21	-	Update Static Folding	
		22~23	-	Update Dimension	
		39~40	-	APPENDIX B. LGD Proposal for System Design	
1.1	May 28 2020	22~23	-	Update GND and no component area	
1.2	Oct. 23 2020	41	-	APPENDIX B. LGD Proposal for PCB Shielding Guide	
1.3	Nov. 05 2020	26	-	Update Label	

Product Specification

1. General Description

The POF133F2048E is a Color Active Matrix Organic Light Emitting Diode Display (OLED). The matrix employs Low Temperature Poly Si Transistor as the active element. It is a top emission display type. It has a 13.3 inch diagonally measured active display area with QXGA resolution (1536 horizontal by 2048 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus, presenting a palette of more than 16.7M colors. The POF133F2048E has been designed to apply the interface method that enables high speed, low EMI, eDP interface with PSR. The POF133F2048E is intended to support applications where thin thickness, high contrast ratio, high color gamut. The POF133F2048E characteristics provide an excellent foldable display for Portable or Monitor mode such as tablet or notebook PC.



General Features

Active Screen Size	13.3 inches diagonal					
Outline Dimension	213.80 (H, typ.) x 284.80 (V, typ.) x 0.53 (D, typ) [mm] (w/o PCB)					
Pixel Pitch	0.132 mm X 0.132 mm					
Pixel Format	1536 horiz. by 2048 vert. Pixels RGB Tri-angle arrangement					
Color Depth	8-bit, 16.7M colors					
Luminance, White	300 cd/m ² (Center 1point, Typ., OPR 80%) 240 cd/m ² (Center 1point, Typ., OPR 100%)					
Power Consumption	Total 10.44W (Typ.) Logic : 1.7W (Typ. @ Mosaic), EL : 8.74W (Typ. @ Full White)					
Weight	120g (Max.)(w/o Protect Film)					
Bending Radius	3R (Typ.)					
Surface Treatment	Glare, Hard coat (6H Cover Window Only) and Anti Fingerprint					
RoHS Compliance	YES					
BFR / PVC / As Free	YES					
eDP version(T-con)	eDP1.3					
DPCD version	Ver1.2					
PSR	MBO	DPST	sDRRS	SSC	NVSR	G-sync or Free sync
Support	Not support	Not support	Not support	Support	Not support	Not support

Product Specification

2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

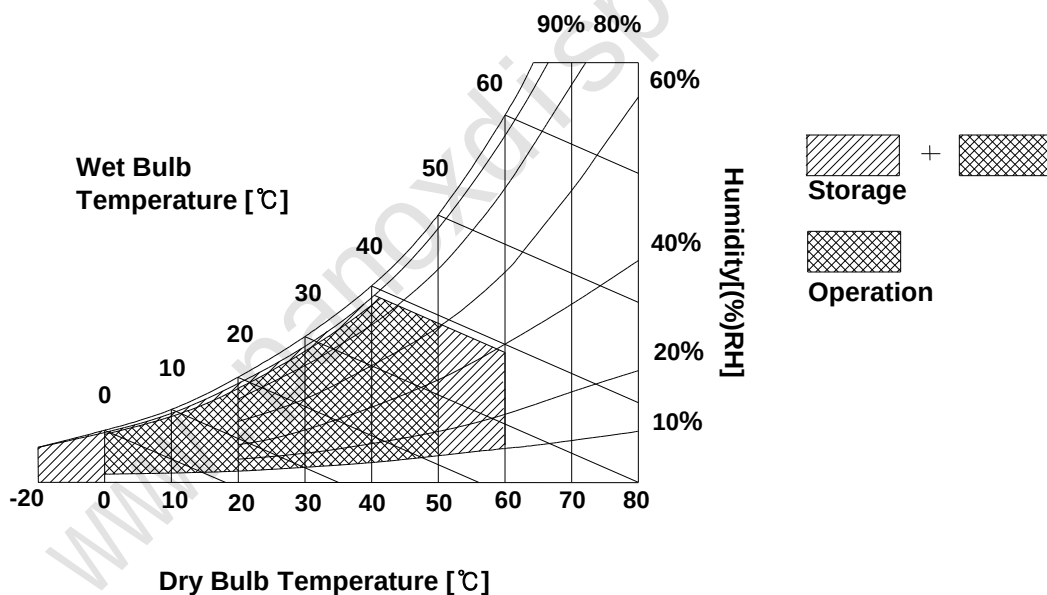
Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	V _{DC}	at 25 ± 2°C
Operating Temperature	T _{OP}	0	50	°C	1
Storage Temperature	T _{ST}	-20	60	°C	1,2
Operating Ambient Humidity	H _{OP}	10	90	%RH	1
Storage Humidity	H _{ST}	10	90	%RH	1,2

Note : 1. Temperature and relative humidity range are shown in the figure below.

Wet bulb temperature should be 39°C Max, and no condensation of water.

Note : 2. Storage Condition is guaranteed with unfolding under packing condition.



Product Specification

3. Electrical Specifications

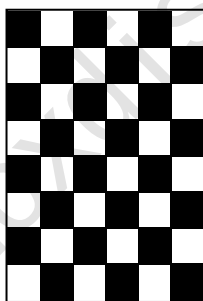
3-1. OLED Electrical Characteristics

Table 2. ELECTRICAL CHARACTERISTICS

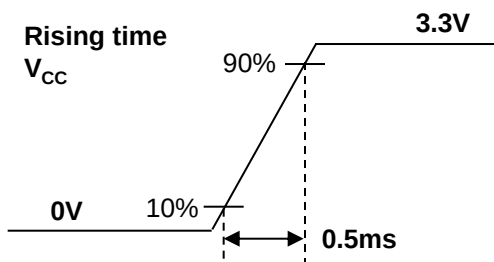
Parameter	Symbol	Values			Unit	Notes
		Min	Typ	Max		
Power Supply Input Voltage	V_{CC}	3.0	3.3	3.6	V	1
Permissive Power Supply Input Ripple	V_{CCrp}	-	-	100	mV _{p-p}	
Power Supply Input Current	Mosaic I_{CC}	-	515	605	mA	2
Power Consumption	P_{CC}	-	1.7	2.0	W	
Power Supply Inrush Current	I_{CC_P}	-	-	2.5	A	3
Differential Impedance	Z_{eDP}	90	100	110	Ω	

Note)

- The measuring position is the connector of Module and the test conditions are under 25°C, $f_v = 60\text{Hz}$
- The specified I_{CC} current and power consumption are under the $V_{CC} = 3.3\text{V}$, 25°C, $f_v = 60\text{Hz}$ condition and Mosaic pattern. (without Burning Compensation)



- The V_{CC} rising time is same as the minimum of T1 at Power on sequence.



Product Specification

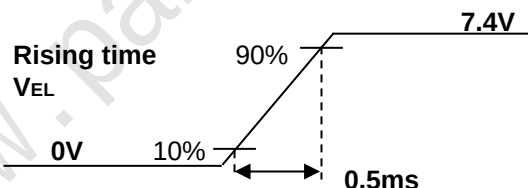
3-2. EL Electrical Characteristics

Table 3. EL ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
EL Power Input Voltage		V_{EL}	4.8	7.4	9.0	V	1
Permissible EL Power Input Ripple		V_{ELrp}	-	-	100	mV _{p-p}	
EL Power Input Current		I_{EL}		1180	1475	mA	2
EL Power Consumption		P_{EL}		8.74	11.0	W	
EL Power Inrush Current		I_{EL_P}	-	-	5.0	A	3
PWM Duty Ratio			1	-	100	%	4
PWM resolution			8			bit	5
PWM Frequency		F_{PWM}	200	-	1000	Hz	6
PWM	High Level Voltage	V_{PWM_H}	2.5	-	3.6	V	
	Low Level Voltage	V_{PWM_L}	0	-	0.3	V	
	Rising Time	T_{r_PWM}	-	-	500	ns	
	Falling Time	T_{f_PWM}	-	-	500	ns	
EL_EN	High Voltage	$V_{EL_EN_H}$	2.5	-	3.6	V	
	Low Voltage	$V_{EL_EN_L}$	0	-	0.3	V	
Life Time (B10)			-	15,000	-	Hrs	7

Note)

- The measuring position is the connector of OLED Module and the test conditions are under 25°C.
- The current and power consumption with EL Driver are under the $V_{EL} = 7.4V$, 25°C, PWM Duty 100% and White pattern(OPR 100%, 240nit) with the normal frame frequency operated(60Hz)
This model apply to enable PLC(Peak Luminance Control)
- The V_{EL} rising time is same as the minimum of T13 at Power on sequence.

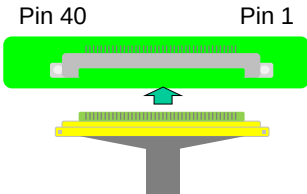


- The operation of EL Driver below minimum dimming ratio may cause flickering or reliability issue.
- 8bit resolution means it's possible to change PWM duty by 0.4% step.
- This Spec. is not effective at 100% dimming ratio as an exception because it has DC level equivalent to 0Hz.
In spite of acceptable range as defined, the PWM Frequency should be fixed and stable for more consistent brightness control at any specific level desired.
- The life time is determined as the time at which brightness of OLED is 50% compare to that of minimum value specified in table 7. under general user condition.

Product Specification

3-3. Interface Connections

Table 4. MODULE CONNECTOR PIN CONFIGURATION (CN11)

Pin	Symbol	Description	Notes
1	VCC_logic	logic and driver power	[Connector] Hirose, KN38A-40S-0.5H (40pin, 0.5pitch) or equivalent [Connector pin arrangement] 
2	VCC_logic	logic and driver power	
3	VCC_logic	logic and driver power	
4	VCC_logic	logic and driver power	
5	SEN_INT	Sensing command	
6	SEN_SCL	Sensing command	
7	SEN_SDA	Sensing command	
8	GND	High Speed Ground	
9	LANE3_N	Complement Signal Link Lane 3	
10	LANE3_P	True Signal Link Lane 3	
11	GND	High Speed Ground	
12	LANE2_N	Complement Signal Link Lane 2	
13	LANE2_P	True Signal Link Lane 2	
14	GND	High Speed Ground	
15	LANE1_N	Complement Signal Link Lane 1	
16	LANE1_P	True Signal Link Lane 1	
17	GND	High Speed Ground	
18	LANE0_N	Complement Signal Link Lane 0	
19	LANE0_P	True Signal Link Lane 0	
20	GND	High Speed Ground	
21	AUX_CH_P	True Signal Auxiliary Channel	
22	AUX_CH_N	Complement Signal Auxiliary Channel	
23	GND	High Speed Ground	
24	HPD	HPD signal pin	
25	EL_EN	EL on/off control	
26	EL_PWM	System PWM signal input for dimming	
27	BIST or NC	Panel Self Test Enable (Optional)	
28	GND	EL ground	
29	GND	EL ground	
30	GND	EL ground	
31	GND	EL ground	
32	NC	Reserved for OLED manufacturer's use	
33	VEL	EL power (7.4V Typical)	
34	VEL	EL power (7.4V Typical)	
35	VEL	EL power (7.4V Typical)	
36	VEL	EL power (7.4V Typical)	
37	VEL	EL power (7.4V Typical)	
38	VEL	EL power (7.4V Typical)	
39	VEL	EL power (7.4V Typical)	
40	VEL	EL power (7.4V Typical)	

Note) This pin-map is not VESA Standard but customized map.

3-3-1. Input/output signal circuit

Figure1.HPD Output circuit is as below

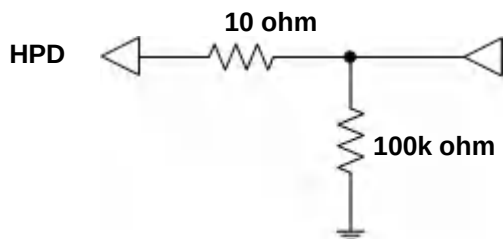


Figure2.EL PWM input circuit is as below

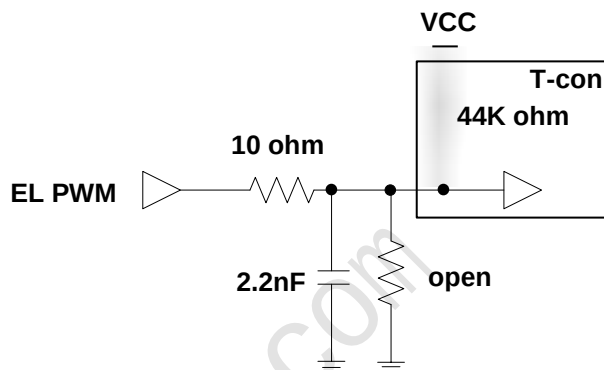


Figure3.EL Enable input circuit is as below

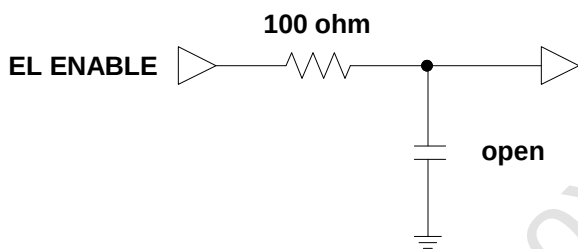
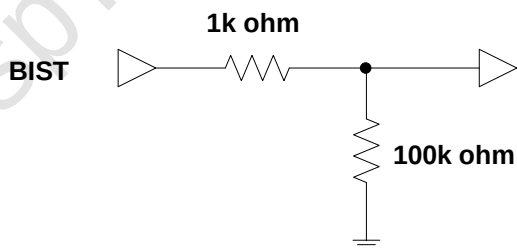


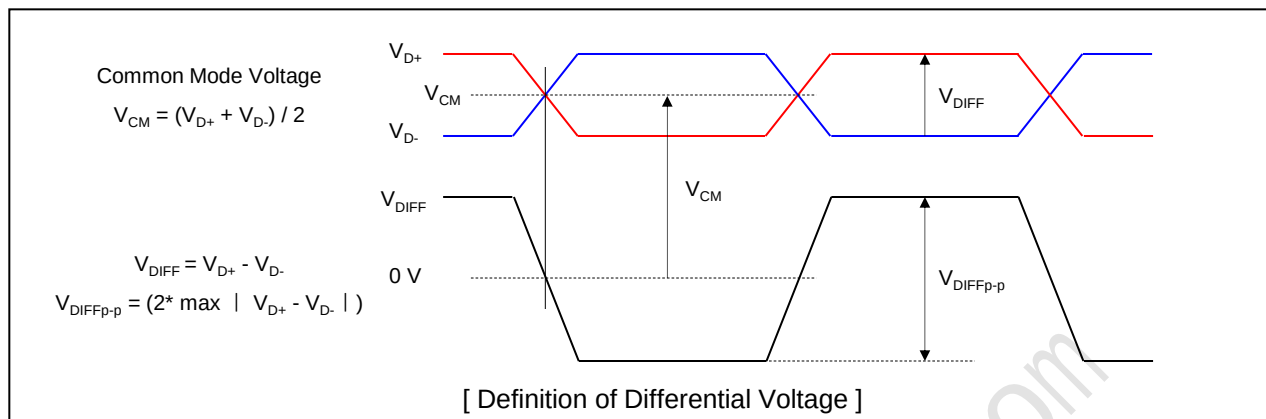
Figure4.BIST input circuit is as below



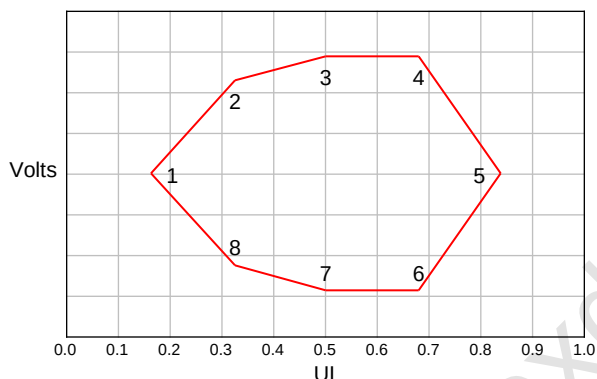
Product Specification

3-4. eDP Signal Timing Specifications

3-4-1. Definition of Differential Voltage



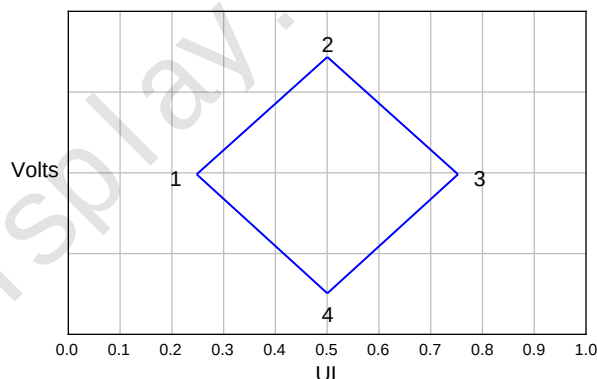
3-4-2. Main Link EYE Diagram



[EYE Mask at Source Connector Pins]

Point	Reduced Bit Rate		High Bit Rate	
	Time(UI)	Voltage(V)	Time(UI)	Voltage(V)
1	0.127	0.000	0.210	0.000
2	0.291	0.160	0.355	0.140
3	0.500	0.200	0.500	0.175
4	0.709	0.200	0.645	0.175
5	0.873	0.000	0.790	0.000
6	0.709	-0.200	0.645	-0.175
7	0.500	-0.200	0.500	-0.175
8	0.291	-0.160	0.355	-0.140

[EYE Mask Vertices at Source Connector Pins]



[EYE Mask at Sink Connector Pins]

Point	Reduced Bit Rate		High Bit Rate	
	Time(UI)	Voltage(V)	Time(UI)	Voltage(V)
1	0.375	0.000	0.246	0.000
2	0.500	0.023	0.500	0.075
3	0.625	0.000	0.755	0.000
4	0.500	-0.023	0.500	-0.075

[EYE Mask Vertices at Sink Connector Pins]

Point	Reduced Bit Rate		High Bit Rate	
	Time(UI)	Voltage(V)	Time(UI)	Voltage(V)
1	0.270	0.000	0.246	0.000
2	0.500	0.068	0.500	0.075
3	0.731	0.000	0.755	0.000
4	0.500	-0.068	0.500	-0.075

[EYE Mask Vertices at embedded DP Sink Connector Pins]