SPECIFICATION
Of AMOLED MODULE

CUSTOMER	
PROJECT Name.	**固曲 w/o TP/FC**

PREPARED BY	CHECKED BY	APPROVED BY

REVERSION HISTORY

Rev No.	Rev Date	Content	Remark
V01	20200710	First release	/

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1. General Specifications

Feature		Spec	Remark
General Spec	Size	7.8 inch	
	Active Area	118.8(W) x 158.4（H)	mm
	Resolution	1440 x 1920	
	PPI	308	
	Aspect Ratio	4:3	
	Power consumption	2.7W @ 300 nits Full White	
	Color Depth	16.7 M (3*8bit)	
	Interface	2 port MIPI	
	Surface Treatment	TBD，具体项目根据盖板匹配	
	Surface Hardness	TBD，具体项目根据盖板匹配	
	Overall Dimention LxHxD (mm)	TBD，具体项目根据盖板匹配	Note 1
	Frame Frequency	Diver IC : 60Hz	

Note 1. The height dimension doesn't include any protect films and electronic components on FPC.

2. Pin Assignment

Mating connector type: BTB

PIN No.	Symbol	I/O	Descriptions
1	ELVDD_FB	P	ELVDD Sense Pin For Power IC FeedBack
2	NC	-	NC
3	AVDD	P	Power supply for analog circuit and driver output
4	NC	-	NC
5	NC	-	NC
6	GND	P	Ground
7	VCI	P	Power supply for analog system & TP
8	NC	-	NC
9	VDDIO	P	Power supply for digital system & TP
10	GND	P	Ground
11	RSTX	I	Reset for AMOLED SIGNAL
12	EN	O	Power IC enable control pin, If not used, Please leave this pin open
13	SWIRE	O	Swire protocol setting pin of power IC, If not used, Please leave this pin open
14	GND	P	Ground
15	P1_D3P	I	DSI-D3+differential data signals of Port 1
16	P1_D3N	I	DSI-D3-differential data signals of Port 1
17	GND	P	Ground
18	P1_CLKP	I	CLK+ differential clock signals of Port 1
19	P1_CLKN	I	CLK- differential clock signals of Port 1
20	GND	P	Ground
21	P1_D0P	I	DSI-D0+differential data signals of Port 1.
22	P1_D0N	I	DSI-D0-differential data signals of Port 1.
23	GND	P	Ground
24	P0_D2P	I	DSI-D2+differential data signals of Port 0.

25	P0_D2N	I	DSI-D2-differential data signals of Port 0.
26	GND	P	Ground
27	P0_D1P	I	DSI-D1+differential data signals of Port 0.
28	P0_D1N	I	DSI-D1-differential data signals of Port 0.
29	GND	P	Ground
30	GND	P	Ground
31	P0_D0N	I	DSI-D0-differential data of Port 0.
32	P0_D0P	I	DSI-D0+differential data of Port 0.
33	GND	P	Ground
34	P0_CLKN	I	CLK- differential clock signals of Port 0.
35	P0_CLKP	I	CLK+ differential clock signals of Port 0
36	GND	P	Ground
37	P0_D3N	I	DSI-D3-differential data of Port 0.
38	P0_D3P	I	DSI-D3+differential data of Port 0.
39	GND	P	Ground
40	P1_D1N	I	DSI-D1-differential data of Port 1.
41	P1_D1P	I	DSI-D1+differential data of Port 1.
42	GND	P	Ground
43	P1_D2N	I	DSI-D2-differential data of Port 1.
44	P1_D2P	I	DSI-D2+differential data of Port 1.
45	GND	P	Ground
46	NC	-	NC
47	TE	O	TE for TP SIGNAL
48	INT18	O	INT for TP SIGNAL(1.8V Logic Level)
49	RST18	I	Reset for TP SIGNAL(1.8V Logic Level)
50	SDA18	I/O	SDA for TP SIGNAL(1.8V Logic Level)
51	SCL18	I/O	SCL for TP SIGNAL(1.8V Logic Level)
52	NC	-	NC
53	GND	P	Ground
54	NC	-	NC
55	NC	-	NC
56	GND	P	Ground
57	SPI_SDI	I/O	SDI for De-Mura FLASH, Please leave this pin open
58	SPI_SDO	O	SDO for De-Mura FLASH, Please leave this pin open
59	SPI_CSN	I	CS for De-Mura FLASH, Please leave this pin open
60	SPI_SCLK	I/O	CLOCK for De-Mura FLASH, Please leave this pin open
61	ELVDD	P	OLED Positive Power
62	GND	G	Ground

Note1: I/O definition: I---Input, O---Output, P--- Power/Ground.
Note2: All of GND pins should be connected to system ground.
Note3: Pin57~60 are used as SPI interface at Royole Display side. Please leave this pin open.
Note4: Recommended Connector: Kyocera 245863060104829+.

3. Absolute Maximum Ratings

GND=0V, Ta = 25℃

Item	Symbol	Min	Max	Unit	Remark
OLED power supply	ELVDD	-0.3	10.0	V	
Power supply for analog circuit and driver output	AVDD	-0.3	8.8	V	
Digital power supply	VDDIO	-0.3	3.6	V	
Analog power supply	VCI	-0.3	3.6	V	

Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	70	℃	

Note1: Ta temperature is the surface temperature of module.
Note2: If the voltage exceeds its absolute maximum ratings, the module may be damaged. Also, If the module is operated with the absolute maximum ratings for a long time, it will present risks on the reliability of the module.

4. Electrical Characteristics

4.1 DC Characteristics for Panel Driving

GND =AGND=0V, Ta = 25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
OLED power supply	ELVDD	-	6.0	-	V	
Power supply for analog circuit and driver output	AVDD	-	6.4	-	V	
Digital power supply	VDDIO	1.65	1.8	3.6	V	
Analog power supply	VCI	3.0	3.3	3.6	V	
Input signal level	V_{IH}	0.8*VDDI	-	VDDI	V	T=25℃
	V_{IL}	0	-	0.2*VDDI	V	T=25℃

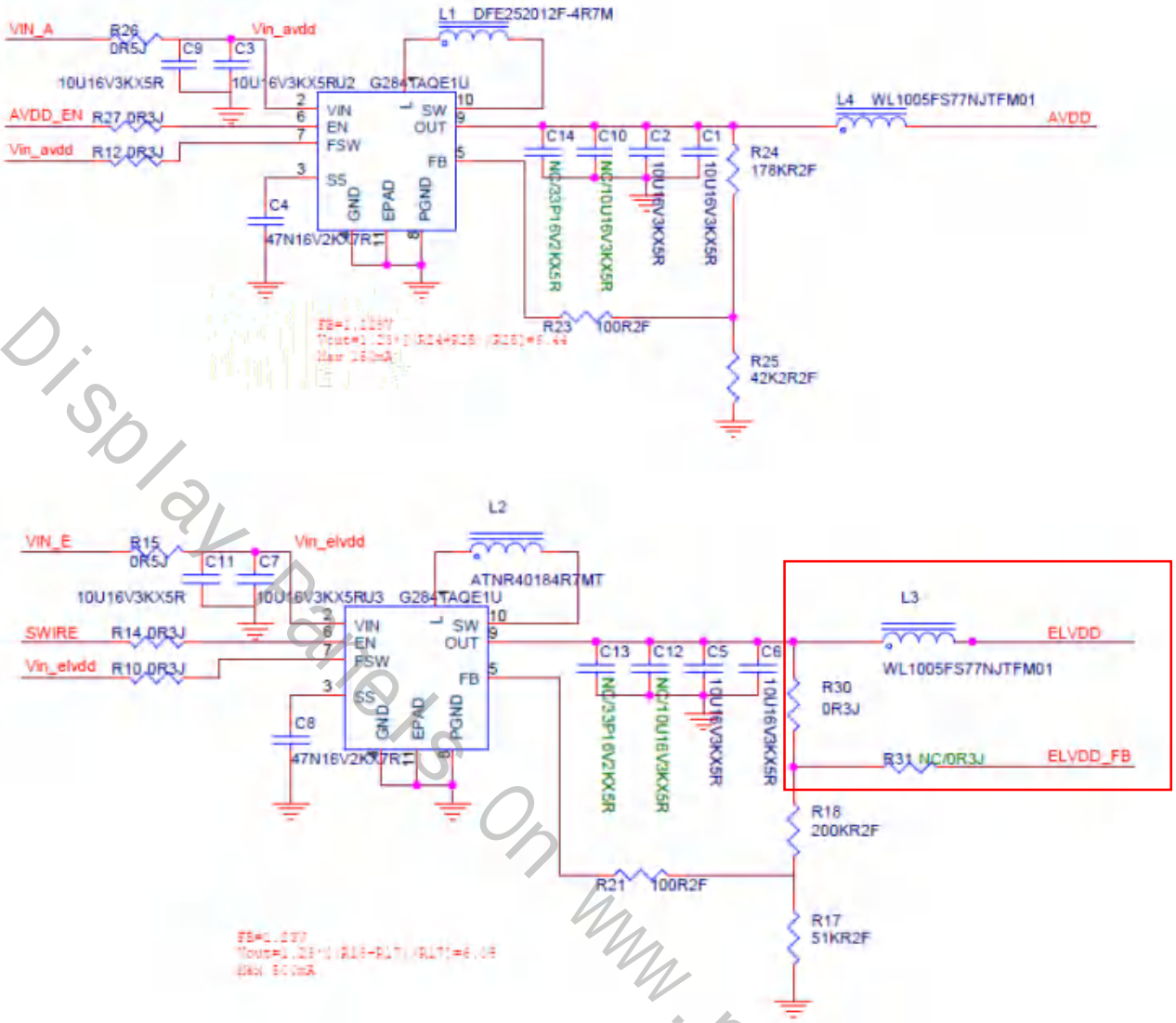
Note 1: Normal functions are guaranteed under the recommended operating conditions only. Functions are not guaranteed if unstable voltage supply occurs during the operation. To prevent such impact, a bypass capacitor must be inserted into the line closed to the power pin.

4.2 Display Current Consumption

Mode	Symbol	Condition(TBD)		Min	Typ	Max	Unit	Remark
Normal	I_{AVDD}	AVDD=6.4V VCI=3.3V VDDIO=1.8V ELVDD=6V		-	68	-	mA	Note1
	I_{VCI}			-	18	-	mA	
	I_{VDDIO}			-	68	-	mA	
	I_{ELVDD}			-	350	-	mA	
Sleep in	I_{AVDD}			-	/	-	uA	Display Off
	I_{VCI}			-	/	-	mA	
	I_{VDDIO}			-	/	-	mA	
	I_{ELVDD}			-	/	-	mA	

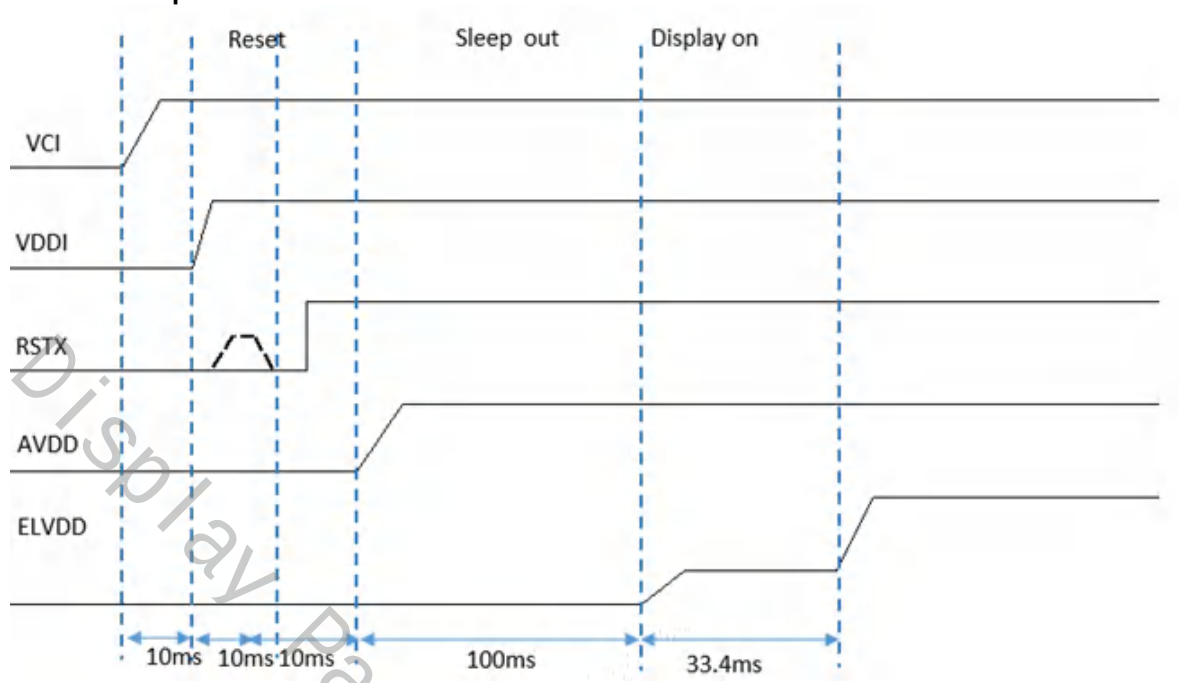
Note1:Test pattern -- White

4.3 Recommend DC/DC Power IC Application Circuit(G2841A)

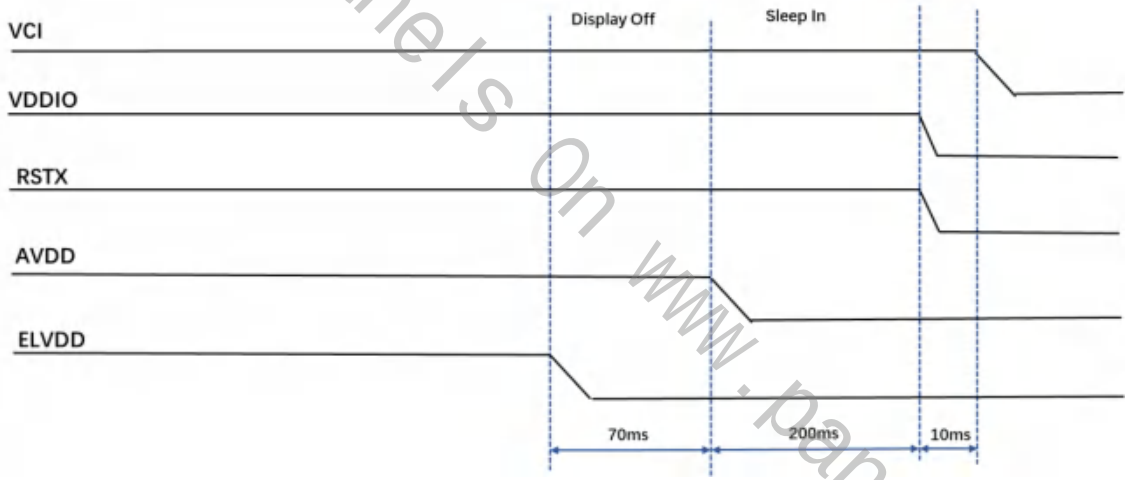


4.4 Recommended Power ON/OFF Sequence

Power ON Sequence



Power OFF Sequence



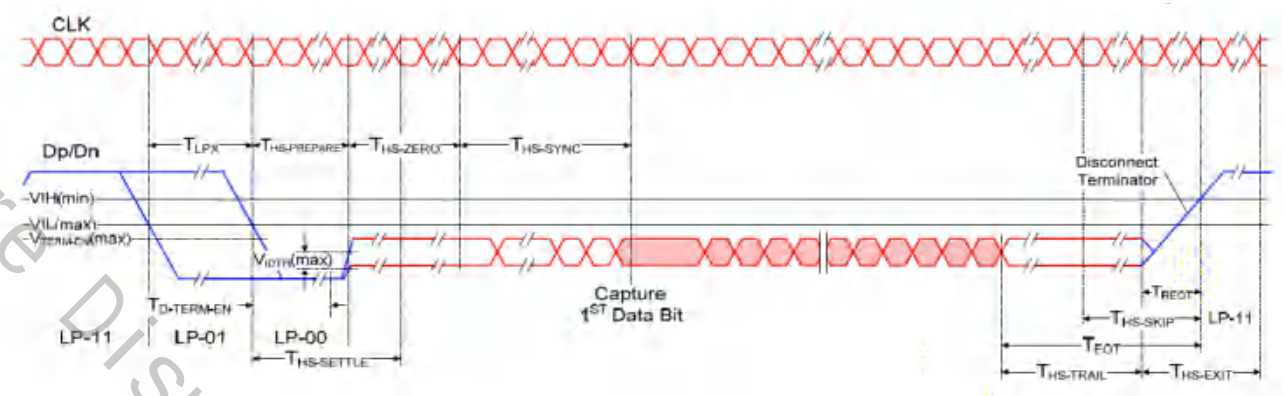
4.5 DC Characteristics for Touch Driving

Description	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply input for analog circuit	VCI	3.0	3.3	3.6	V	
I2C clock input	SCL18	0	1.8	2.1	V	IOVCC=1.8V
I2C data pin	SDA18	0	1.8	2.1	V	IOVCC=1.8V
External Reset, Low is active	RST18	0	1.8	2.1	V	IOVCC=1.8V
Interrupt	INT18	0	1.8	2.1	V	IOVCC=1.8V
Ground	GND	0	0	0	V	
Input Signal Level	V_{IH}	0.7*IOVCC	IOVCC	IOVCC+0.3	V	T=25℃
	V_{IL}	0	0	0.3*IOVCC	V	T=25℃

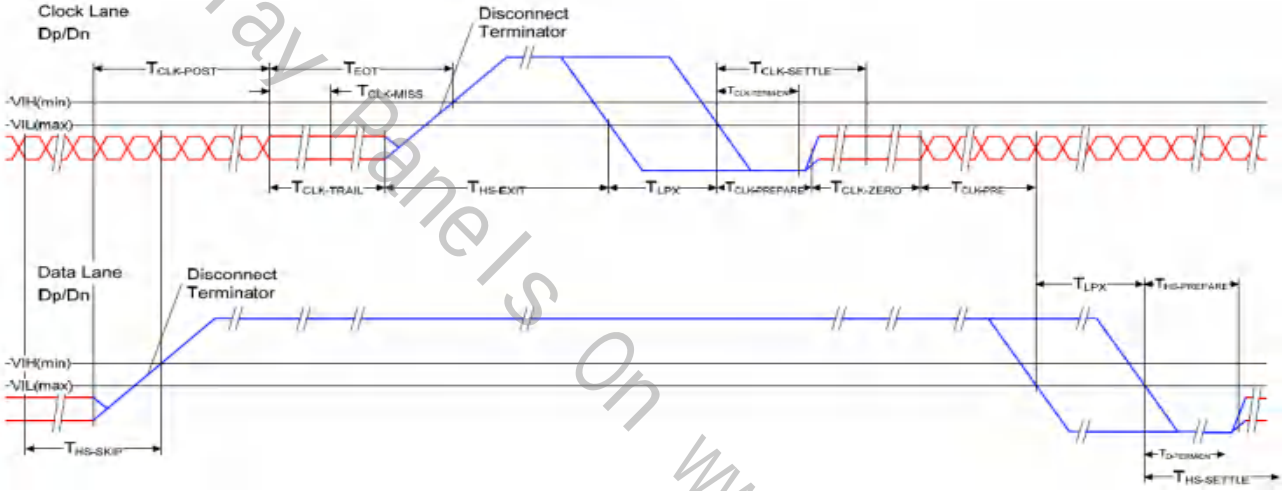
5. Timing Characteristics

5.1 MIPI Interface Characteristics

HS Data Transmission Burst



HS clock transmission

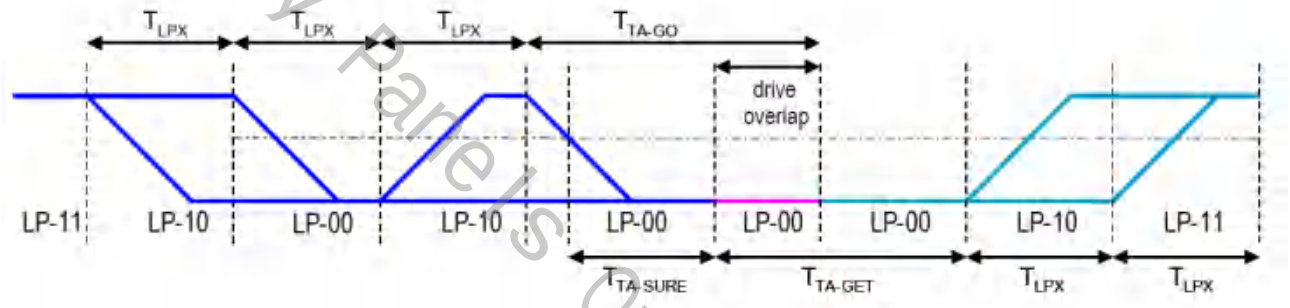


Timing Parameters (for 5.1)

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	-		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI

$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX .	-		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

Bus Turnaround Procedure (From MPU to display module)



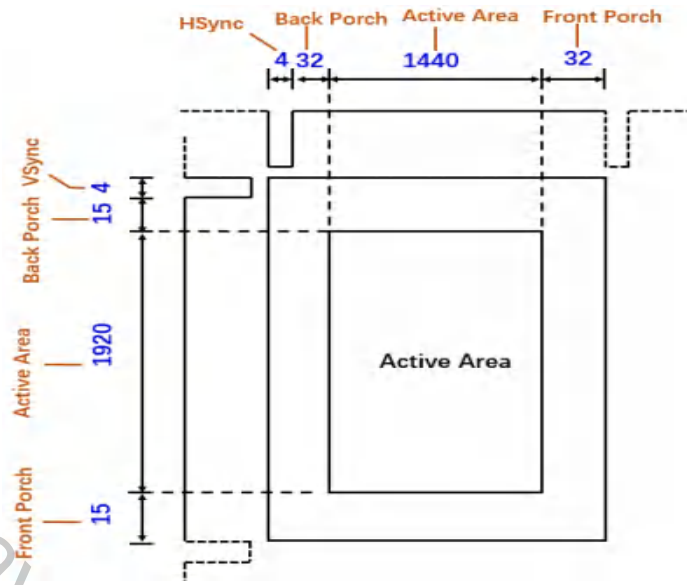
Timing Specifications for Low Power Transmission:

Parameter	Description	Min	Typ	Max	Unit	Remark
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		150	ns	Note1 Note2
$T_{TA-SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX(M)		2*TLPX(M)	ns	Note2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		150	ns	Note1 Note2
$T_{TA-GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*TLPX(D)		ns	Note2
$T_{TA-GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*TLPX(D)		ns	Note2
$T_{TA-SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX(D)		2*TLPX(D)	ns	Note2

Note1: TLPX is an internal state machine timing reference. Externally measured value may differ slightly from the specified values due to asymmetrical rise and fall times.
Note2: Transmitter-specific parameter

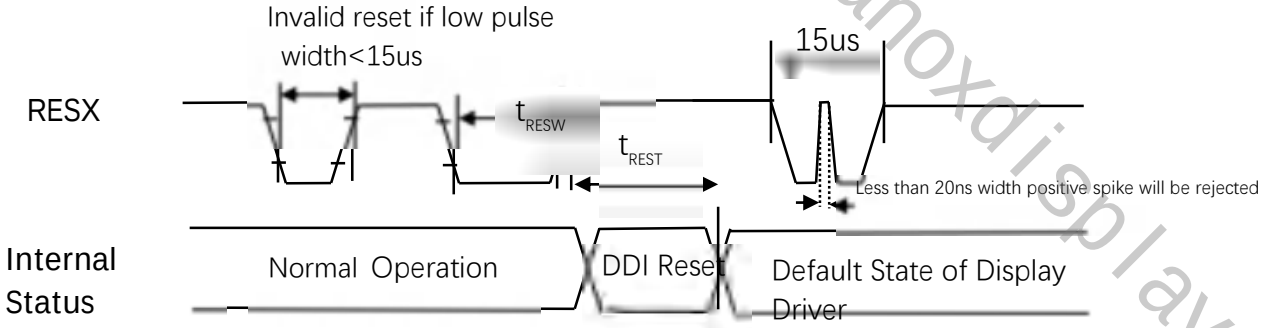
5.2 Video Mode Interface Timing Specification

5.2.1 Display Video Mode



Name	Quantity	Unit
Frame Rate	60	Hz
Line Time	8.5	Us
H Sync	4	Dot
H Back Porch	32	Dot
H Active	1440	Dot
H Front Porch	32	Dot
H Total	1508	Dot
V Sync	4	Line
V Back Porch	15	Line
V Active	1920	Line
V Front Porch	15	Line
V Total	1954	Line

6.2.2 DSI Video Mode Interface Timing



5.3 Reset Timing Characteristics

If Reset starts in Sleep-Out mode the display driver will enter blanking sequence with maximum time 120 msec. On the other hand, the display driver will remain in blanking state if

Reset occurs in Sleep-In mode and then return to IC's default sate soon after H/W reset. "Spike Rejection" also applies during a valid reset pulse as shown below.

During reset complete time (*t*REST), data in MTP will be re-loaded and latched to internal registers. This data re-load is done every time when there is an H/W reset and completes within 10ms after the rising edge of RESX. Therefore, it is necessary to wait at least 10ms after releasing RESX before sending commands. Also, the rising edge of RESX to Sleep-Out command should be longer than120msec.

Reset timing @VDDI=1.62V to 1.98V, VSS =0V

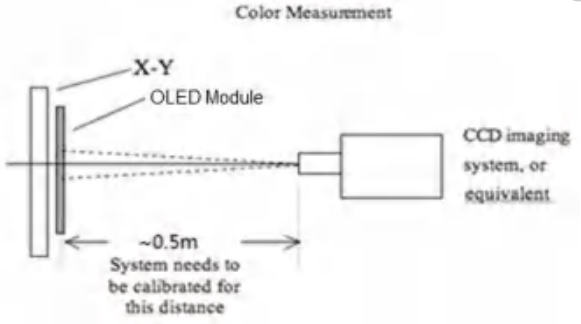
Symbol	Parameter	MIN	TYP	MAX	Note	Unit
tRESW	Reset low pulse width	15	-	-	1. Shorter than 5us, Reset rejected 2. Longer than 15μs, IC reset 3. Between 5μs and 15μs, It depends on voltage and temperature condition.	μs
tREST ms	Reset complete time	-	-	10	When reset applied at sleep-in mode	
		-		120	When reset applied at sleep-out mode ms	

6. Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
Brightness		L	--		300	--	cd/m^2	Note1 Note2
Contrast Ratio		CR			100,000	--		Note1 Note3
Brightness Uniformity		White state	9 points		80	--	%	Note1 Note4
View Angles		U	CR≥200	80	--	--	Degree	Note 5
		D		80	--	--		
		L		80	--	--		
		R		80	--	--		
Chromaticity	White	x		0.282	0.302	0.322	--	Note1 Note6
		y		0.295	0.315	0.335		
	Red	x		0.645	0.665	0.685		
		y		0.315	0.335	0.355		
	Green	x		0.215	0.245	0.275		
		y		0.680	0.710	0.740		
	Blue	x		0.114	0.134	0.154		
		y		0.040	0.060	0.080		
NTSC		--		84	99	--	--	
Crosstalk		--		--	2	--	%	Note 7

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room and a temperature of 25℃. After 5 minutes operation, the optical properties were measured at the center point of the AMOLED panel.



Item	Photo detector
Contrast Ratio	PR730
Brightness	PR730
Chromaticity	PR730
Brightness Uniformity	PR730

Note 2: Definition of Luminance

Measure the luminance of full white state at the center point.

Note 3: Definition of contrast ratio

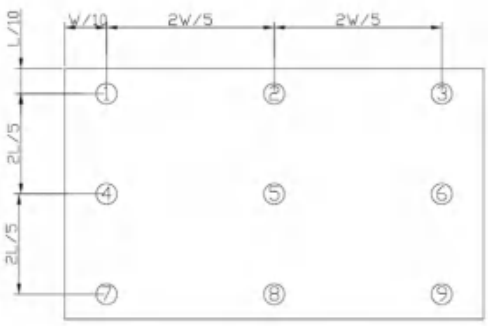
$$\textbf{Contrast Ratio} = \frac{\textbf{Luminance measured when the panel is on full white state}}{\textbf{Luminance measured when OLED is on full dark state}}$$

Note 4: Definition of Luminance Uniformity

The luminance uniformity is calculated by using following formula.

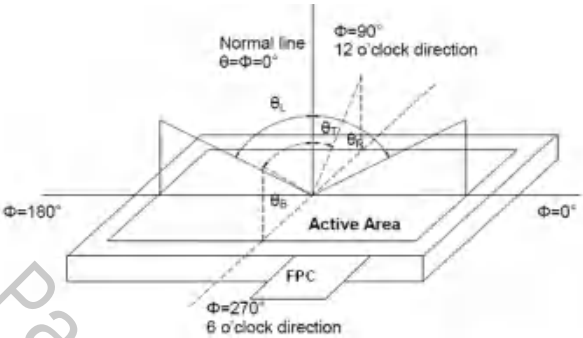
$$\text{Luminance uniformity (Lu)} = \frac{\text{Minimum luminance from ① to ⑨}}{\text{Maximum luminance from ① to ⑨}}$$

The luminance is measured at the 9 locations as shown below.



Note 5:

Definition of viewing angle range and measurement system



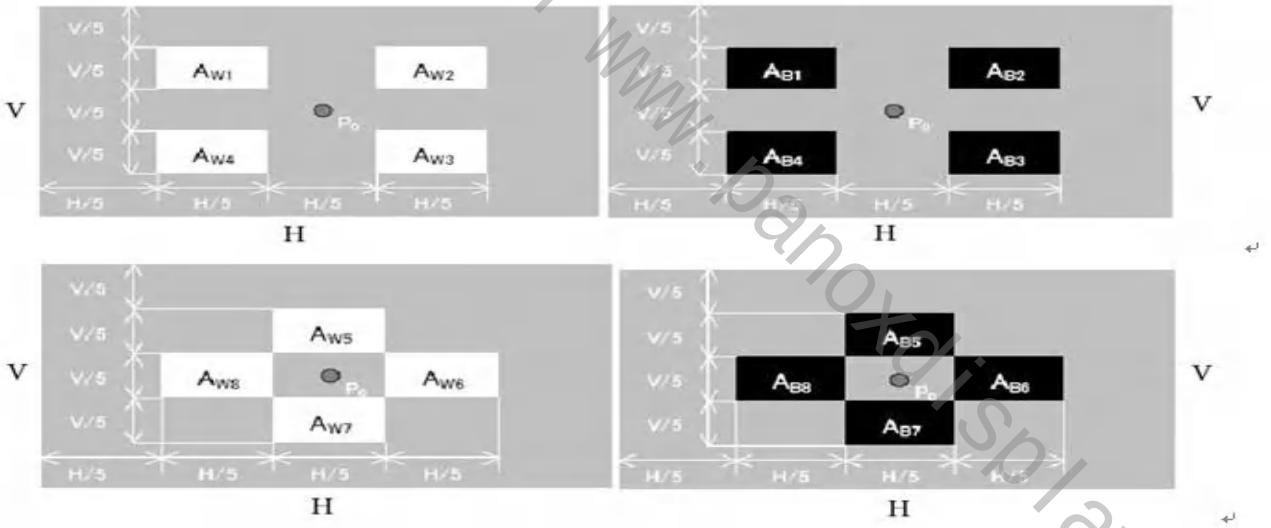
FPC at θ 270°

Note 6: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of the AMOLED panel.

Note 7: Definition of Crosstalk

4% black or white window,127 gray background.



$$L_{W\_OFF} = \frac{L_{W1} + L_{W2} + L_{W3} + L_{W4}}{4}$$

For white windows A_{Wi} (i = 5 to 8)

$$CT = \frac{|L_{Wi\_ON} - L_{W\_OFF}|}{L_{W\_OFF}} \times 100\%(i = 5\ to\ 8)$$

$$L_{B\_OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

For black windows A_{Bi} (i = 5 to 8)

$$CT = \frac{|L_{Bi\_ON} - L_{B\_OFF}|}{L_{B\_OFF}} \times 100\%(i = 5\ to\ 8)$$