0.5inch Micro-OLED（1600×1200）

Preliminary Specification

Model Name：

S050M1600M01

Revision

Version	Date	Description
V0.0	2023.6.21	Initial release

Contents

1. General Description

This display is a 0.5 inch diagonal, 1600(RGB) × 1200 dots active-matrix color OLED panel module based on single-crystal silicon transistors. This panel integrates panel driver and logic driver, and realizes small size, light weight, low power consumption and high resolution.
Applications: View finders, Head mounted displays, etc.

- 1600x1200 Real RGB Resolution
- Frame rate: 60Hz to 120Hz
- Normal operation supports full color mode: 16.7M colors (24-bit 8(R):8(G):8(B)) or 1.07B colors (30-bit 10(R):10(G):10(B))
- Interface
  -- MIPI + I2C
  -- MIPI DPHY v1.1 with 1 port (4 lanes, 1.0Gbps/Lane)
  -- MIPI DSI v1.02 r11 Video mode
  -- Support VESA-DSC v1.1 in-chip decoder (3:1 & 3.75:1 compression ratio)
  -- Support scaling up x1.33 (1200x900 to 1600x1200) and x2 (800x600 to 1600x1200)
- Scan direction selection, up or down and right or left
- Orbit supported
- Wide range Brightness adjustment
- Temperature compensation

2. General Feature

Item	Specification
Resolution	1600(H) x 1200 (V)
Number of dots	5.76M (1600x1200x3)
Pixel Size	6.3μm x 6.3μm
Useable Display Area	10.08mm x 7.56mm / 0.50" diagonal
Luminance	1000
Contrast Ratio	100,000:1 typical
Uniformity	> 85%
Power Consumption	500mW
Gray Levels	256 or 1024
Interface	MIPI (1port D-PHY)
Frame Rate	60Hz~120Hz
Weight	TBD
Operating Temperature	-40°C to +70°C
Storage Temperature	-40°C to +80°C

3. Optical Specification

Tpanel=30℃	Parameter	Min.	Typ.	Max.	Unit
Brightness	-	-	1000	-	cd/m2
CR	white to Black Contrast Ratio	-	100,000:1		
Uniformity	End to end large-area uniformity	85			%
CIE Red	CIE-x	-	0.650	-	
	CIE-y	-	0.330	-	
CIE Green	CIE-x	-	0.230	-	
	CIE-y	-	0.690	-	
CIE Blue	CIE-x	-	0.150	-	
	CIE-y	-	0.060	-	
CIE White	CIE-x	-	0.313	-	
	CIE-y	-	0.329	-	
DCI-P3			90%		
Frame rate		60		120	HZ
Power consumption(1600×1200Hz，DSC off，Full White)			500	-	mW

Note1: If there is no specified, the specification of optical is specified at 30 degrees Celsius.

Note2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. Brightness is measured as peak luminance at full white pattern (Gray level=255 with 8bits color depth);

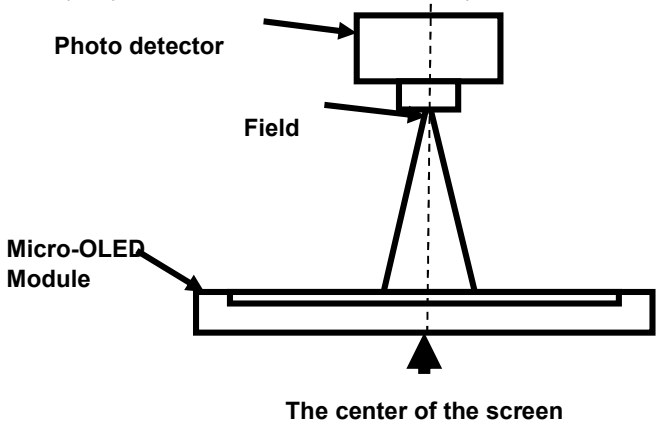


Fig.1

Note3: Definition of Uniformity at gray level255(8bits color depth) and 100%duty emission.

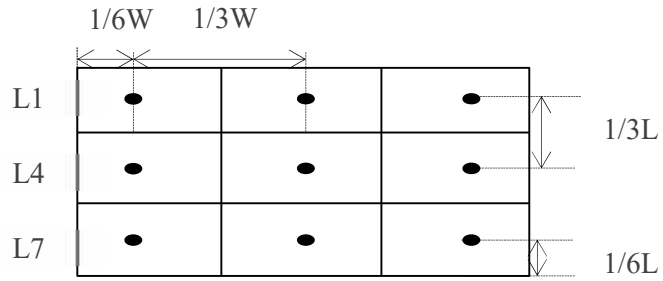
Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

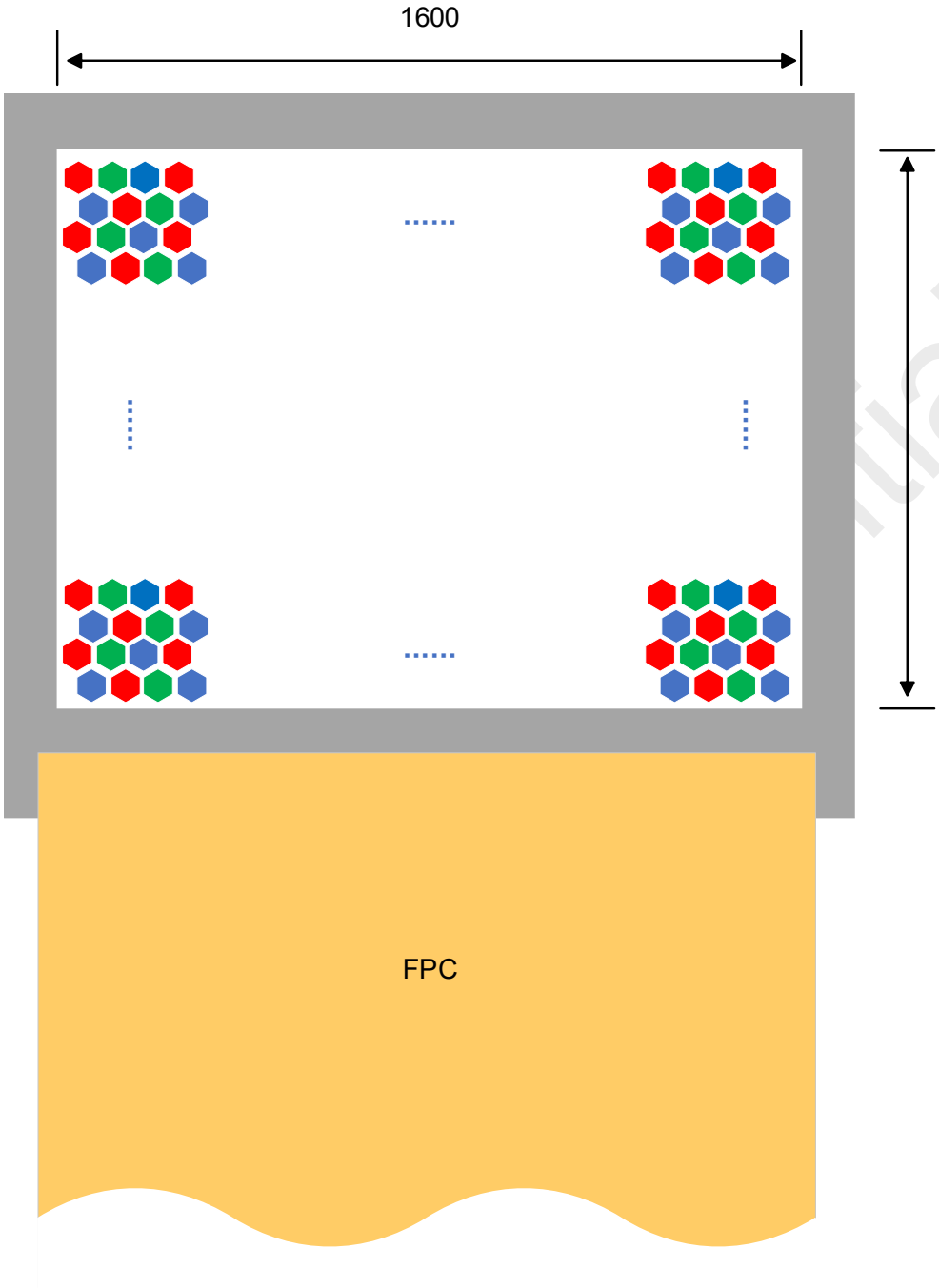
L-------Active area length; W----- Active area width

Lmax: The measured maximum luminance of all measurement position.

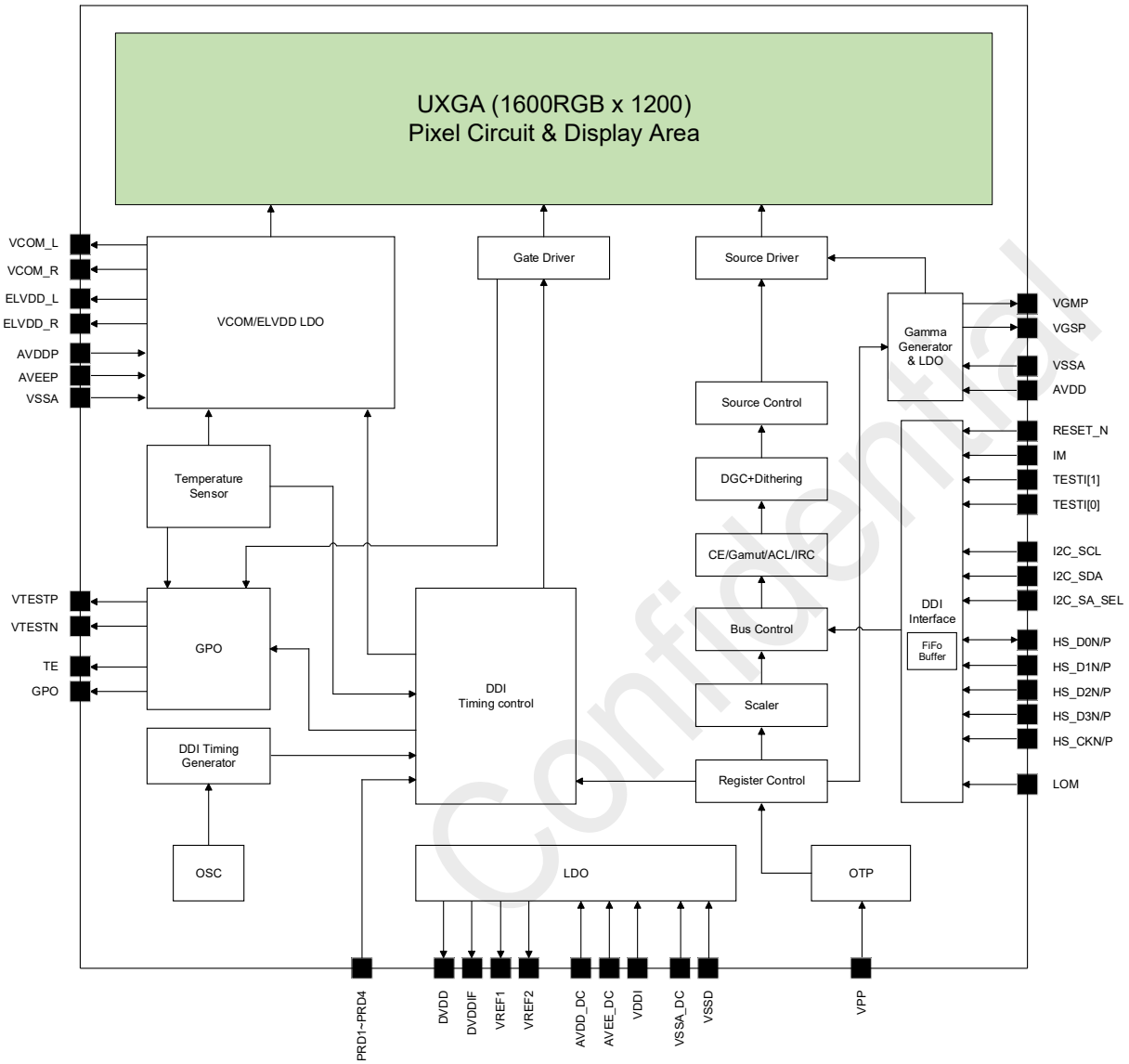
Lmin: The measured minimum luminance of all measurement position.



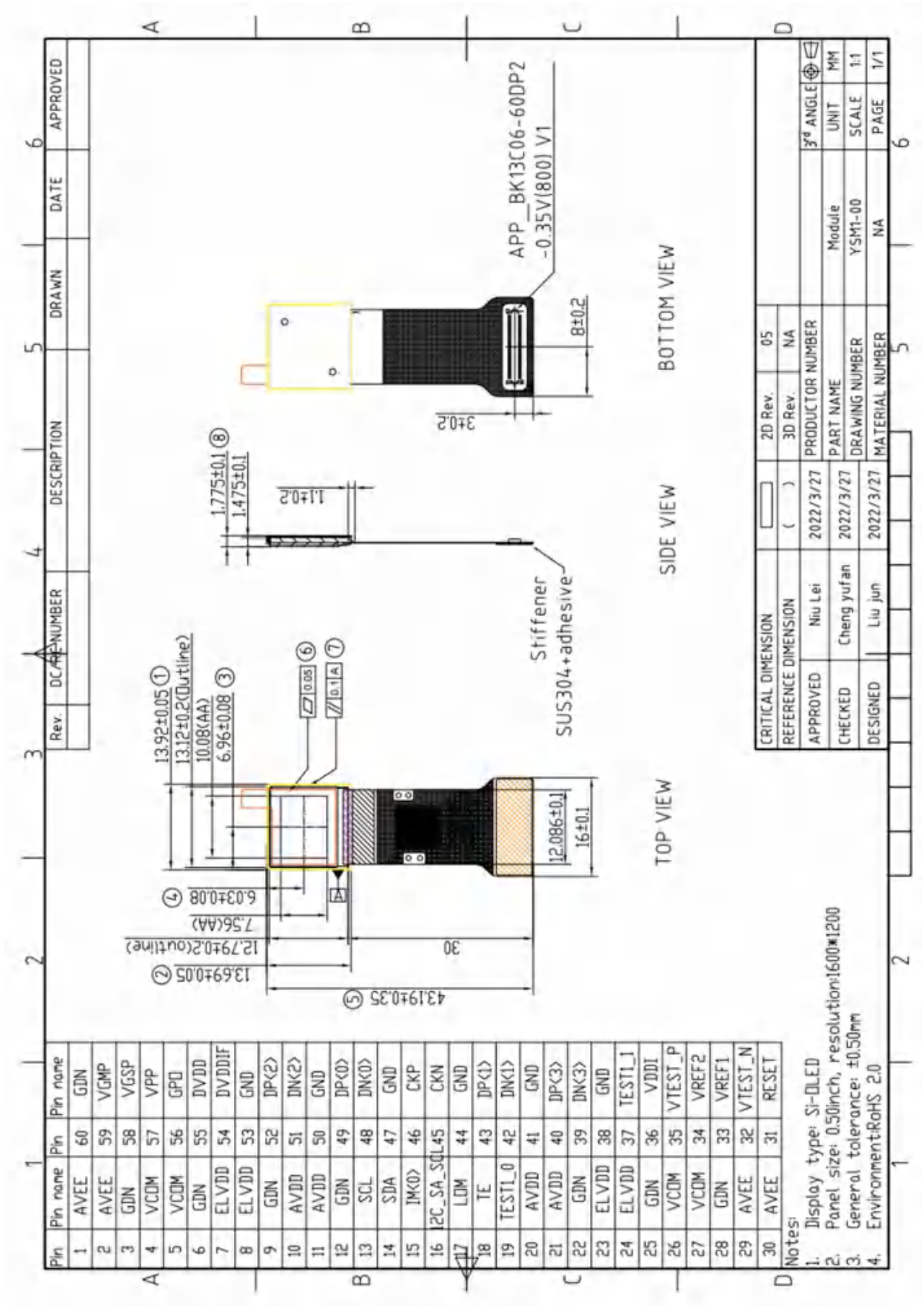
4. Pixel Array



5. System Block



6. Module Diagram



Pin	Pin name	Pin	Pin name
1	AVEE	60	GDN
2	AVEE	59	VGMP
3	GDN	58	VGSP
4	VCOM	57	VPP
5	VCOM	56	GPO
6	GDN	55	DVDD
7	ELVDD	54	DVDDIF
8	ELVDD	53	GND
9	GDN	52	DP<2>
10	AVDD	51	DN<2>
11	AVDD	50	GND
12	GDN	49	DP<0>
13	SCL	48	DN<0>
14	SDA	47	GND
15	IM<0>	46	CKP
16	I2C_SA_SCL	45	CKN
17	LOM	44	GND
18	TE	43	DP<1>
19	TEST1_0	42	DN<1>
20	AVDD	41	GND
21	AVDD	40	DP<3>
22	GDN	39	DN<3>
23	ELVDD	38	GND
24	ELVDD	37	TEST1_1
25	GDN	36	VDDI
26	VCOM	35	VTEST_P
27	VCOM	34	VREF2
28	GDN	33	VREF1
29	AVEE	32	VTEST_N
30	AVEE	31	RESET

7. Pin Description

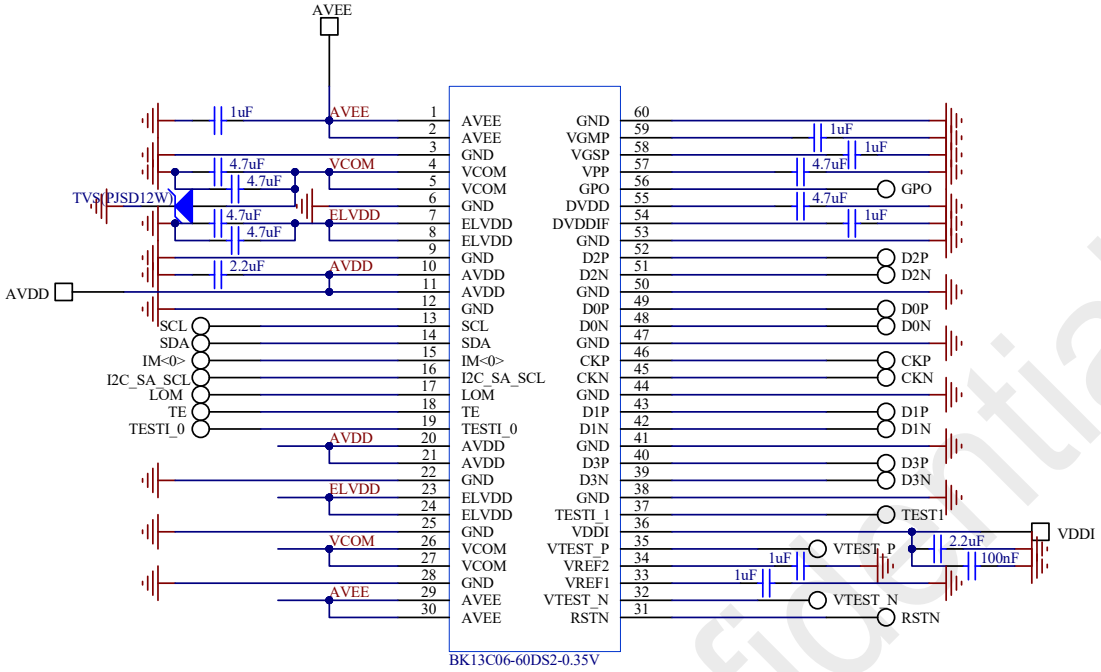
7.1 Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>AVEE</td><td>Power</td><td>Power supply for OLED cell.
It must be connected a stabilizing capacitor 2.2μF to GND.</td></tr>
<tr><td>2</td><td>AVEE</td><td>Power</td><td>Power supply for OLED cell.
It must be connected a stabilizing capacitor 2.2μF to GND.</td></tr>
<tr><td>3</td><td>GND</td><td>Power</td><td>System GND for internal digital/analog system.</td></tr>
<tr><td>4</td><td>VCOM</td><td>Output</td><td>LDO output for Panel common voltage.
It must be connected a stabilizing capacitor 4.7μF and a TVS to GND</td></tr>
<tr><td>5</td><td>VCOM</td><td>Output</td><td>LDO output for Panel common voltage.
It must be connected a stabilizing capacitor 4.7μF and a TVS to GND</td></tr>
<tr><td>6</td><td>GND</td><td>Power</td><td>System GND for internal digital/analog system.</td></tr>
<tr><td>7</td><td>ELVDD</td><td>Power</td><td>LDO output for Panel positive voltage.
It must be connected a stabilizing capacitor 4.7μF to GND</td></tr>
<tr><td>8</td><td>ELVDD</td><td>Power</td><td>LDO output for Panel positive voltage.
It must be connected a stabilizing capacitor 4.7μF to GND</td></tr>
<tr><td>9</td><td>GND</td><td>Power</td><td>System GND for internal digital/analog system.</td></tr>
<tr><td>10</td><td>AVDD</td><td>Power</td><td>Positive power supply for analog circuit.</td></tr>
<tr><td>11</td><td>AVDD</td><td>Power</td><td>Positive power supply for analog circuit.</td></tr>
<tr><td>12</td><td>GND</td><td>Power</td><td>System GND for internal digital/analog system.</td></tr>
<tr><td>13</td><td>SCL</td><td>Input/ Output</td><td>I2C clock pin, when not in use, please fix to VDDI.</td></tr>
<tr><td>14</td><td>SDA</td><td>Input/ Output</td><td>I2C data output, when not in use, please fix to VDDI.</td></tr>
<tr><td>15</td><td>IM<0></td><td>Input</td><td>Use to select the interface type
<table>
<tr><td>IM<0></td><td>Command</td><td>Display Data</td></tr>
<tr><td>0</td><td>MIPI</td><td>MIPI</td></tr>
<tr><td>1</td><td>I2C</td><td>MIPI</td></tr>
</table></td></tr>
<tr><td>16</td><td>I2C_SA _SCL</td><td>Input</td><td>This signal will decide bit 0 of the I2C slave address. When not in use, keep it low.
<table>
<tr><td>I2C_SA_SEL</td><td>Slave Address bit 0</td></tr>
<tr><td>GND</td><td>0</td></tr>
<tr><td>VDDI</td><td>1</td></tr>
</table></td></tr>
<tr><td>17</td><td>LOM</td><td>Output</td><td>Enable pin for Light-on-mode. When not in use, keep it open.</td></tr>
<tr><td>18</td><td>TE</td><td>Output</td><td>Output Pad for GPIO or checking signal, when not in use, keep it open.</td></tr>
<tr><td>19</td><td>TESTI_0</td><td>Output</td><td>Test mode for Internal logical function test, when not in use, keep it open.</td></tr>
<tr><td>20</td><td>AVDD</td><td>Power</td><td>Positive power supply for analog circuit.</td></tr>
<tr><td>21</td><td>AVDD</td><td>Power</td><td>Positive power supply for analog circuit.</td></tr>
<tr><td>22</td><td>GND</td><td>Power</td><td>System GND for internal digital/analog system.</td></tr>
<tr><td>23</td><td>ELVDD</td><td>Power</td><td>LDO output for Panel positive voltage.
It must be connected a stabilizing capacitor 4.7μF to GND</td></tr>
<tr><td>24</td><td>ELVDD</td><td>Power</td><td>LDO output for Panel positive voltage.
It must be connected a stabilizing capacitor 4.7μF to GND</td></tr>
<tr><td>25</td><td>GND</td><td>Power</td><td>System GND for internal digital/analog system.</td></tr>
<tr><td>26</td><td>VCOM</td><td>Output</td><td>LDO output for Panel common voltage.
It must be connected a stabilizing capacitor 4.7μF to GND.</td></tr>
<tr><td>27</td><td>VCOM</td><td>Output</td><td>LDO output for Panel common voltage.
It must be connected a stabilizing capacitor 4.7μF to GND.</td></tr>
<tr><td>28</td><td>GND</td><td>Power</td><td>System GND for internal digital/analog system.</td></tr>
<tr><td>29</td><td>AVEE</td><td>Power</td><td>-5.0V~-7.5V Power supply for OLED cell.
It must be connected a stabilizing capacitor 2.2μF to GND.</td></tr>
<tr><td>30</td><td>AVEE</td><td>Power</td><td>-5.0V~-7.5V Power supply for OLED cell.
It must be connected a stabilizing capacitor 2.2μF to GND.</td></tr>
<tr><td>31</td><td>RSTN</td><td>Input</td><td>This signal will reset the function and must be applied to properly initialize the display part. Signal is active low.</td></tr>
<tr><td>32</td><td>VTEST_N</td><td>Output</td><td>Test mode for checking signal, when not in use, keep it open.</td></tr>
<tr><td>33</td><td>VREF1</td><td>Output</td><td>Reference voltage output for internal circuit.
It must be connected a stabilizing capacitor 1.0μF to GND.</td></tr>
<tr><td>34</td><td>VREF2</td><td>Output</td><td>Reference voltage output for internal circuit.
It must be connected a stabilizing capacitor 1.0μF to GND.</td></tr>
</table>

35	VTEST_P	Output	Test mode for checking signal, when not in use, keep it open.
36	VDDI	Power	Power supply for logic power and I/O circuit. It must be connected a stabilizing capacitor 2.2μF to GND.
37	TEST1_1	Output	Test mode for Internal logical function test, when not in use, keep it open.
38	GND	Power	System GND for internal digital/analog system.
39	DN<3>	Input	MIPI-DSI Data differential signal input pins.
40	DP<3>	Input	MIPI-DSI Data differential signal input pins.
41	GND	Power	System GND for internal digital/analog system.
42	DN<1>	Input	MIPI-DSI Data differential signal input pins.
43	DP<1>	Input	MIPI-DSI Data differential signal input pins.
44	GND	Power	System GND for internal digital/analog system.
45	CKN	Input	MIPI-DSI Clock differential signal input pins.
46	CKP	Input	MIPI-DSI Clock differential signal input pins.
47	GND	Power	System GND for internal digital/analog system.
48	DN<0>	Input/ Output	MIPI-DSI Data differential signal input / Output pins.
49	DP<0>	Input/ Output	MIPI-DSI Data differential signal input / Output pins.
50	GND	Power	System GND for internal digital/analog system.
51	DN<2>	Input	MIPI-DSI Data differential signal input pins.
52	DP<2>	Input	MIPI-DSI Data differential signal input pins.
53	GND	Output	System GND for internal digital/analog system.
54	DVDDIF	Output	LDO output for MIPI. It must be connected a stabilizing capacitor 1.0μF to GND.
55	DVDD	Output	LDO output for Digital circuit. It must be connected a stabilizing capacitor 4.7μF to VSSD.
56	GPO	Output	Output Pad for GPIO or checking signal, when not in use, keep it open.
57	VPP	Power	Power supply for OTP. It must be connected a stabilizing capacitor 4.7μF to GND.
58	VGSP	Output	LDO output for Positive Gamma low voltage. It must be connected a stabilizing capacitor 1.0μF to GND.
59	VGMP	Output	LDO output for Positive Gamma high voltage. It must be connected a stabilizing capacitor 1.0μF to GND.
60	GND	Power	System GND for internal digital/analog system.

7.2 Application circuit

Below circuit is one of typical example for reference to drive the module.



8. Electrical Characteristics

8.1 Absolute Maximum Ratings

The absolute maximum rating is listed on the below table. When this Micro-OLED product is used beyond the absolute maximum ratings, it may be permanently damaged. It is strongly recommended use this Micro-OLED product within the following specified limits for normal operation. If these electrical characteristic conditions are exceeded during normal operation, this Micro-OLED product will malfunction and cause poor reliability.

Item	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Supply voltage	VDDI	-0.3	-	+2.0	V
Supply voltage	AVDD	-0.3	-	+7.5	V
Supply voltage	AVEE	-7.5	-	0	V
Supply voltage	AVDD~AVEE	|AVDD-AVEE| ≤ 15			V
Operating temperature	Topr	-40	-	+85	℃
Storage temperature	Tstg	-50	-	+85	℃
Input voltage	V_{in}	-0.3	-	VDDI+0.3	V

8.2 DC Characteristic

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
Power & Operation Voltage							
Analog Operating voltage	DVDD	Operating Voltage	-	1.3	-	V	
Analog Operating voltage	AVDD	Operating Voltage	5.0	-	7.5	V	
Analog Operating voltage	AVEE	Operating Voltage	-7.5	-	-5.0	V	
Analog Operating voltage	ELVDD	Operating Voltage	3.0	-	6.5	V	1
Analog Operating voltage	VCOM	Operating Voltage	-6.5	-	-1.1	V	2
Analog Operating voltage	VGMP	Operating Voltage	4.0	-	6.5	V	
Analog Operating voltage	VGSP	Operating Voltage	0	-	2.0	V	

Analog Operating voltage	|AVDD-AVEE|	Operating Voltage	|AVDD-AVEE| ≤15			V	
Analog Operating voltage	|AVDD-VREF2|	Operating Voltage	|AVDD-VREF2| ≤8.5			V	
Analog Operating voltage	|AVEE-VREF2|	Operating Voltage	|AVEE-VREF2| ≥4			V	
Analog Operating voltage	|AVDD-VGMP|	Operating Voltage	|AVDD-VGMP| ≥1			V	3
I/O Operating voltage	VDDI	I/O Supply Voltage	1.65	1.8	1.95	V	
MIPI Operating Voltage	DVDDIF	DVDDIF Supply Voltage	-	1.3	-	V	
LOGIC INPUT/OUTPUT							
Logic High level input voltage	VIH	-	0.7x VDDI	-	VDDI	V	4
Logic Low level input voltage	VIL	-	GND	-	0.3x VDDI	V	4
Logic High level output voltage	VOH	IOH= -0.1mA	0.8x VDDI	-	VDDI	V	5
Logic Low level output voltage	VOL	IOL= +0.1mA	GND	-	0.2x VDDI	V	5
Logic High level leakage	ILIH1	Vin=0 to VDDI	-	-	1	μA	4,5
Logic Low level leakage	ILIL1	Vin=0 to VDDI	-1	-	-	μA	4,5
Source OP Output							
Output deviation voltage	V_{dev}	Sout≥AVDD-1.2V Sout≤1.2V			±30	mV	
Output deviation voltage	V_{dev}	AVDD-1.2V>Sout>1.2V			±15	mV	
Output deviation voltage	V_{OFSET}				±40	mV	
Stand-by Current							
DDI Sleep In mode	I_{stlp1}	DSI LP mode VDDI Current		1000		μA	4
		DSI LP mode AVDD Current		200		μA	
		DSI LP mode AVEE Current		80		μA	

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
DDI Sleep In mode	I_{stul1}	DSI Ultra Low power VDDI Current		950		μA	4
		DSI Ultra Low power AVDD Current		100		μA	
		DSI Ultra Low power AVEE Current		50		μA	
Oscillator Output							
Oscillator tolerance	ΔOSC	Ta=25℃	-5%	-	5%	%	6

Note1: *The maximum output of ELVDD would be lower than AVDDP - 1.0V.*

Note2: *The maximum output of \|VCOM\| would be lower than \|AVEEP\| - 1.0V.*

Note3: *The maximum output of VGMP would be lower than AVDDP - 1.0V when heavy loading.*

Note4: *Including of RESET*

Note5: *Including of GPO and TE.*

Note6: *Oscillator = 70MHz.*

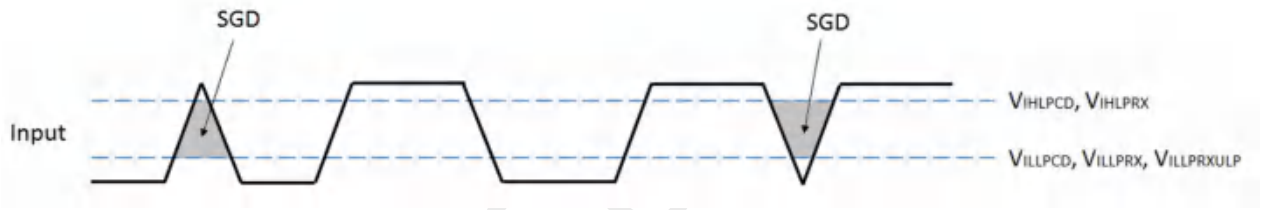
8.3 DSI DC/AC Characteristic

8.3.1 DC/AC Characteristics for DSI LP Mode

Condition: Ta=25℃, VDDI=1.65V~1.95V, AVDD=5.0V~7.5V, AVEE=-5.0V~-7.5V.

Parameter	Symbol	Conditions	Specification			Unit	Notes
			Min	Typ.	Max		
Logic high level input voltage	V_{IHLPCD}	LP-CD	450		1350	mV	
Logic Low level input voltage	V_{ILLPCD}	LP-CD	0		200	mV	
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK,D0)	880		1350	mV	
Logic Low level input voltage	V_{ILLPCD}	LP-RX(CLK,D0)	0		550	mV	
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0		300	mV	
Logic high level input voltage	V_{OHLPTX}	LP-TX(D0)	1.1		1.3	V	
Logic Low level input voltage	V_{OLLPTX}	LP-TX(D0)	-50		50	mV	
Logic high level input current	I_{IH}	LP-RX, Vin=0~1.3V			10	μA	
Logic Low level input current	I_{IL}	LP-RX, Vin=0~1.3V	-10			μA	
Input pulse rejection	SGD	DSI-CLKP/N, DSI-DnP/N			300	Vps	1

Note1: *Peak interference amplitude max. 200mV and interference frequency min. 450MHz.*



8.3.2 DC/AC Characteristics for DSI HS Mode

Condition: Ta=25℃, VDDI=1.65V~1.95V, AVDD=5.0V~7.5V, AVEE=-5.0V~-7.5V.

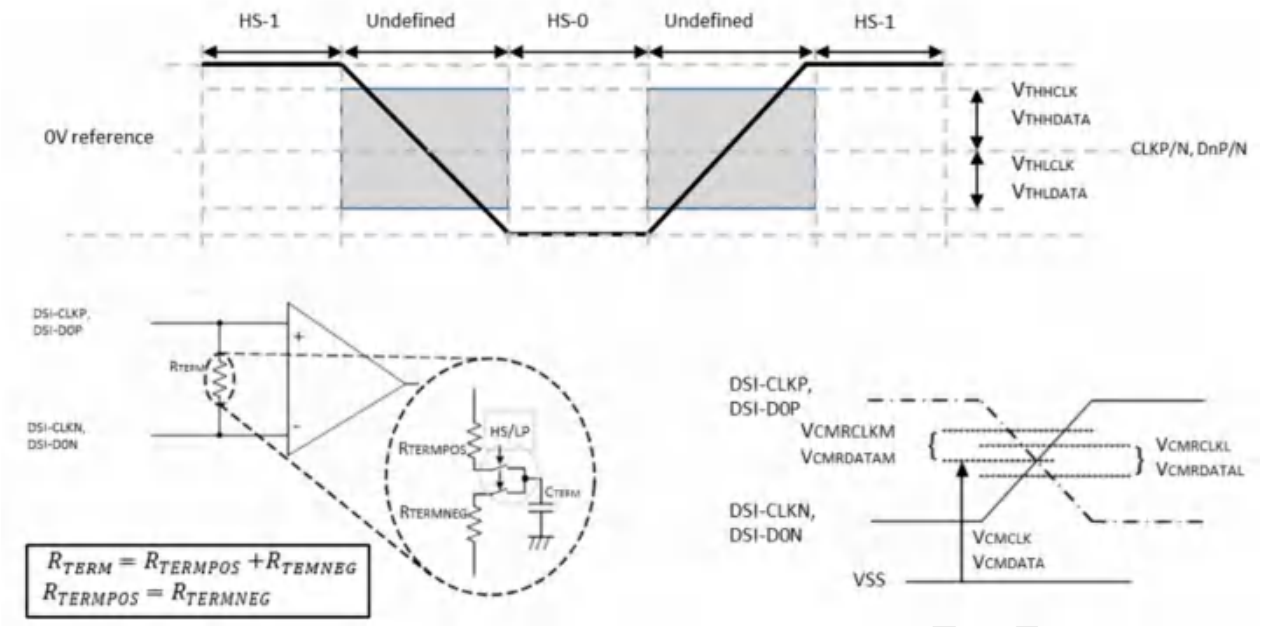
Parameter	Symbol	Conditions	Specification			Unit	Notes
			Min	Typ.	Max		
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	CLKP/N, DnP/N	70		330	mV	1, 2
Differential input low threshold	V_{THLCLK} $V_{THLDATA}$	CLKP/N, DnP/N	-70			mV	
Differential input high threshold	V_{TLLCLK} $V_{TLLDATA}$	CLKP/N, DnP/N			70	mV	
Single-ended input low voltage	V_{ILHS}	CLKP/N, DnP/N	-40			mV	2
Single-ended input high voltage	V_{IHHS}	CLKP/N, DnP/N			460	mV	2
Differential input termination resistor	R_{TERM}	CLKP/N, DnP/N	80	100	125	Ω	
Single-ended threshold voltage for termination enable	V_{TERM_EN}	CLKP/N, DnP/N			450	mV	
Input voltage common mode interference (≦450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	CLKP/N, DnP/N	-50		50	mV	3
Input voltage common mode interference (≧450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	CLKP/N, DnP/N			100	mV	
Common-mode termination capacitance	C_{TERM}	CLKP/N, DnP/N	14		60	pF	

Note1: *Includes 50mV (-50mV to 50mV) ground difference.*

Note2: *Without V CMRCLKM / V CMRDATAM .*

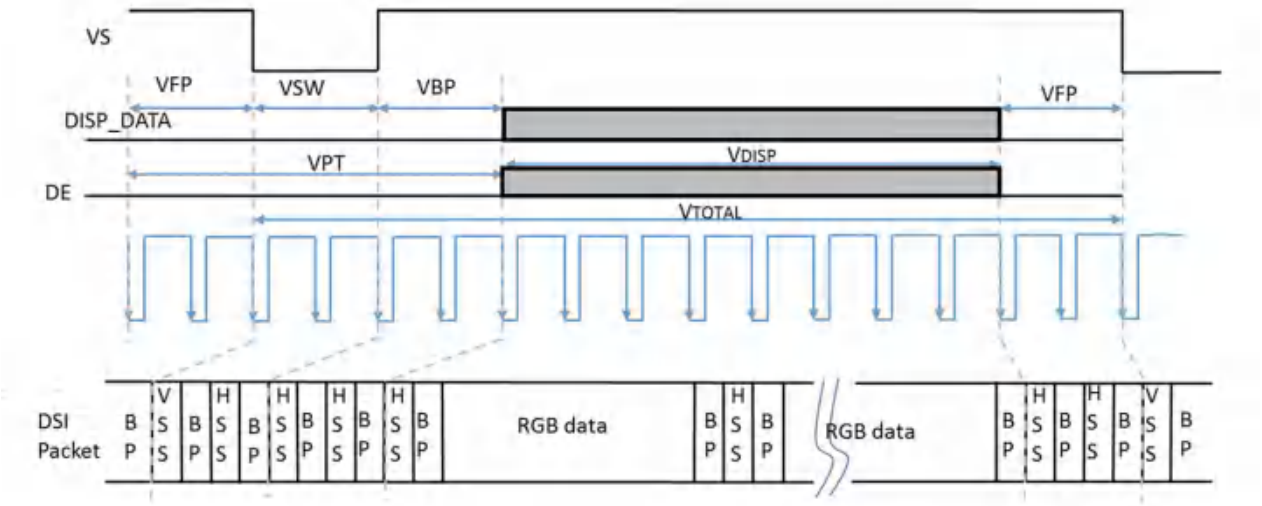
Note3: *Without 50mV (-50mV to 50mV) ground difference.*

Note4: *Dn =D0,D1,D2 and D3.*



8.4 AC Timing Characteristics

8.4.1 Vertical Timings for DSI video mode



Condition: Ta=25℃, VDDI=1.65V~1.95V, AVDD=5.0V~7.5V, AVEE=-5.0V~-7.5V.
Resolution = 1600(RGB) x 1200 @ 800Mbps

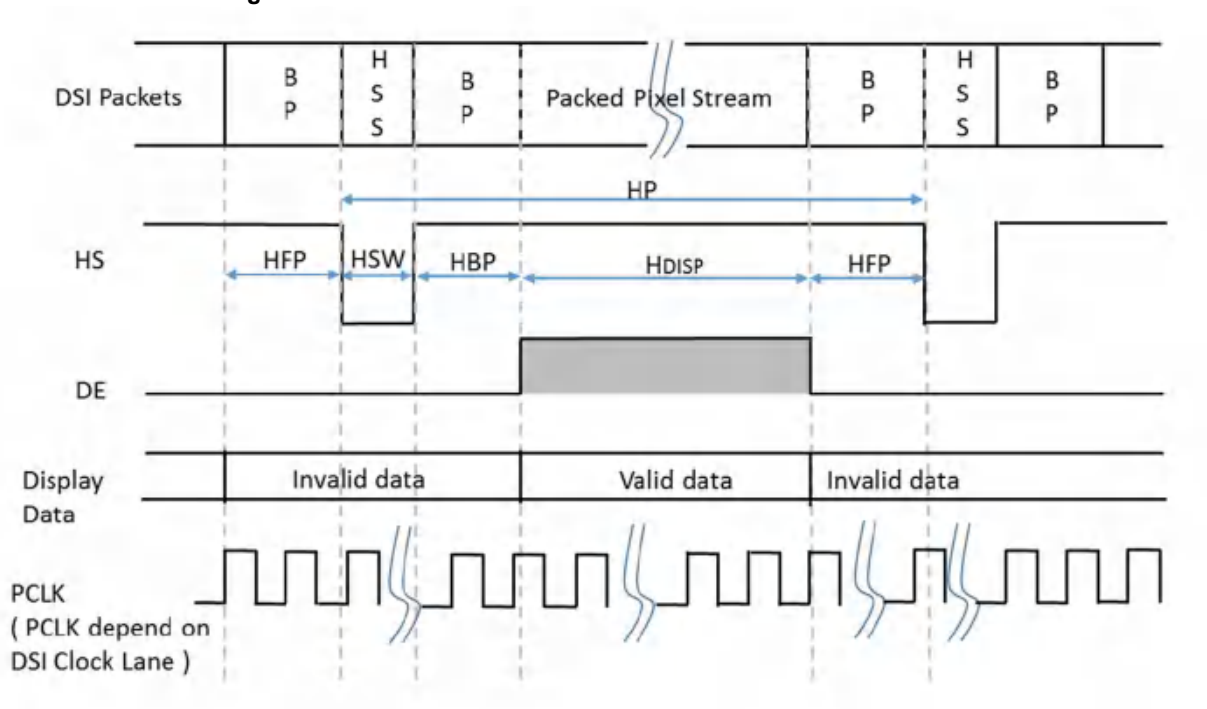
Parameter	Symbol	Conditions	Specification			Unit	Notes
			Min	Typ.	Max		
Vertical Total	V_{TOTAL}		-		2047	Line	
Vertical low pulse width	VSW		2	2		Line	1,2
Vertical front porch	VFP		30	36		Line	1
Vertical back porch	VBP		30	34		Line	1
Vertical data start point		VSW+VBP	32	36		Line	
Vertical blanking period	VPT	VSW+VBP+VFP	62	72		Line	
Vertical active area	V DISP		-		1200	Line	
Vertical Frame rate	VFR			60	120	Hz	3

Note1: *The VBP+VSW and VFP must be divisible by four for pixel shift function enable.*

Note2: *The Minimum VSW should be greater than or equal to 2.*

Note3: *The Maximum vertical frame rate should depend on MIPI bandwidth.*

8.4.2 Horizontal Timings for DSI video mode



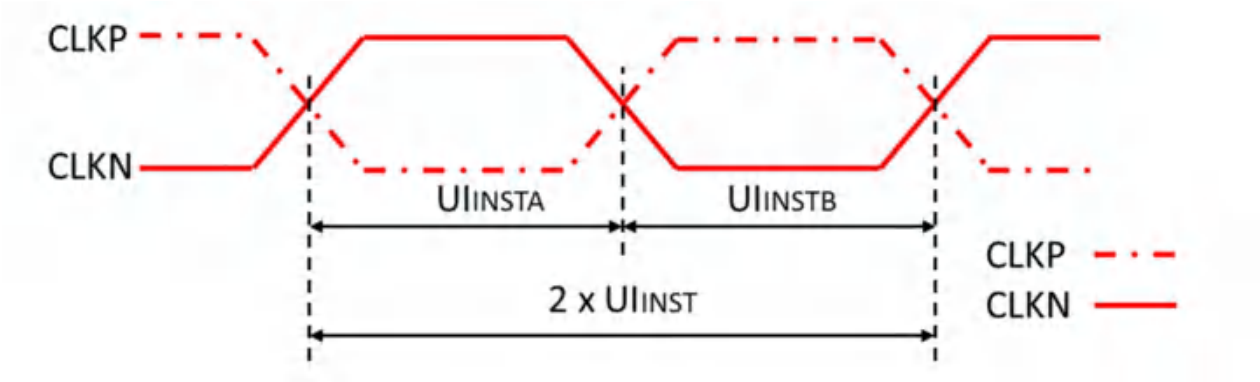
Condition: Ta=25℃, VDDI=1.65V~1.95V, AVDD=5.0V~7.5V, AVEE=-5.0V~-7.5V.
Resolution = 1600(RGB) x 1200 @ 800Mbps

Parameter	Symbol	Conditions	Specification			Unit	Notes
			Min	Typ.	Max		
HS low pulse width	HSW		30			nS	
Horizontal back porch	HBP		150			nS	
Horizontal front porch	HFP		150			nS	
Horizontal data start point		HSW+HBP	230			nS	
Horizontal blanking period	HBLK	HSW+HBP+HFP	350			nS	
Horizontal active area	H_{DISP}		-	1600	1600	DCLK	

Parameter	Symbol	Conditions	Specification			Unit	Notes
			Min	Typ.	Max		
HS low pulse width	HSW		6	6		Pixel	
Horizontal back porch	HBP		20	32		Pixel	
Horizontal front porch	HFP		20	32		Pixel	
Horizontal data start point		HSW+HBP	26	38		Pixel	
Horizontal blanking period	HBLK	HSW+HBP+HFP	46	70		Pixel	
Horizontal active area	H_{DISP}		-	1600	1600	DCLK	

8.5 MIPI AC Characteristics

8.5.1 High Speed Mode – Clock Timings



Signal	Symbol	Parameter	Specification			Unit	Notes
			Min	Typ.	Max		
CLK P/N	$2xUI_{INST}$	Double UI instantaneous	4		25	nS	
CLK P/N	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	1	1.334	12.5	nS	3,4,5

Note1: *UI = UI_{INSTA} = UI_{INSTB}*

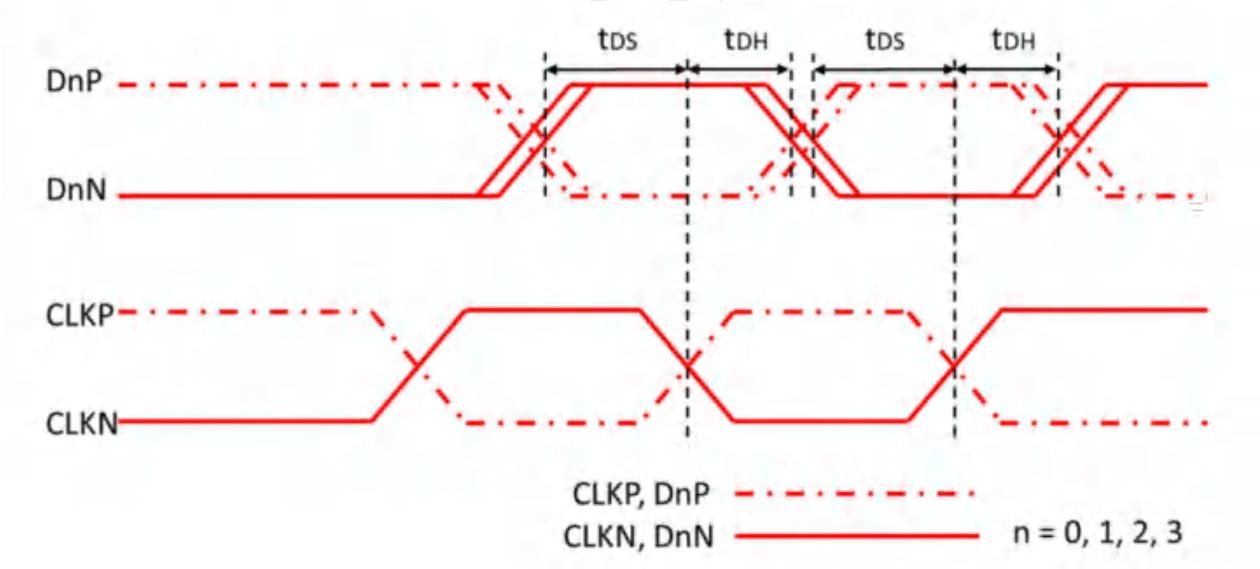
Note2: *Total bandwidth is 2.25Gbps with VESA DSC function active.*

Note3: *This display can support maximum 563Mbps per lane at 4 lane application with VESA DSC function active.*

Note4: *This display can support maximum 750Mbps per lane at 3 lane application with VESA DSC function active.*

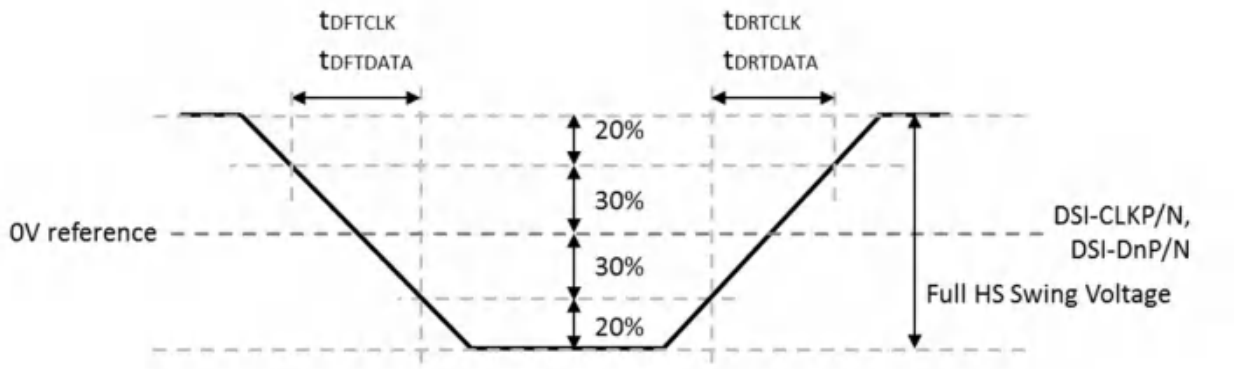
Note5: *This display can support maximum 1000Mbps per lane at 4 lane application without VESA DSC function active.*

8.5.2 High Speed Mode – Clock / Data Timings



Signal	Symbol	Parameter	Specification			Unit	Notes
			Min	Typ.	Max		
Dn P/N (n=0,1,2 and 3)	t_{DS}	Data to Clock Setup time	0.15*UI			UI	
	t_{DH}	Clock to Data Hold time	0.15*UI			UI	

8.5.3 High Speed Mode – Rising and Falling Timings



Parameter	Symbol	Conditions	Specification			Unit	Notes
			Min	Typ.	Max		
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		0.3*UI		1,2,3

Note1: *DnP/N, n =0,1,2 and 3.*

Note2: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-PHY Standard*

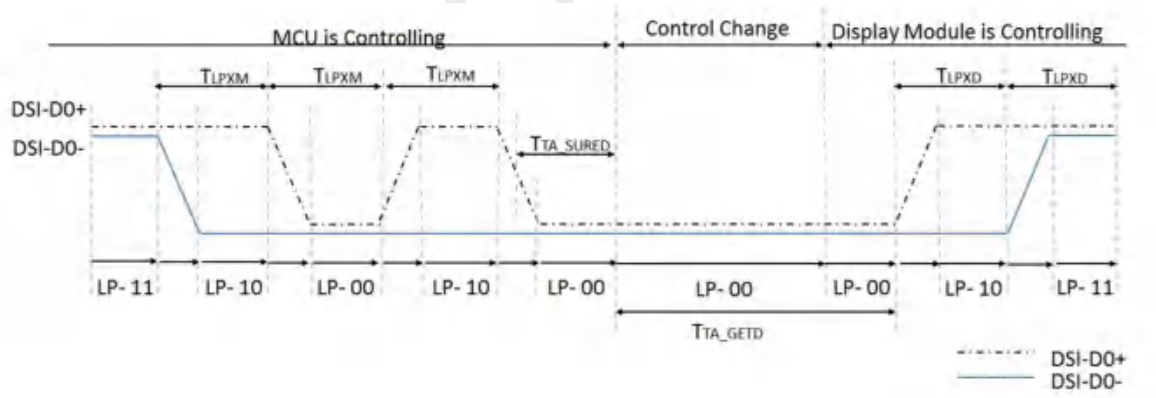
Note3: *DSI-CLK+ = CLKP.*

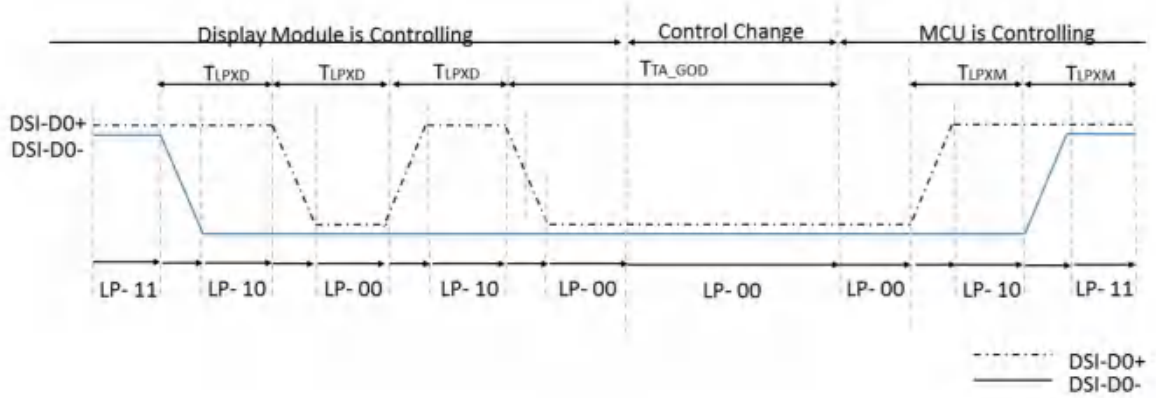
DSI-CLK- =CLKN.

DSI-D0+ =D0P.

DSI-D0- =D0N.

8.5.4 Low Speed Mode – Bus Turn Around

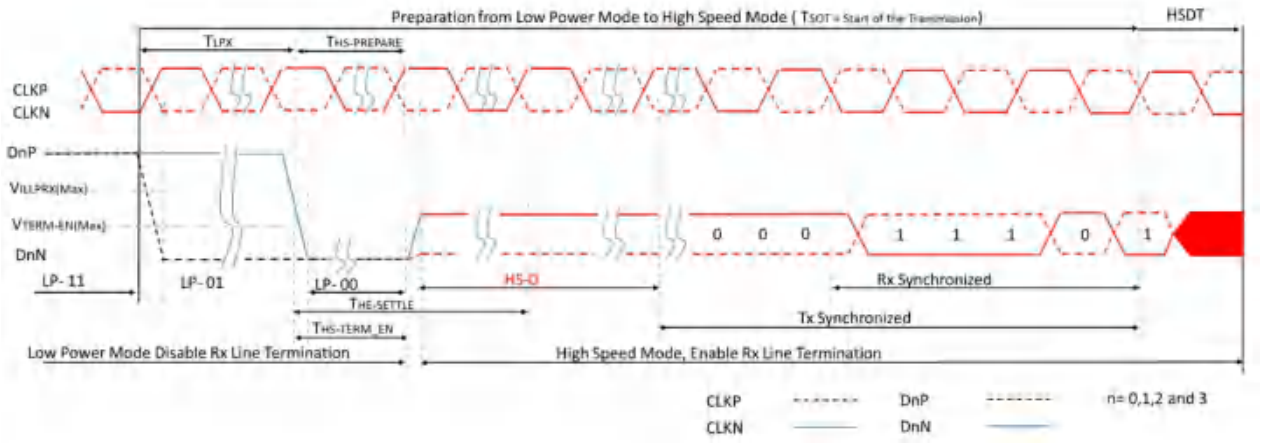




Signal	Symbol	Parameter	Specification			Unit	Notes
			Min	Typ.	Max		
D0P/N	T_{LPXM}	Length of LP-00, LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	T_{LPXD}	Length of LP-00, LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	
D0P/N	T_{TA_SURED}	Time-out before the Display Module starts driving	T_{LPXD}		$2*T_{LPXD}$	nS	
D0P/N	T_{TA_GETD}	Time to drive LP-00 by Display Module	$5*T_{LPXD}$			nS	
D0P/N	T_{TA_GOD}	Time to drive LP-00 after turnaround request –MCU	$4*T_{LPXD}$			nS	

Note1: *D0P = DSI-D0+, D0N = DSI-D0-.*

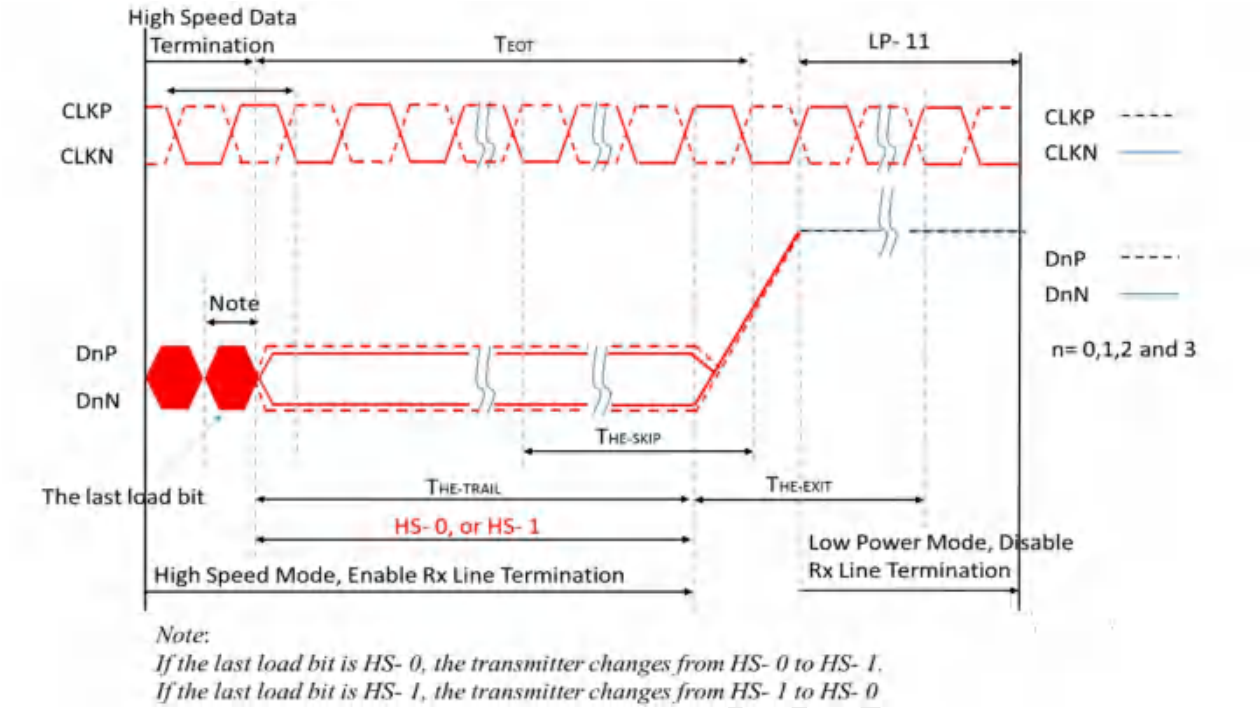
8.5.5 Data Lanes from Low Power Mode to High Speed Mode



Signal	Symbol	Parameter	Specification			Unit	Notes
			Min	Typ.	Max		
DnP/N	T_{LPX}	Length of any Low Power State Period	50			nS	1
DnP/N	Ratio T_{LPX}	Ratio of $T_{LPX(Master)}$ / $T_{LPX(Slave)}$ between Master and Slave side	2/3		3/2		
DnP/N	T HS-PREPARE	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	
DnP/N	T HS-PREPARE +T HS-ZERO	$T_{HS-PREPARE}$ +time that the transmitter drives the HS-0 state before the synce sequence	145+10* UI			nS	
DnP/N	T HS-TREM-EN	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	

Note1: *DnP/N, n=0,1,2 and 3.*

8.5.6 Data Lanes from High Speed Mode to Low Power Mode

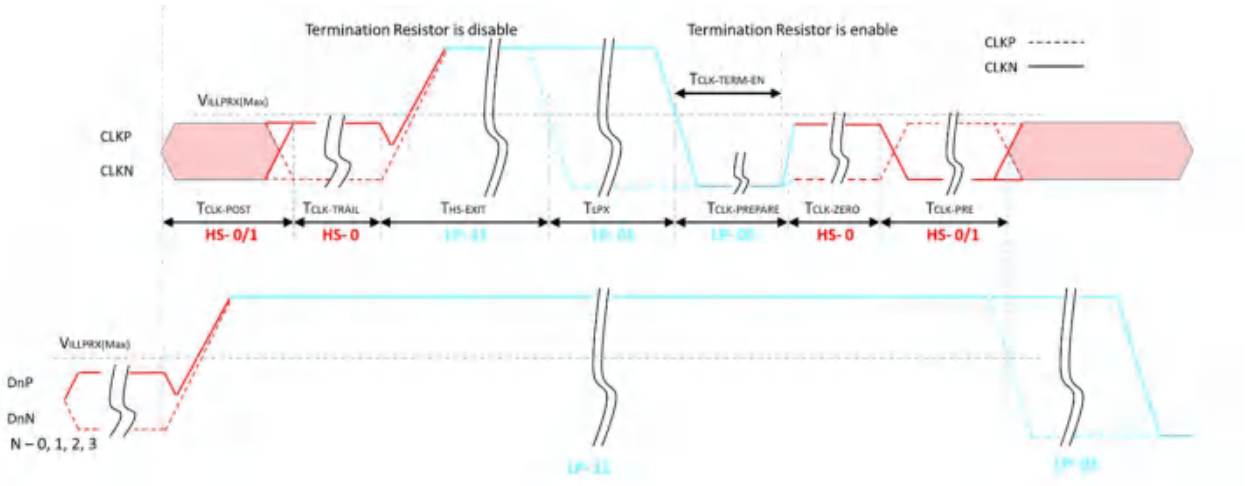


Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Signal	Symbol	Parameter	Specification			Unit	Notes
			Min	Typ.	Max		
DnP/N	$T_{HS-SKIP}$	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	

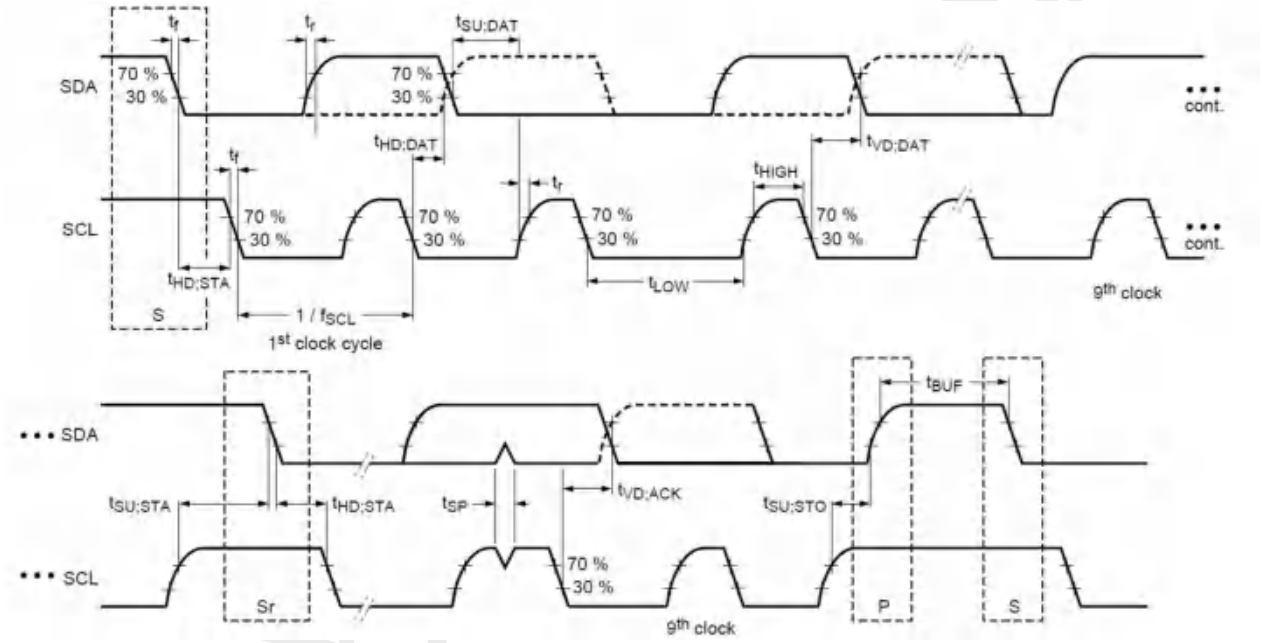
Note1: *DnP/N, n=0,1,2 and 3.*

8.5.7 DSI Clock Burst – High speed mode to /from Low Power Mode



Signal	Symbol	Parameter	Specification			Unit	Notes
			Min	Typ.	Max		
CLK P/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52 *UI			nS	
CLK P/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CLK P/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	
CLK P/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CLK P/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination			38	nS	
CLK P/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300			nS	
CLK P/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			UI	

8.6 I2C AC Characteristics



Characteristics of the SDA and SCL I/O stages for I2C-bus

Symbol	Parameter	Description	Specification		Unit	Notes
			Min	Max		
V_{IL}	Low-level input voltage		-0.5	0.3 x VDDI	V	
V_{IH}	High-level input voltage		0.7 x VDDI	VDDI	V	
V_{OL1}	Low-level output voltage 1	at 3 mA sink current; VDDI > 2 V	0	0.4	V	
V_{OL2}	Low-level output voltage 2	at 2 mA sink current; VDDI ⩽ 2 V	0	0.2 x VDDI	V	
I_{OL}	Low-level output current	VOL = 0.4 V	3	-	mA	
t_{of}	output fall time from V_{Ihmin} to V_{Ilmax}		-	250	ns	
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	50	ns	
C_i	capacitance for each I/O pin		-	10	pF	

Characteristics of the SDA and SCL bus lines for I2C-bus

Symbol	Parameter	Description	Specification		Unit	Notes
			Min	Max		
f_{SCL}	SCL clock frequency		0	400	kHz	
$t_{HD;STA}$	hold time for (repeated) START condition	After this period, the first clock pulse is generated.	0.6	-	μs	
t_{LOW}	LOW period of the SCL clock		1.3	-	μs	
t_{HIGH}	HIGH period of the SCL clock		0.6	-	μs	
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	μs	
$t_{HD;DAT}$	data hold time		0	-	μs	2,3
$t_{SU;DAT}$	data set-up time		100	-	ns	4
t_r	rise time of both SDA and SCL signals		20	300	ns	
t_f	fall time of both SDA and SCL signals		20	300	ns	1,2
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	μs	
t_{BUF}	bus free time between a STOP and START condition		1.3	-	μs	
$t_{VD;DAT}$	data valid time		-	0.9	μs	3,4
$t_{VD;ACK}$	data valid acknowledge time		-	0.9	μs	3,5

Note1: *The maximum t_f for the I2C_SDA and I2C_SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage tf is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.*

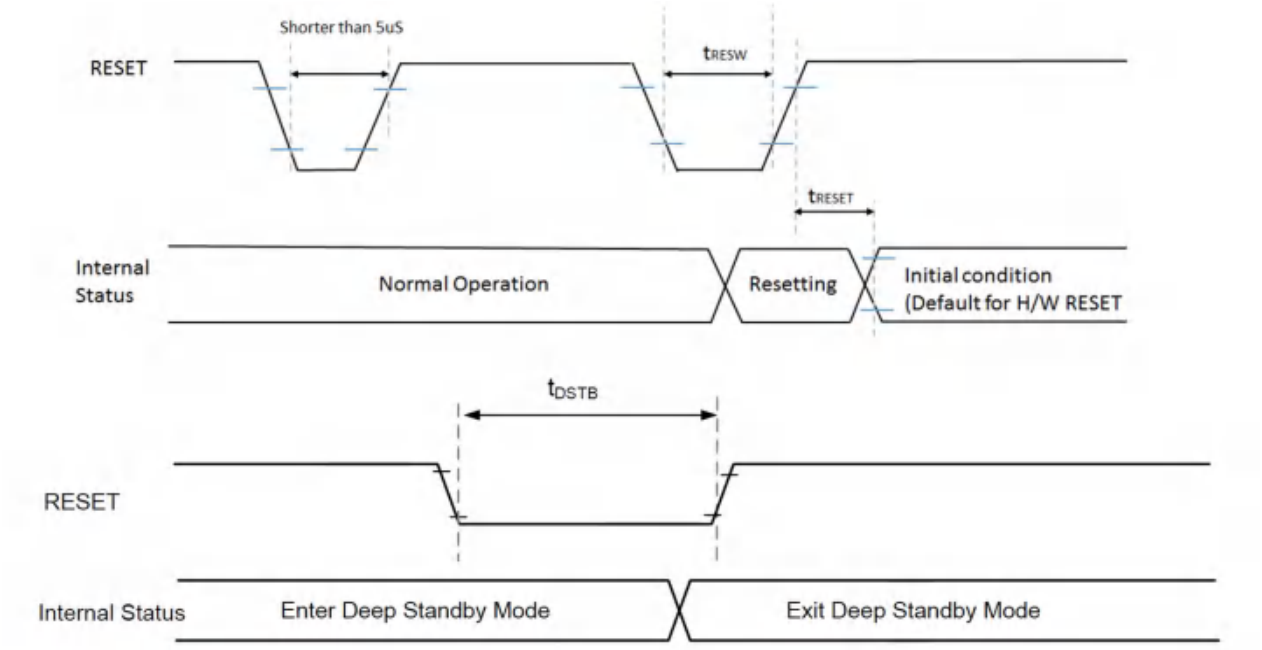
Note2: *A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.*

Note3: *The maximum $t_{HD;DAT}$ could be 3.45 μs and 0.9 μs, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.*

Note4: *$t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).*

Note5: *$t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).*

8.7 Reset Input Timing



Reset input timing

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				Min	Typ.	Max		
RESET	t_{RESW}	Reset "L" pulse width		10			μS	1
	t_{RESET}	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	2
	t_{DSTB}	Reset "L" pulse width	When exit DSTB mode	10			mS	

Note1: *Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.*

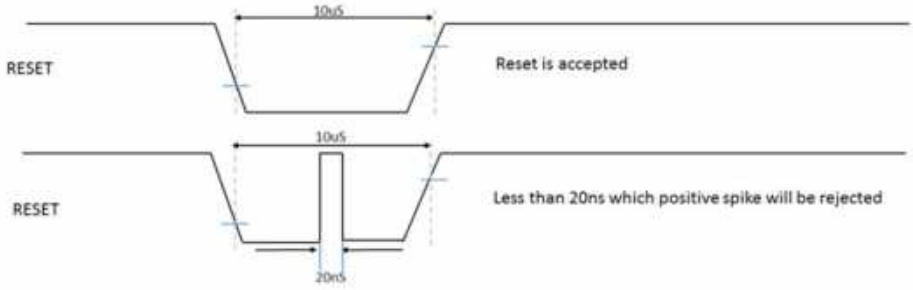
Note2: *During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.*

Reset input actions

RESET Pulse	Action
Short than 5us	Reset Rejected
Long than 10μS	Reset
Between 5us and 10μS	Reset Start

Note3: *During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (tRESET) within 5ms after a rising edge of RESET.*

Note4: *Spike Rejection also applies during a valid reset pulse as shown below.*



Note5: *It is necessary to wait 5ms after releasing RESET before sending any commands.*

9. Power Sequence

9.1 Power on sequence

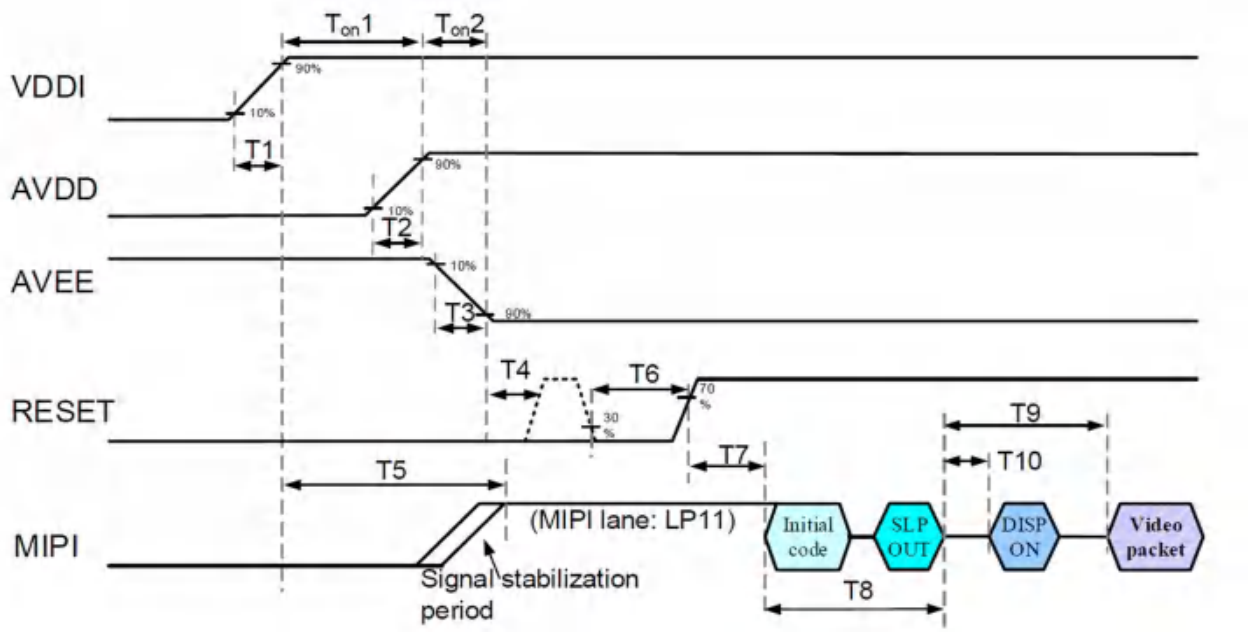
Power on sequence timing

Symbol	Description	Specification			Unit	Notes
		Min	Typ.	Max		
$T_{on}1$	VDDI on to AVDD on delay.	>0.1			ms	1
$T_{on}2$	AVDD on to AVEE on delay.	>0			μs	
T1	VDDI power rising time.	0.1		2	ms	
T2	AVDD power rising time.	0.2			ms	
T3	AVEE power falling time.	0.2			ms	
T4	AVEE valid to RESET high.	10			ms	
T5	DVDDIF to MIPI bus ready delay.	0		Note	ms	
T6	RESET low period.	10			μs	
T7	RESET high to OTP load ready.	30			ms	
T8	User initial code ready.	20			ms	
T9	Sleep-out command received to video packet transmit delay.	90	120		ms	
T10	Sleep-out command received to display on command transmit delay.	>0			μs	

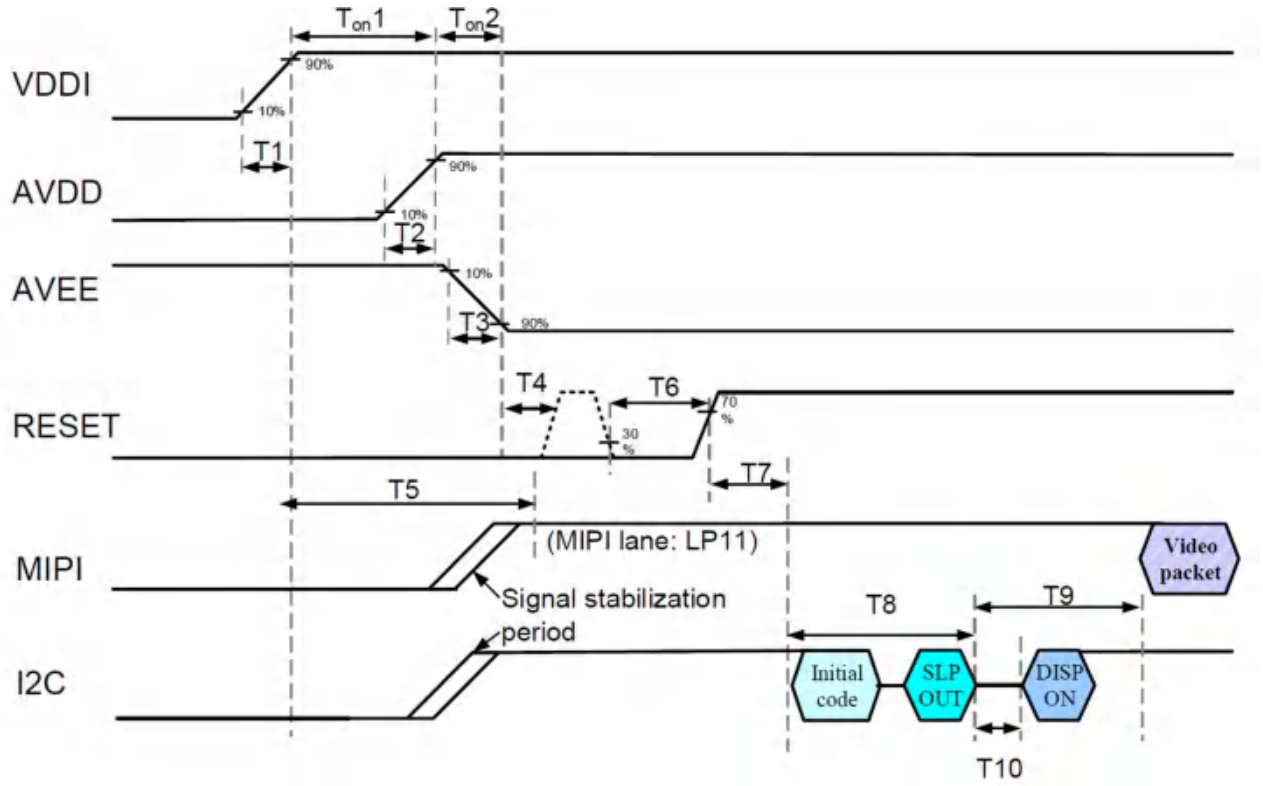
Note1: *T5 max time= Ton1+Ton2+T4.*

Note2: *Set T9 as 120 ms is the recommended time. If 90 ms is required, it has to work on particular register setting.*

Power on sequence (IM=0)



Power on sequence (IM=1)



Note1: *Unless particularly specified, timings herein show cross point at 50% of signal/power level.*

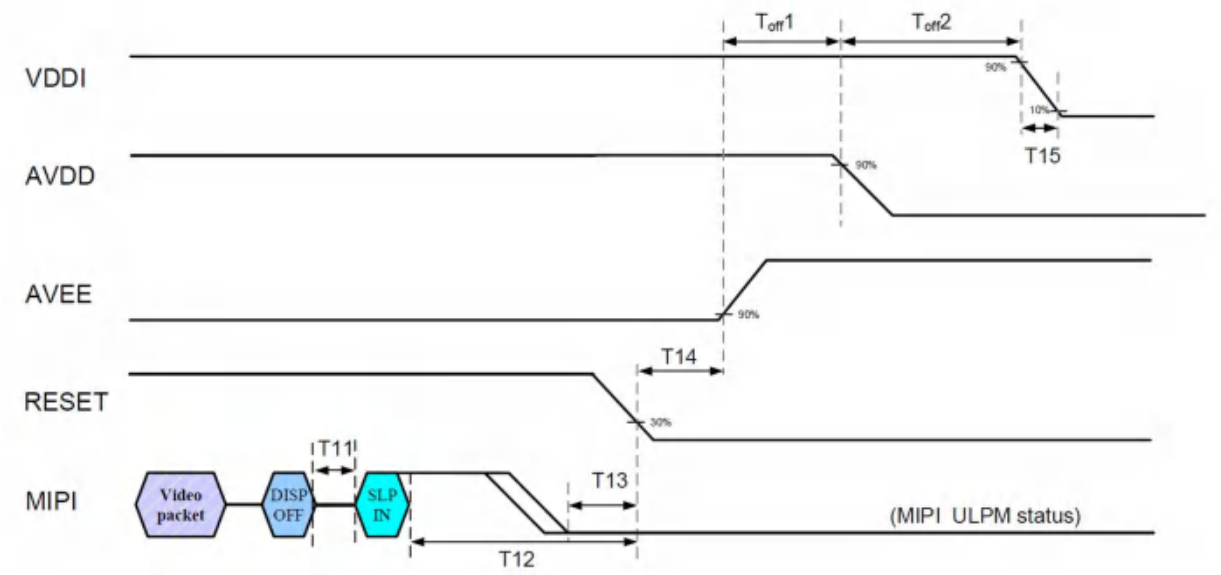
Note2: *These power-on sequence are based on adding Schottky diode on VCOM pin to ground.*

9.2 Power off sequence

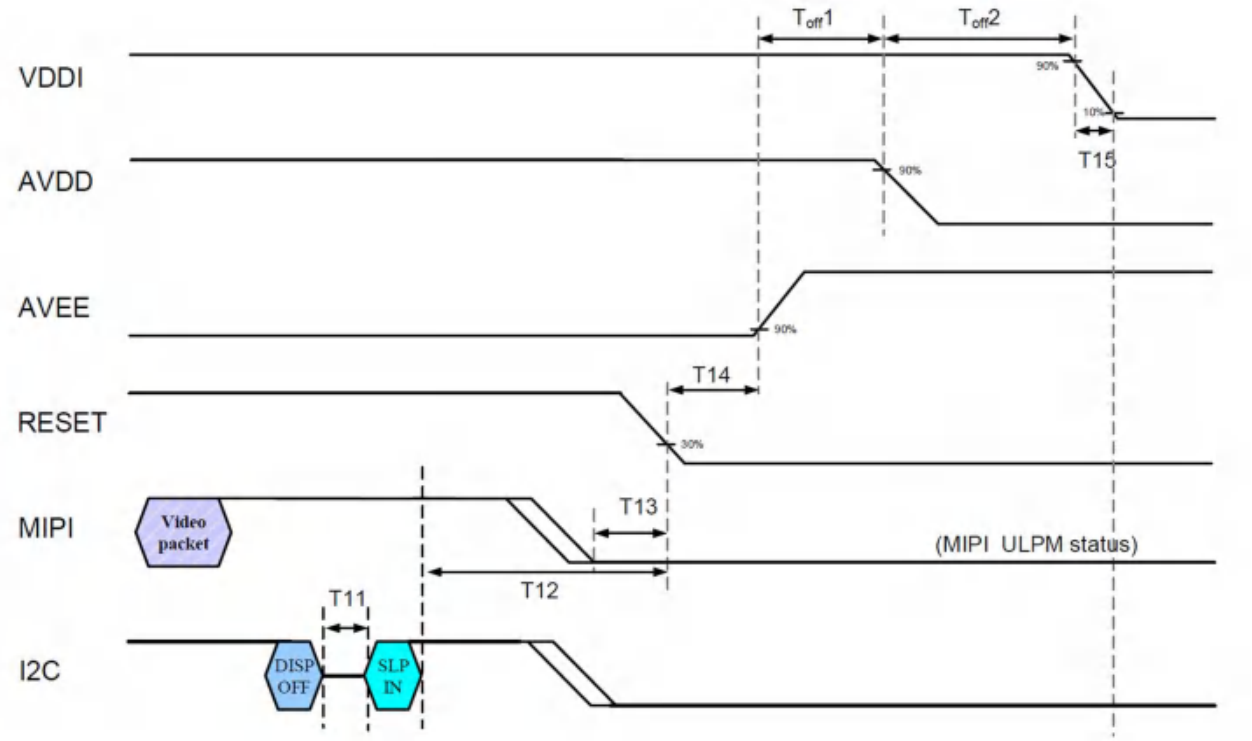
Power OFF sequence timing

Symbol	Description	Specification			Unit	Notes
		Min	Typ.	Max		
$T_{off}1$	AVEE off to AVDD off delay.	>0			μs	1
$T_{off}2$	AVDD off to VDDI off delay.	>0			μs	
T11	Display-off command received to Sleep-in command delay.	>0			μs	
T12	Sleep-in command received to valid to RESET low.	100			ms	
T13	MIPI ultra low power mode to valid to RESET low.	>0			μs	
T14	RESET low to AVEE off delay.	>0			μs	
T15	VDDI power falling time.			2	ms	

Power off sequence (IM=0)



Power off sequence (IM=1)



Note1: *Unless particularly specified, timings herein show cross point at 50% of signal/power level.*

10. Interface

This Micro-OLED product supports MIPI interface and inter-integrated circuit interface (I2C).

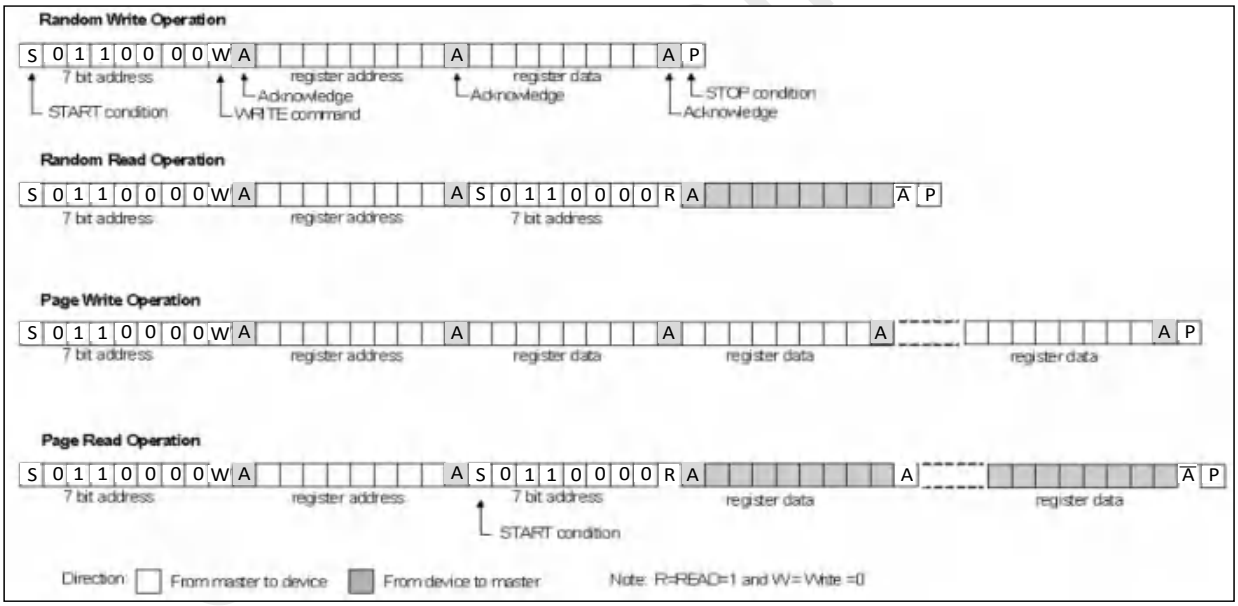
IM<0>	Command Execute	Image Write
0	MIPI	MIPI
1	I2C	MIPI

10.1 I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data Line (I2C_SDA) and Serial Clock Line (I2C_SCL). Both lines must be connected to a positive power supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte maybe sent. The master generates all clock pulses, including the ninth acknowledge clock pulse.

I2C-Bus Protocol

Before any data is transmitted on the I2C-bus, the device, which should respond is addressed first. The address of SY050 is 0x4C or 0x4D. The slave addressing is always carried out with the first byte transmitted after the START procedure.

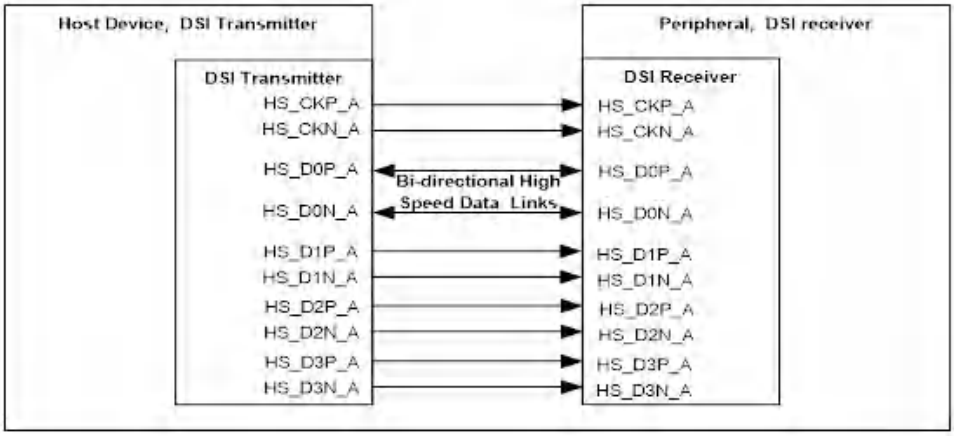


10.2 MIPI Interface

The Display Serial Interface (DSI) specifies the interface between a host processor and a peripheral. DSI builds on existing MIPI Alliance specifications by adopting pixel formats and command set specified in DPI-2, DBI-2 and DCS standards.

Figure shows a simplified DSI interface. DSI sends display data or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data,

commands, and events that, in traditional or legacy interfaces, are normally conveyed to and from the peripheral on a parallel data bus with additional control signals.



DSI transmitter and receiver interface

11. USER COMMAND

12. Reliability

No.	Item	Condition	Judgement Criterion
1	High Temperature Storage	80℃ 240hrs	After testing 1.No clearly visible defects or remarkable deterioration of display quality. 2.No function-related abnormalities *The results must be checked after 2hours later under room temperature
2	High Temperature Operating	70℃ 240hrs	
3	Low Temperature Storage	-40℃ 240hrs	
4	Low Temperature Operating	-30℃ 240hrs	
5	High Temperature / Humidity Storage	60℃/90%RH 240hrs	
6	High Temperature / Humidity Operating	60℃/90%RH 240hrs	
7	Thermal Shock	-30℃ ←→ 80℃, 0.5hr, Change time <1min, 100cycles	
8	ESD	Air discharge ±2kv Contact discharge ±1kv	After testing 1.Hard defect should not happen 2.If it would be recovered to normal state after resetting, it would be judged as a good state.

13. Handling Precautions

- Mounting Method

The MOLEDA panel of Panox Display module consists of one silicon backplane and one cover glass, which can easily get damaged. Since the module is constructed as to be fixed by utilizing fitting holes in the printed circuit board . Extreme care should be used when handling the MOLED.

- Caution of MOLED Handling and Cleaning

When cleaning the display surface, use soft solvent as recommended isopropyl alcohol and wipe gently, don't wipe the display surface with dry or hard materials that will damage the polarizer surface, don't use the following solvent, Water, Ketone, Aromatics

- Caution of Against Static Charge

For MOLED module, use C-MOS drivers, therefore we recommend that you, connect any unused input terminal to VCI or VSS, do not input and signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity. It could occur static electricity when taping off the film which protects MOLED. Against static charge, you should make sure that the product is safe or not by experiment in advance.

- Packing

The packing principle is that MOLED module should keep its packing condition at the time of delivery. For safety & avoiding the module damage, Carton box must stack the below 4 boxes.

When storing the MOLED after unpacking, note the followings. MOLED module is consisted of GLASS and assemblies. It should avoid pressure, strong impact, and being dropped from a height.

To prevent modules from degradation, do not operate or store them in a place where they are directly exposed to sunlight or high temperature/humidity.

- Caution for Operation

If you do not follow normal POWER ON, OFF sequence or abnormal operating, then MOLED module can be damaged electro-optically and does not recover. Do not change software without Panox Display confirmation.

Response time may extremely delay at a temperature lower than operating range, MOLED does not normally operate at a high temperature. But this may recover at a proper temperature.

When you set optimal operating voltage to MOLED module, you can see the optimal contrast of MOLED. So, add voltage controllable function at SET Module.

MOLED module may not display normally when twisting power or pressing power is added. Therefore, you should secure MOLED module maximum thickness at set assembly not to have any pressure affect MOLED module.

Electro-chemical reaction may occur when there is humidity on pad, therefore, you should use MOLED Module below maximum operating humidity.

MOLED Module Power VDD should be designed to protect surge current at SET Module. You should not damage connector and cable for MOLED module assembly by force folding or by applying extreme power.

MOLED may not display normally when it is interfered by surrounding elements, therefore you should consider setting design not to damage MOLED module by surrounding elements.

To satisfy EMI standards, you should plan your design after considering emitting energy. We can't guarantee display characteristics outside viewing area, therefore your set window should be fixed into viewing area. Image-sticking may occur if MOLED displays same image for a long time, so you need to make a change for MOLED.

- Storage

Place in a dark place where neither exposure to direct sunlight or any fluorescent light is permitted and keep at room temperature & room humidity. Store with no contact with polarizer surface. It is recommended to store them as they have been contained in the inner container when we delivered them.

- Safety Precautions

Disassembly or modification may cause electric shock, damages to sensitive part inside of the AMOLED module, dust adhesion, or scratches on the display part. In the event that the contents of AMOLED module are on skin, wipe them with a paper towel or gauge and wash the part well, and receive medical attention if necessary. Do not use the AMOLED module for the special purpose besides display units. Be careful of the glass chips that may cause injury to fingers of skin, when the display part is broken. For keeping safe quality from outer exposure or contamination, modules should be consumed within 2 months after unpacking.

- Precautions before use

- in case of any questions about contents of this "Specification for Approval".
- in case of occurring new problems not mentioned at this "Specification for Approval".
- in case of your request about income inspection specification change.
- in case of occurring new problem at your driving test.

14. Packing

TBD