Product Specification

Product Name : QHD HMD VR

Issue Date : 2017.09.06

Model Name : SDC350VR0

Description : 3.50" QHD(1440×1600) 16M Colors

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Proposed by			Customer's Approval
Designed	Checked	Approved	
H.S.Moon	J.H.Song	K.B.Lee	

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Revision History

Date	Rev. No.	Contents	Remark
2016-10-15	0.0	- Initial issue	-
2016-10-26	0.1	- Electro optical characteristics updated - Cosmetic Spec. updated - Add Driver IC LP mode guide	
2016-12-28	0.2	- Add Important Information - Operating manual updated (Add porch information) - Cosmetic Spec. updated - Drawing update	
2017-02-14	0.3	- Operating manual updated (Add porch information) - Cosmetic Spec. updated - Packing Specification updated	
2017-06-08	0.4	- Interface Updated (DSC included) - Electrical characteristics updated (Current spec) - Electro optical characteristics updated (Crosstalk Spec. included) - Operating manual updated (Add porch information) - Cosmetic Specification included (ETC)	
2017-06-14	0.5	- Drawing update (Add CP point)	
2017-07-18	0.6	- Electrical characteristics updated (Current spec) Mechanical Specification Changed (Dimensional Outline) - Cosmetic Spec. Changed (Uneven color stain Picture & pattern Condition Change 127G	
2017-07-20		- Maximum Rating updated (DCDC voltage) - Electro optical characteristics updated (DCDC voltage,Note)	
2017-08-08		- Delete Preliminary Mark - Cosmetic Spec. Changed (Delete Random Mura) - Packing Specification updated	
2017-08-29	0.9	- Cosmetic Spec. Changed	
2017-09-06	1.0	- Operating manual updated (Important information)	

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1. Scope

This Specification defines general provisions as well as inspection standards for AMOLED module supplied by SAMSUNG Display Co., LTD.,
If the event of unforeseen problems or unspecified items occurs, we naturally shall negotiate and agree to solution with customer.

2. Warranty

Basically, warranty term is 12 months of reliability characteristics of quality level after the outgoing date in SAMSUNG Display Co., LTD., and SAMSUNG Display Co., LTD., could compensate for defectives which happens within warranty term under condition that the products should be stored or be used as specified under normal condition within the contents of specificati
Otherwise, it is impossible to compensate for defectives when they happens by customer's mistake such as careless handing or circuit change, etc.
And after 12 months of warranty term, all replacements for defectives will be charged.

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This Specification stipulates the final and comprehensive requirements for the respective products hereof. Beyond this Specification, it is responsibility of the customer to explicitly disclose any additional requirements, information or reservations regarding these requirements to Samsung Display prior to implementation, where any and all disclosures of the customer shall be with an authorized representative of Samsung Display in writing. Samsung Display shall not be responsible for safety, performance, functionality, compatibility of the system with which the SAMSUNG DISPLAY-supplied components are integrated unless such features have been expressly communicated and described in the Specification. SAMSUNG DISPLAY MAKES NO GUARANTY OR WARRANTY, EXPRESS OR IMPLIED , INCLUDING BUT NOT LIMITED TO MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, TO ANY PARTY. Moreover, any party should do their own due diligence regarding these requirements prior to implementation.

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3. Features

1) Display Color : 16M Color
2) Display Format : 3.50" QHD Diamond : 1440x1600
3) Main Interface : MIPI DSI Dual 8-lane Video mode
   Support Interface : VESA DSC(Display Stream Compression) 1/2, 1/3
4) Driver IC : S6E3HA3 (SEC)

4. Mechanical Specification

Item	Specifications	Unit
Dimensional outline	62.472(W) x 100.91(H) x 0.846(T)	mm
Glass outline	62.472(W) x 73.28(H) x 0.616(T)	mm
Number of dots	1440(W) x RG(BG) x 1600(H)	Dots
Active area	59.4(W) X 66.0(H)	mm
Diagonal Inch	3.50	inch
Pixel pitch	41.25(W) X 41.25(H)	um
Glass Thickness (ENCAP/LTPS)	0.3/0.3	mm

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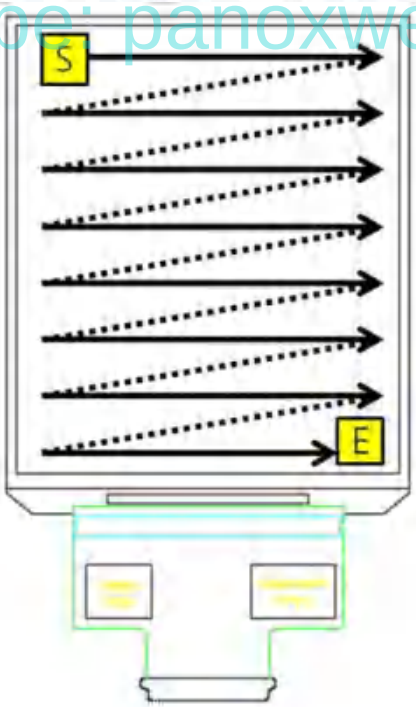
< Display Orientation >



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5. Maximum Rating

Item		Symbol	Min.	Max.	Unit	Note
Supply voltage (Display)	Driver-IC	VCI	-0.3	5.0	V	1),2)
		VDD3	-0.3	2.7	V	1),2)
	DCDC	VLIN	-0.3	10.0	V	3)
		ELVDD	-0.3	6.0	V	3)
		ELVSS	-6.5	0.3	V	3)
Operating temperature		Top	-20	70	℃	-
Storage temperature		Tstg	-30	75	℃	-
Humidity		Hstg	10	90	RH	

Note 1) Supply voltage should satisfy the below condition of VCI, VDD3 > VSS (GND).

Note 2) If the supplied voltage exceeds the maximum limitation, LSI can be damaged permanently. Therefore, while operating, it is recommend to use LSI within the maximum electrical limitation. If not, LSI can cause decreased reliability or operational problems.

Note 3) VBAT is input supply to DCDC IC which is mounted on SET board. And ELVDD and ELVSS, which are supply voltage for display, are output power from DCDC IC.

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6. Electrical Characteristics

6-1. DC Characteristics.

-. Test Conditions: VDD3=1.8V, VCI=3.3V, VSS=0V, VBAT=3.8V
Temp=25℃ unless otherwise specified.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Supply voltage (Display)	Logic Voltage	VDD3	-	1.65	1.8	1.95	V	
	Analog Voltage	VCI	-	2.9	3.3	4.8		
	EL Driving	ELVDD	±0.5% @No load	4.577	4.6	4.623		1)2)
		ELVSS	±30mV @No load	-1.4	-	-5.4		3)
	Analog Voltage	VLIN	±1% @No load	7.227	7.3	7.373		
Logic Input Voltage (Display)	"H" level	VIH	-	0.7*VDD3	-	VDD3	V	
	"L" level	VIL	-	0.0	-	0.3*VDD3		
Logic Output Voltage (Display)	"H" level	VOH	IOH = -1mA IOL = +1mA	0.8*VDD3	-	VDD3	V	
	"L" level	VOL		0.0	-	0.2*VDD3		
Current Consumption (Display)	Display mode	IVCI	Frame frequency=90Hz white pattern	-	3.0	6.5	mA	
		IVDD3		-	40	55	mA	
		IBAT		-	70	85	mA	2)
Frame Frequency		f_{FRM}	-		90		Hz	

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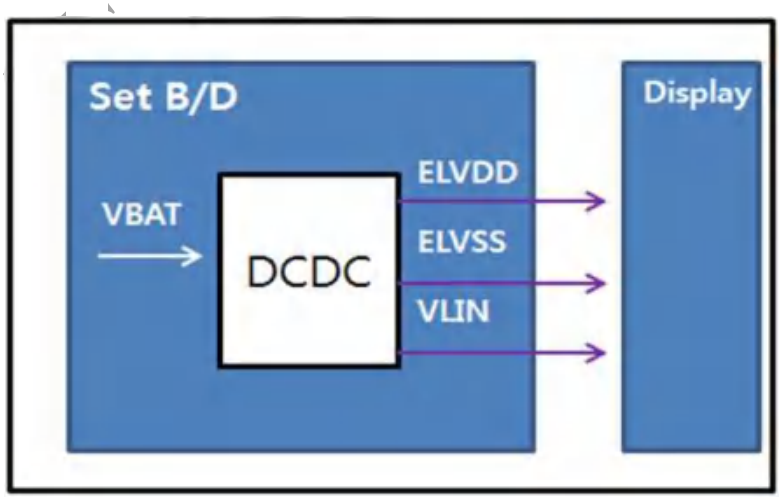
Note 1) VBAT is input supply of DCDC IC mounted on SET board.
ELVDD & ELVSS & VLIN is output from DCDC-IC
Note 2) IBAT is measured at DCDC input, VBAT.
Note 3) Each Cell has different ELVSS

※ DCDC IC : TPS65633B (TEXAS INSTRUMENTS)



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7. Electro-optical characteristics

Item		Symbol	Temp	Condition	Min.	Typ.	Max.	Unit	Note
Brightness			25℃	Normal (White Mode)	130	166	200	cd/m²	Center brightness
Uniformity			25℃	Normal (White Mode)	75	85	-	%	(1)
Contrast ratio		K	25℃	Φ=0° ,θ=0°	10,000	-	-	-	(1),(2)
Color of CIE coordinate	White	x	25℃	Φ=0° θ=0°	0.280	0.300	0.320	-	(1),(2),(3)
		y			0.300	0.320	0.340	-	
	Red	x			0.637	0.667	0.697	-	
		y			0.302	0.332	0.362	-	
	Green	x			0.185	0.235	0.285	-	
		y			0.668	0.718	0.768	-	
	Blue	x			0.100	0.140	0.180	-	
		y			0.005	0.045	0.085	-	
Color Gamut			25℃	vs. NTSC	85	100	-	%	CIE1931
Gamma			25℃	-	2.0	2.2	2.4	-	(4)
Crosstalk			25℃	-	0	-	5	%	(5)
Life Time			25℃	166cd/m², 240hr	93			%	B10 (5)

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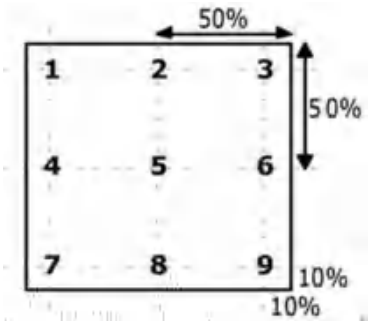
Above optical spec is only based on the brightness of 166nit normal white mode

Note 1) Uniformity Measuring Point



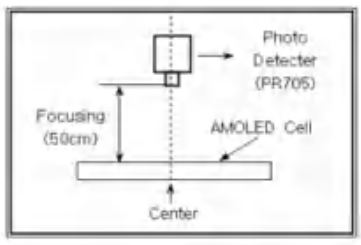
Uniformity = Lmin / Lmax * 100 [%]

Note 2) Definition of contrast ratio (K)

$$\text{Contrast Ratio(K)} = \frac{\text{Brightness of White pattern center at } \underline{166\ cd/m^2}}{\text{Brightness of Black pattern center at } \underline{166\ cd/m^2}}$$

Note 3) Optical measuring system

Dark Room Chamber (External Light : dark state)



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Portable System

CA-210 or CA-310 can be used to measure luminance and color coordinate of Full White/Red/Green/Blue.

[CA-210]

[CA

Note) If flicker is detected by visually, SDC shall negotiate and agree to solution with customer.

Note 4) gamma is calculated value

- gamma calculation formula

$$\log(L - L_b) = \gamma \log(V) + \log(a)$$

L_b = black luminance level, V = gray level

- Measurement point for gamma calculation

48gray, 72gray 104gray, 132gray, 164gray, 192gray, 224gray, 252gray, 255gray

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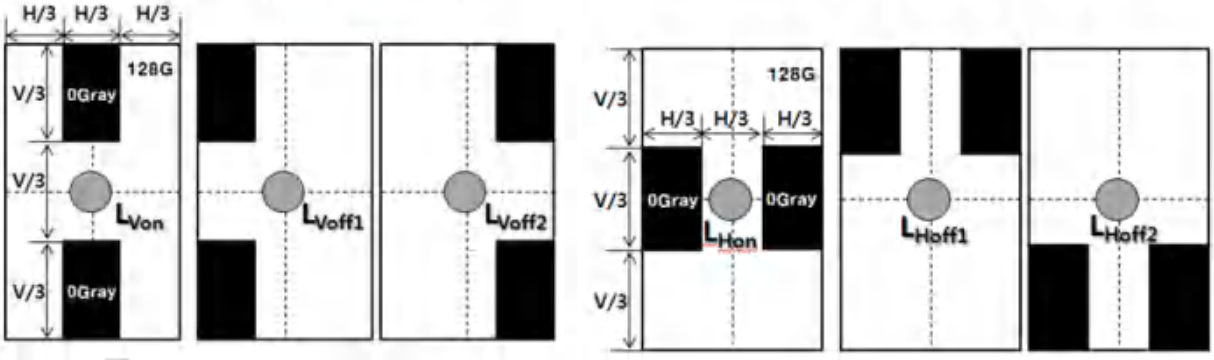
Note 5) Crosstalk Measurement

Vertical Crosstalk

$$Crosstalk(V) = \left| \frac{L_{Von} - (L_{Voff1} + L_{Voff2})/2}{(L_{Voff1} + L_{Voff2})/2} \right| \times 100$$

Horizontal Crosstalk

$$Crosstalk(H) = \left| \frac{L_{Hon} - (L_{Hoff1} + L_{Hoff2})/2}{(L_{Hoff1} + L_{Hoff2})/2} \right| \times 100$$

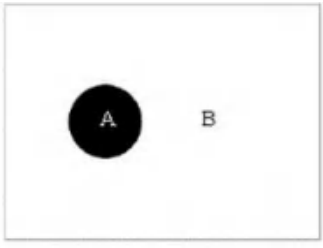


- Measurement Position : Display Center, D<8mm with spectrometer, Circle

Note 6)

Life time = (A luminance @240hr) – (B luminance drop @240hr)

(A : Non aging area, B : aging area)



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8. I/O Connection & Block Diagram

8-1. I/O Connection

No	Pin Name	Description	I/O	No	Pin Name	Description	I/O
1	GND	Ground	G	32	GND	Ground	G
2	AVDD	D-IC Power Connect to DC-DC Output	I	33	DSI0CN	Differential Clock 0_N	I/O
3				34	DSI0CP	Differential Clock 0_P	I/O
4	VCI	D-IC Power	I	35	GND	Ground	G
5				36	DSI0D1N	Differential Data 0_1N	I/O
6	VDDIO	D-IC Power	I	37	DSI0D1P	Differential Data 0_1P	I/O
7				38	GND	Ground	G
8	RESET_N	Reset		39	DSI0D2N	Differential Data 0_2N	I/O
9	GND	Ground	G	40	DSI0D2P	Differential Data 0_2P	I/O
10	GND	Ground	G	41	GND	Ground	G
11	DSI1D3N	Differential Data 1_3N	I/O	42	GND	Ground	G
12	DSI1D3P	Differential Data 1_3P	I/O	43	F_CSN	SDC internal use only Leave it Open	N
13	GND	Ground	G	44	F_SCLK		
14	DSI1D0N	Differential Data 1_0N	I/O	45	F_IO<0>		
15	DSI1D0P	Differential Data 1_0P	I/O	46	F_IO<1>		
16	GND	Ground	G	47	GND	Ground	G
17	DSI1CN	Differential Clock 1_N	I/O	48	ERR_FG	Error Flag	O
18	DSI1CP	Differential Clock 1_P	I/O	49	TE	TE Signal	O
19	GND	Ground	G	50	REGCTRL	EL Control	O
20	DSI1D1N	Differential Data 1_1N	I/O	51	AVDD_EN	AVDD Cotrol	O
21	DSI1D1P	Differential Data 1_1P	I/O	52	VPP	Connect to GND	G
22	GND	Ground	G	53	GND	Ground	G
23	DSI1D2N	Differential Data 1_2N	I/O	54	ELVDD	EL Power Connect to DC-DC Output	I
24	DSI1D2P	Differential Data 1_2P	I/O	55			
25	GND	Ground	G	56			
26	GND	Ground	G	57	N/C	Leave it Open	N
27	DSI0D3N	Differential Data 0_3N	I/O	58	ELVSS	EL Power Connect to DC-DC Output	I
28	DSI0D3P	Differential Data 0_3P	I/O	59			
29	GND	Ground	G	60			
30	DSI0D0N	Differential Data 0_0N	I/O	61	NC	Leave it Open	N
31	DSI0D0P	Differential Data 0_0P	I/O				

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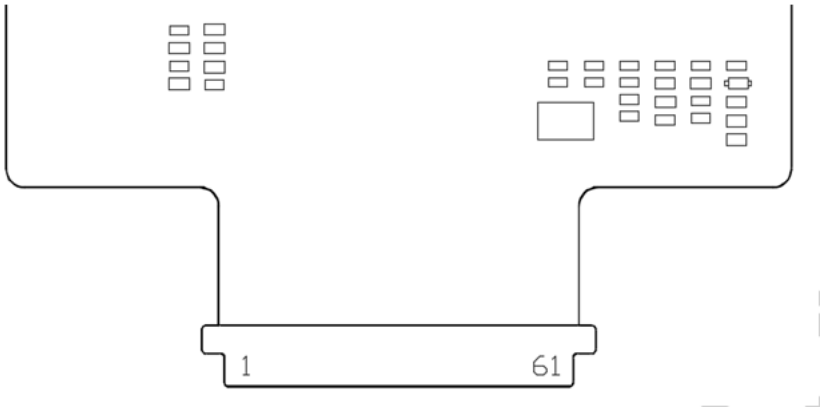
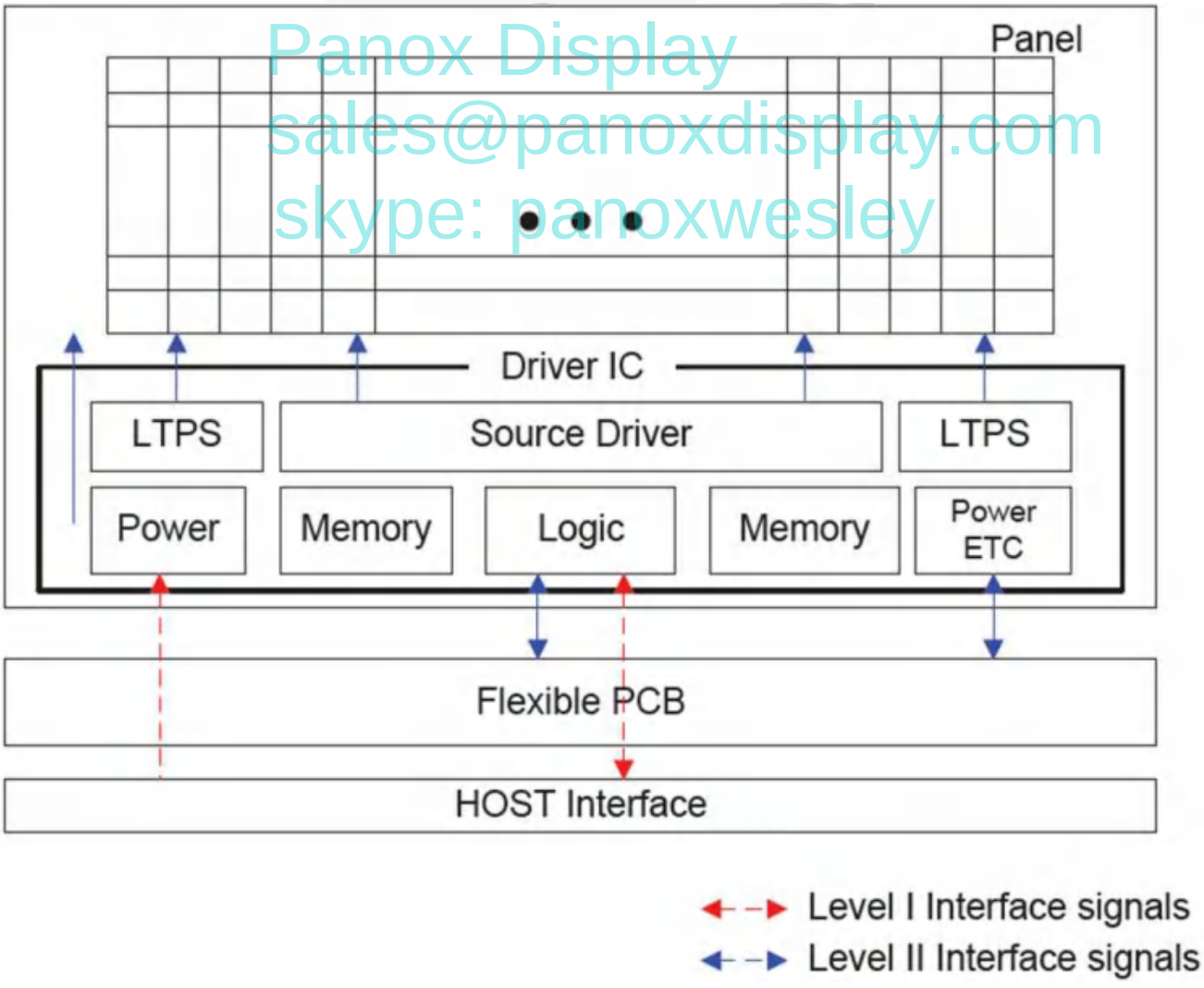
<Pin layout of ZIF contact pads>



Connector :

8-2. Circuit block diagram (Display)



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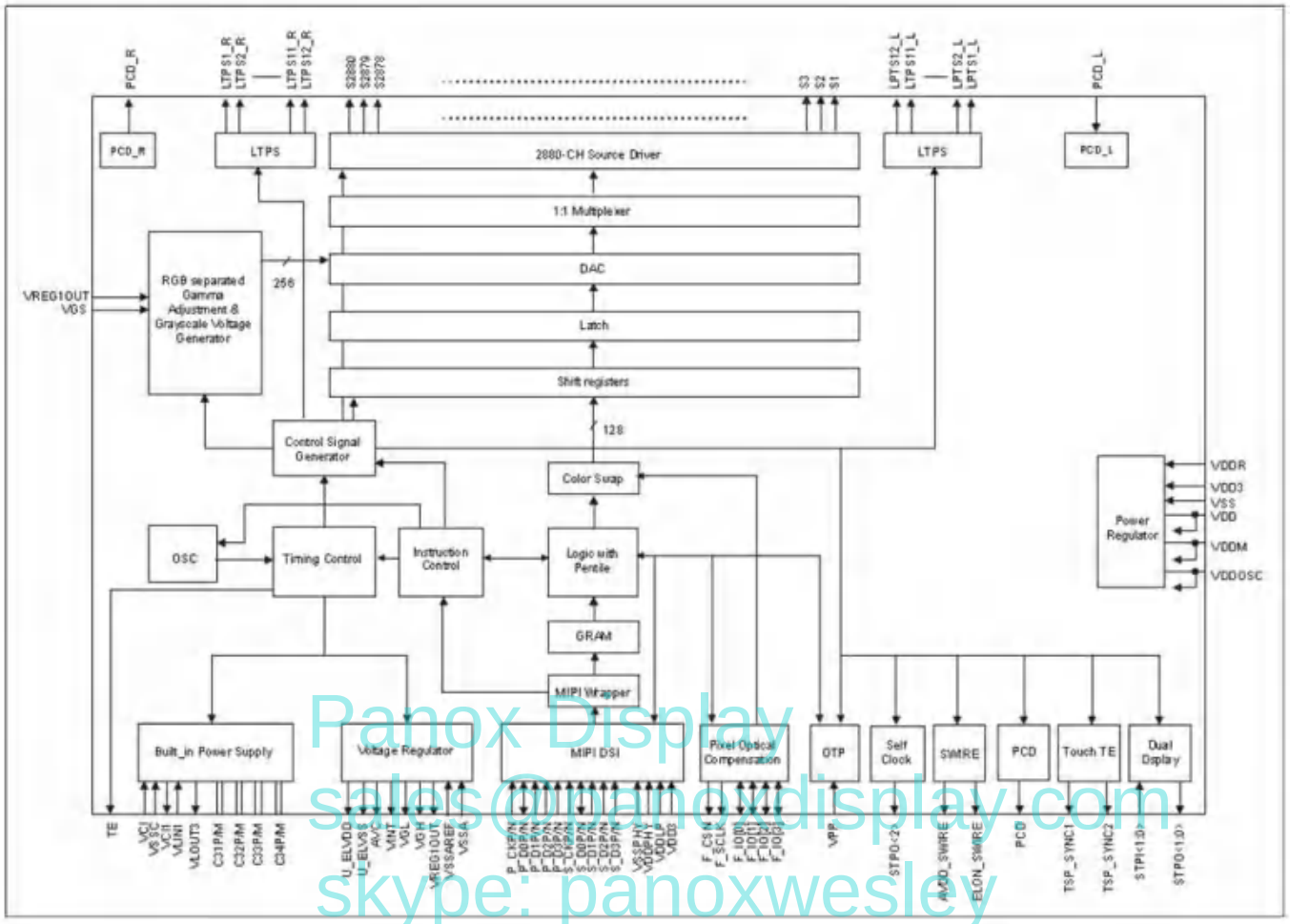
8-3. Circuit block diagram (Driver IC for display)



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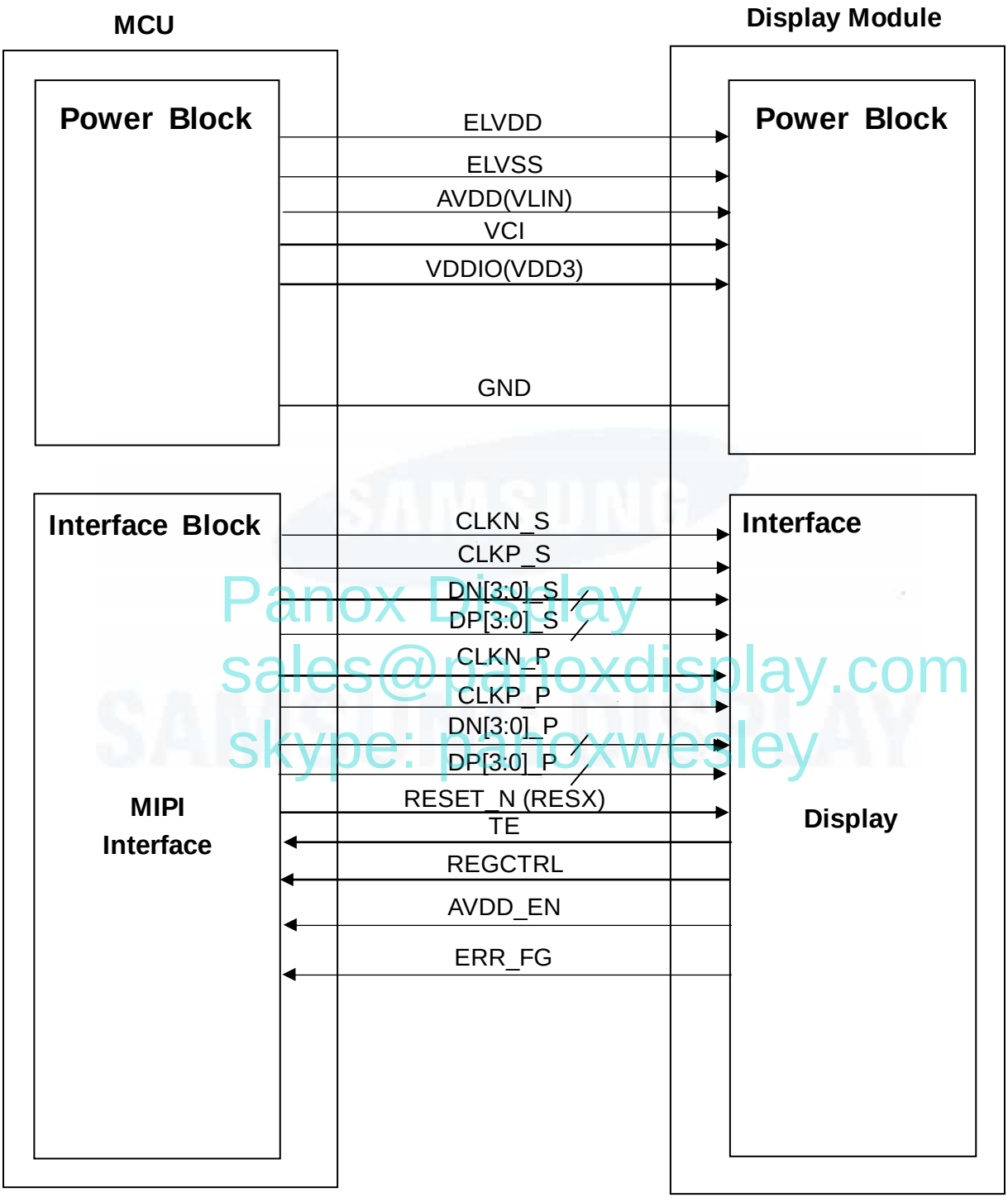
8-4. MCU and Display Module Interface Configuration



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9. Recommended Operating Sequence

9-1. Operating condition

Model	AMS350MU04			
LDI	S6E3HA3 (SEC S.LSI)			
Resolution	1440(H) x 1600(V)			
Condition	**I/F**	MIPI 8 Lane (Dual DSI) Video Mode		
	MIPI Speed	**HS**	Typ.	950 Mbps
		LP	**AP IC**	6.2Mbps ~ 10Mbps
			IC AP	Typ. 8.7Mbps
	Porch (Video only)	**HFP / HBP(With HS)**		HSW : 70ns ↑ HBP 110ns HFP 250ns↑ (Refer to Note)
		VFP / VBP(With VS)		10/ 14 (ex. VBP : 2,VS :12)
	Frame Freq.	Typ.		90Hz
Input Voltage	**VBAT**	Typ.		3.8V
	VCI	Typ.		3.3V
	VDD3 (VDDIO)	Typ.		1.8V
	VLIN (AVDD)	Typ.		7.3V
Output Voltage	**ELVDD**	Typ		4.6V
	ELVSS	Variable		-5.4V ~ -1.4V

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Note)

■Spec Restriction List

- MIPI speed is up to 1.1Gbps per lane in case of 4 lane.
- Minimum setting value HSW : 70ns ↑, HBP : 110ns↑, HFP : 250ns↑.
- VBP register must be set more than 3. (VBP+VS ≥3) Vertical back porch includes VSA (Vertical sync. Area line).

Display line + VBP + VFP should be even value. Minimum value of VFP Register is 3.

It is necessary to wait 20ms before sending read command. The execution of Applied command must be done before vertical sync packet.

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< Driver IC LP mode guide >

■ First LP command does not work right after frame data writing in HS mode

- When sending register command in LP mode, first command is ignored
- There is no problem to send register command in LP mode after sending NOP(0x00) command in LP mode
- There is no problem to send register command in HS mode (SDC recommend)
- There is no problem to send register of no parameter in LP mode

< Important Information >

■ Display power (VCI, VDDIO, AVDD) should be turned down immediately when any of DSI signals (CLK and DATA) are disconnected or in unknown state during Display On Status.

■ Clock lane always must be activated after sleep out command @ video mode

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9-2. Operating Sequence

9-2-1. Power On Sequence

Order	Sequence	Remark
1	Power Off Status	
2	System Power on (VBAT/VCI/VDD3)	Note1
3	**Wait 10ms**	
4	Data, Clk : LP 00 01 11	Note2
5	Activate Reset (System Reset)	Note1
6	**Wait 5ms**	
7	Sync Packet Start (HS)	
8	**Wait 5ms**	
9	OSC Timing Control Setting	Refer to Ch.9-3
10	Interface Setting	Refer to Ch.5
11	Sleep Out(11h)	
12	**Wait 5ms**	
13	OSC Timing Control Setting	Refer to Ch.9-3
14	Interface Setting	Refer to Ch.5
15	Pentile Setting	Refer to Ch.6
16	**Wait 120ms**	
17	Error Flag Setting	Refer to Ch.9
18	Brightness Setting	Refer to Ch.7
19	Memory Setting	Refer to Ch.8
20	Memory Access(2Ch/3Ch)	
21	Display On(29h)	
22	Display On Status	

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9-2-2. Power Off Sequence

Order	Sequence	Remark
1	Display On Status	
2	Display Off (28h)	
3	Sleep In (10h)	
4	**Wait 120ms**	
5	Sync Packet Stop (HS →LP11→OFF)	
6	RESET OFF (H→L)	
7	System Power Off (VDD3/VCI/VBAT)	Note3
8	Power Off Status	

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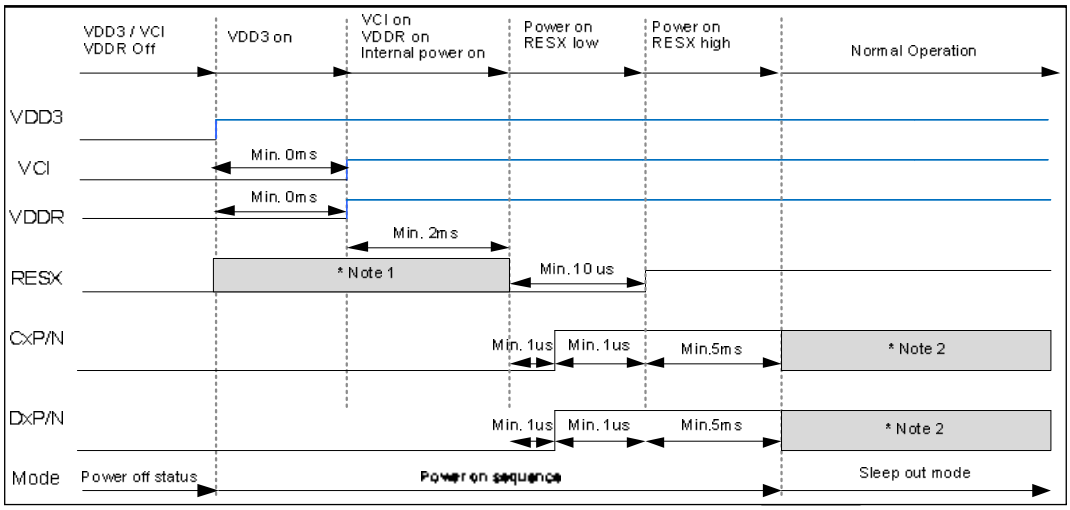
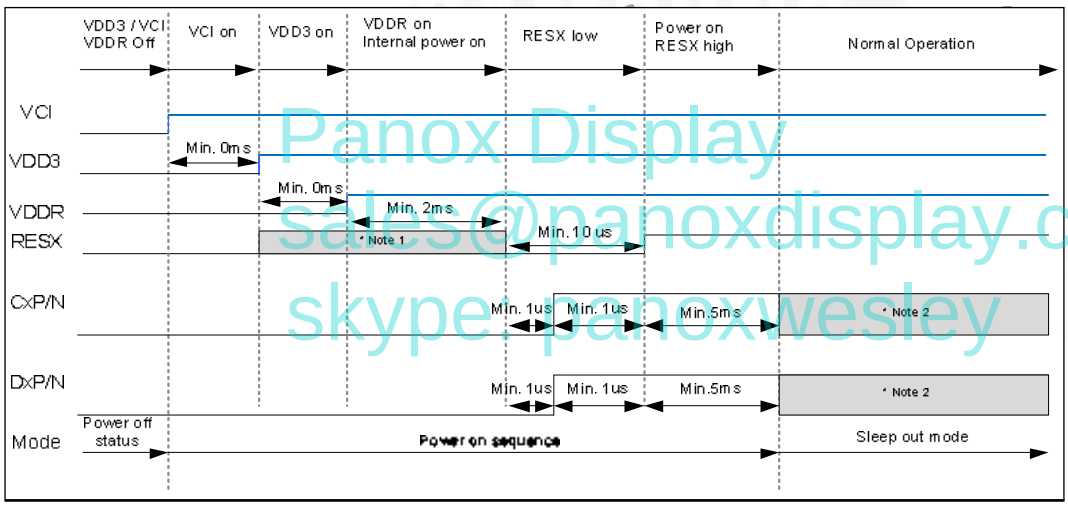
Note1) System Power on



[Case1- VCI to VDD3 Power On]



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[Case2- VDD3 to VCI Power on]

1. RESX can be either high or low state after VDD3 has been supplied.

2. Global operating timing should be observed.

3. When measuring timings for the power lines, 10%-90% of its rising and falling edge are reference points.

4. When measuring timings for the logic signals, 30%-70% of its rising and falling edge are reference points.

Note2) LP Status : LP11 maintenance required during Reset

Note3) Clock lane always must be activated after sleep-out command@video mode

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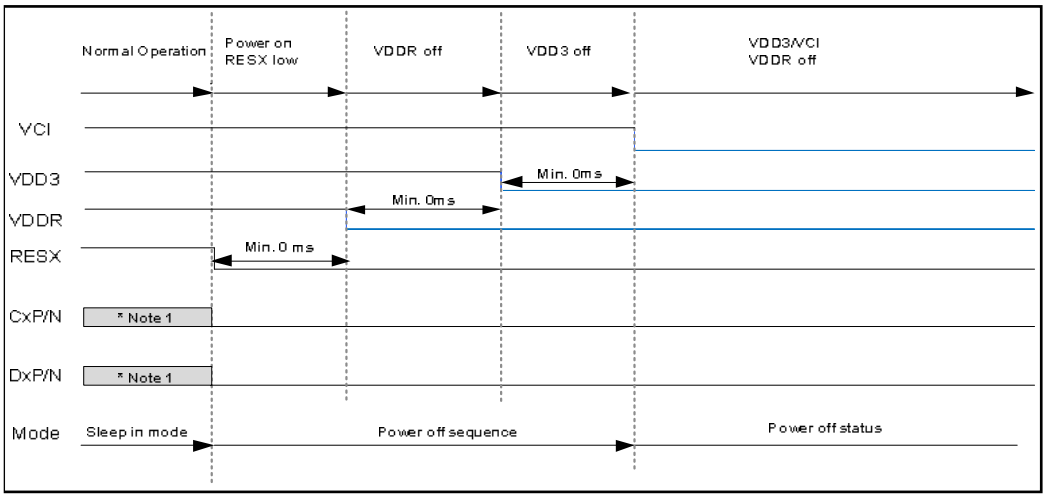
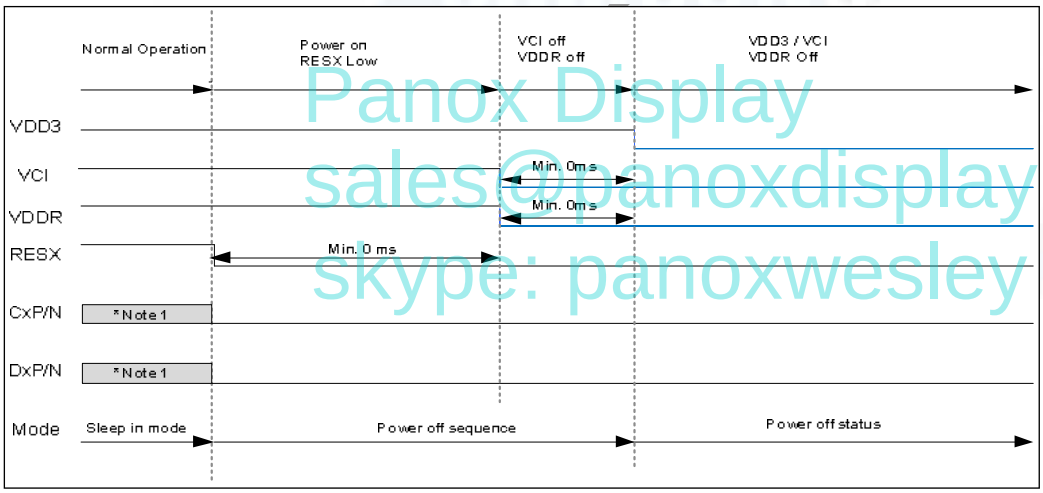
Note3) System Power off



[Case1- VCI to VDD3 Power off]



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[Case2- VDD3 to VCI Power off]

1. **Global operating timing should be observed.**
2. **When measuring timings for the power lines, 10%-90% of its rising and falling edge are reference points.**
3. **When measuring timings for the logic signals, 30%-70% of its rising and falling edge are reference points.**

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9-3. OSC Timing Control Setting

Command	R/W	Values	Description
0xFC	W	{ 0x5A, 0x5A };	TEST KEY Enable
0xB0	W	{ 0x2F };	Internal OSC Timing Control
0xFE	W	{ 0x21 };	
0xFC	W	{ 0xA5, 0xA5 };	TEST KEY Disable

9-4. Interface Setting

Command	R/W	Values	Description
0xF0	W	{ 0x5A, 0x5A };	TEST KEY Enable
0xF9	W	{ 0x03 };	Dual DSI
0xF2	W	{ 0x41, 0x5A }; /* Video Mode */	
0xF0	W	{ 0xA5, 0xA5 };	TEST KEY Disable

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9-5. Pentile Setting

Command	R/W	Values	Description
0xF0	W	{ 0x5A, 0x5A };	TEST KEY Enable
0xC2	W	{ 0x00, 0x00, 0xD8, 0xD8, 0x00, 0x80, 0x2B, 0x05, 0x08, 0x0E, 0x07, 0x0B, 0x05, 0x0D, 0x0A, 0x15, 0x13, 0x20, 0x1E };	PENTILE Setting
0xF0	W	{ 0xA5, 0xA5 };	TEST KEY Disable

9-6. Brightness Control (Max. Luminance : 166nit)

Command	R/W	Values	Description
0x53	W	{ 0x20 }; /*Brightness On SETTING*/	Brightness Control
0x51	W	{ 0xFF }; /*Luminance setting*/ EX) /* 0xFF : 166nit */	WRDISBV

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9-7. Memory Setting

Command	R/W	Values	Description
0x2A	W	{ 0x00,0x00,0x05,0x9F }; /*CASET 1440	Column Address Set

9-8. ERR_FG Setting

Command	R/W	Values	Description
0xF0	W	{ 0x5A, 0x5A };	TEST KEY Enable
0xED	W	{ 0xXX };	ERR_FG Setting (Note)
0xF0	W	{ 0xA5, 0xA5 };	TEST KEY Disable

Note) HSYNC & HS CLK Flag necessary

Type	Access	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	R/W	1	1	1	0	1	1	0	1	ED
1st Para	R/W	Reserved	Frag of Vlin1	Frag for HSYNC		Flag of ELVDD	Flag of VLOUT3	Frag for HS CLK	Frag of MIPI	

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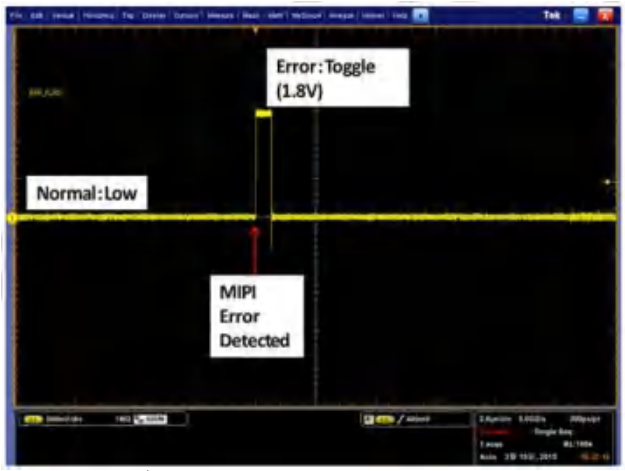
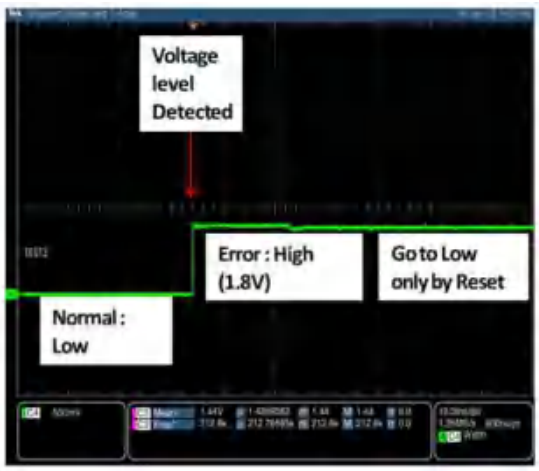


< MIPI Signal Wave Form>



< Voltage Level Wave Form >

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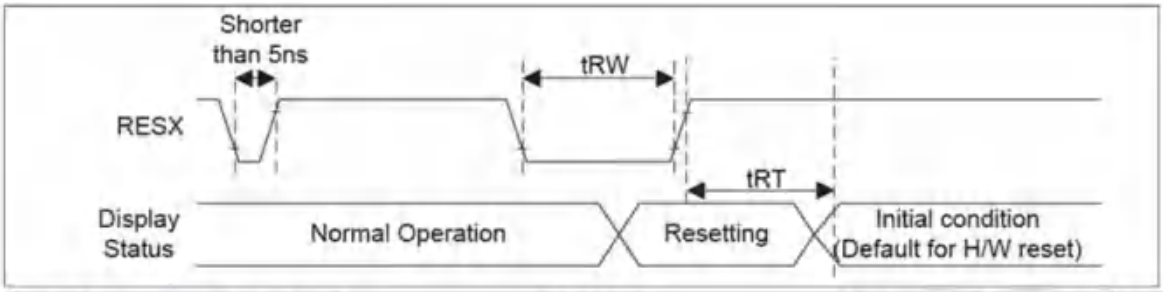
10. AC characteristics

10-1. Reset Timing



Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	tRW	Reset pulse duration	10	–	µs
	tRT	Reset cancel	–	5(6)	ms
			–	120(7)(8)	
	tr	Reset Rising Time	–	10	ns
	tf	Reset Falling Time	–	10	ns

NOTE:

1. The reset cancel includes also required time for loading ID bytes (or similar) from EEPROM (or similar) to ID (or similar) registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Reset Operation According to Reset Pulse Width Condition.

RESX Pulse	Action
Shorter than 5 µs	Reset rejected
Longer than 10 µs	Reset
Between 5 µs to 10 µs	Reset starts

3. During the Resetting period, the display will be blanked (The display enters blanking sequence, in which maximum time is 120 ms, when Reset Starts in Sleep Out-mode. The display remains in the blank state at Sleep In-mode) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below: (Positive Noise Pulse When Reset Low)

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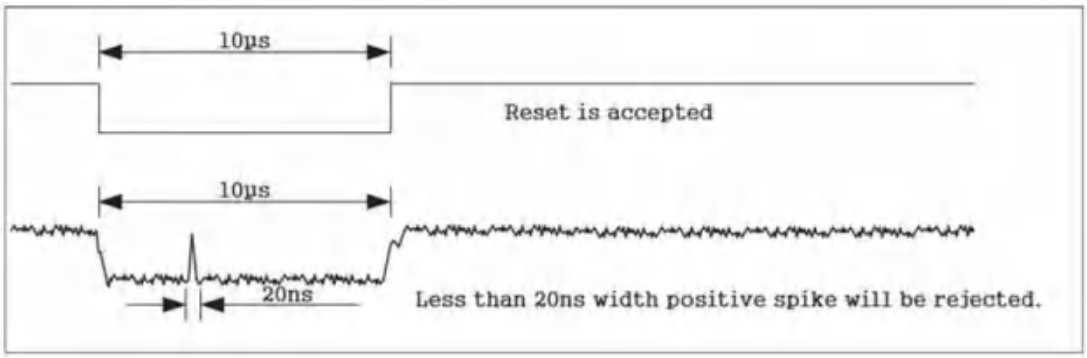

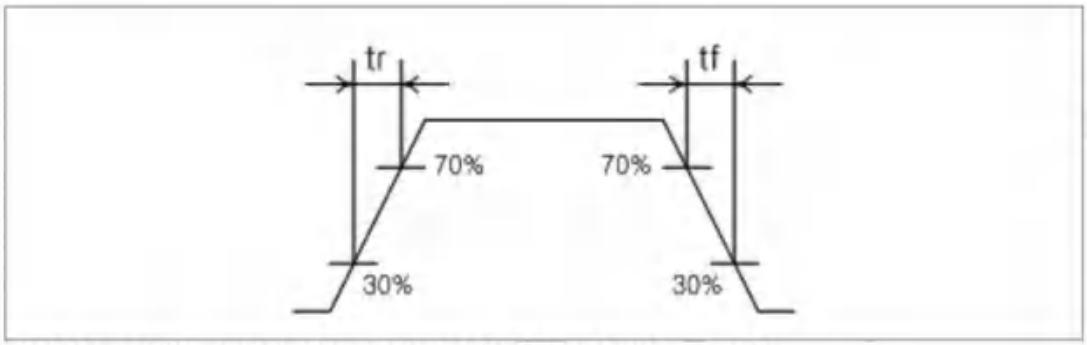

5. During the resetting period, MIPI Data and CLK lane have to be LP11.

6. When Reset is applied during Sleep In Mode.

7. When Reset is applied during Sleep Out Mode.

8. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent out for 120 msec.

9. HW reset cannot cause any spike/glitch on control or data lines or spike/glitch/noise on power (VCI and VDD3) lines.

10. The display module can also initialize and calibrate DSI - CLK ± DSI-D0 ± and DSI - D1 ± lanes within 5 ms if it is needed when DSI has been selected to use.

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11. MIPI characteristics

11-1. DC Characteristics

Figure 11-1

Items		Parameter	Min.	Nom.	Max.	Unit	Note
LP_TX	Thevenin output high level	VOH	1.1	1.2	1.3	V	
	Thevenin output low level	VOL	– 50	–	50	mV	
	Output impedance of LP transmitter	ZOLP	110	–	–	Ω	(1)
HS_RX	Common-mode voltage HS receive mode	VCMRX (DC)	70	–	330	mV	(2) (3)
	Differential input high threshold	VIDTH	–	–	70		
	Differential input low threshold	VIDTL	– 70	–	–		
	Single-ended input high voltage	VIHHS	–	–	460		(2)
	Single-ended input low voltage	VILHS	– 40	–	–		
	Single-ended threshold for HS termination enable	VTERM-EN	–	–	450		
	Differential input impedance	ZID	80	100	125	Ω	
LP_RX	Logic 1 input voltage	VIH	880	–	–	mV	
	Logic 0 input voltage, not in ULP State	VIL	–	–	550		
	Input hysteresis	VHYST	25	–	–		(4)
LP_CD	Logic 1 contention threshold	VIHCD	450	–	–		
	Logic 0 contention threshold	VIOLED	–	–	200		

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NOTE:
1. Even though a maximum value for ZOLP is not specified, the output impedance of the LP transmitter ensures that the TRLP/TFLP specification is met
2. Excluding additional RF interference of 100 mV peak sine wave beyond 450 MHz.
3. This Table 2-9 value includes a ground difference of 50 mV between the transmitter and the receiver, the static common- mode level tolerance and variations below 450 MHz.
4. Temperature condition = 25 °C.

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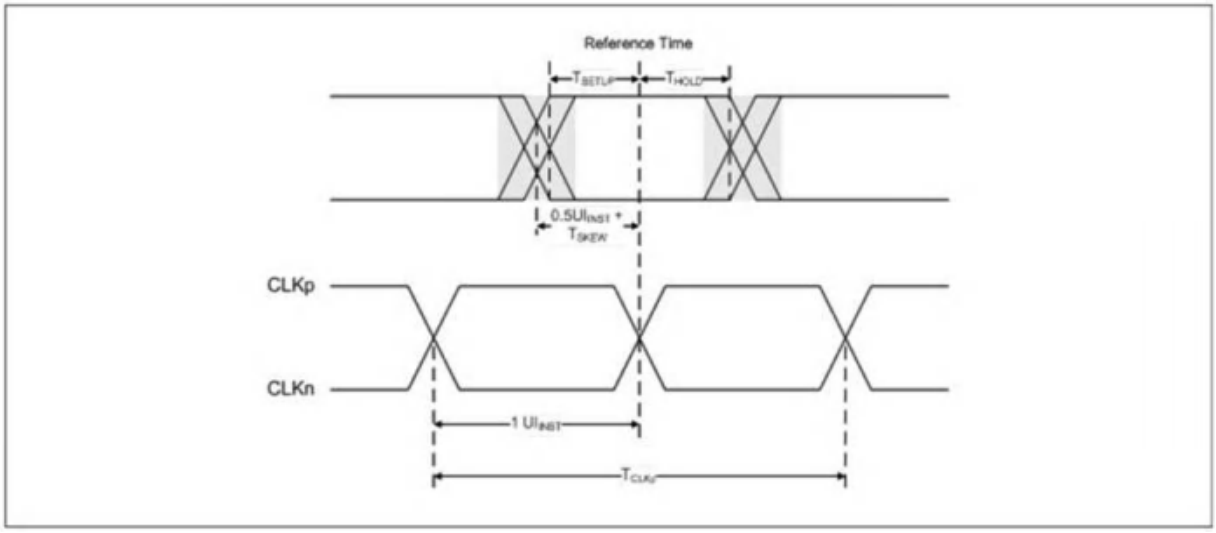
11-2. High Speed Data-clock Timing



Clock Parameter	Symbol	# of d-lane	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	4	0.909	–	12.5	ns	(1) (2)

NOTE:
1. This value corresponds to a minimum 80 Mbps data rate.
2. The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

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Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to clock skew (Measured at transmitter)	TSKEW[TX]	– 0.2	–	0.2	UI_{INST}	(1)
Data to clock setup time (Receiver)	TSETUP[RX]	0.2	–	–		(2)
Clock to data hold time (Receiver)	THOLD[RX]	0.2	–	–		

NOTE:
1. Total silicon and package delay budget of 0.3 × UI_{INST}
2. Total setup and hold window for receiver of 0.3 × UI_{INST}
3. TSETUP[RX] and THOLD[RX] are only for RX without FPCB and connector and guaranteed by design.

11-3. AC Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
Thost-enable	Host output enable time	0	–	24 × t-bit	ns
Thost-disable	Host output disable time, entire length of the Turn-around 1 field	0	–	24 × t-bit	
Tclient-enable	Client output enable time, entire length of the Turn-around 1 field	0	–	24 × t-bit	
Tclient-disable	Client output disable time, measured from the end of the last bit of the Turn-around 2 field	0	–	24 × t-bit	

NOTE: t-bit = 1/Link_Data_Rate, where Link_Data_Rate is the bit rate of a single data pair. (For example, if the average forward link bit rate is 150 Mbps, then t-bit = 1/150 Mbps = 6.6 ns)

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12. Interface

12-1. MIPI DSI Feature

- (4 data lanes) x 2 ports DSI.
- HS (High Speed) transmission (Unidirectional) up to 1.1Gbps/lane for command and data.
- LP (Low Power) transmission (Bidirectional)

MIPI Alliance Specification for D-PHY

Version 1.1 7-Nov-2011

MIPI Alliance Specification for Display Serial Interface

Version 1.2 16-Jun-2014

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12-2 MIPI D-PHY

12-2-1. Global Operation

Figure below shows the operational flow diagram for a Data Lane Module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, Escape mode, Turnaround and Initialization

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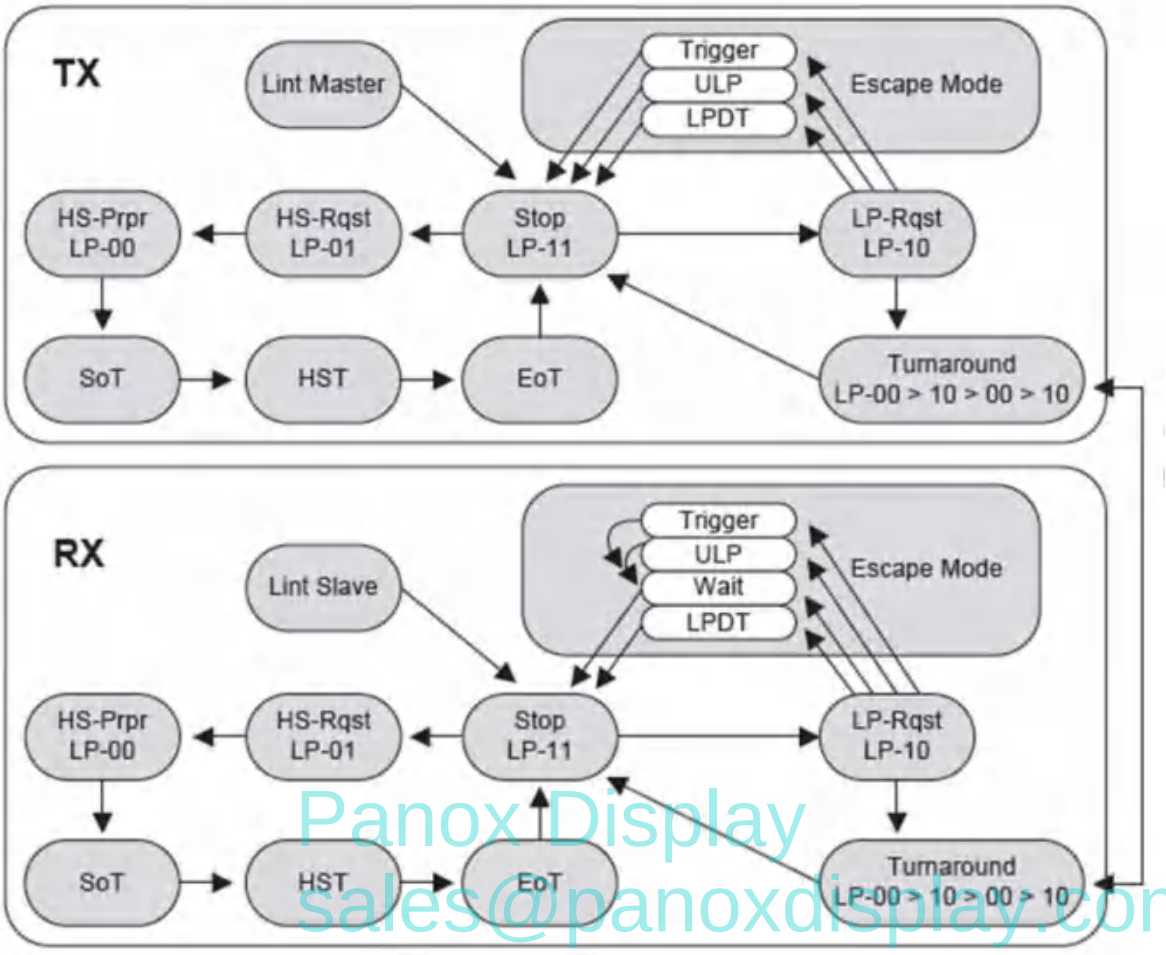

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State Code	Line Voltage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

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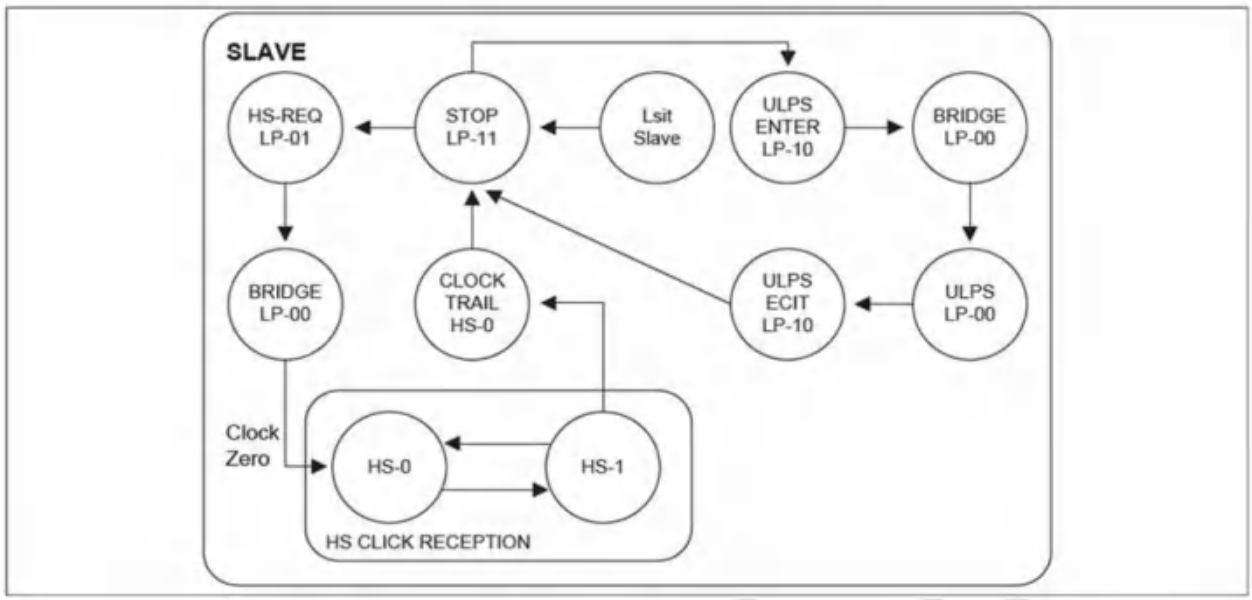
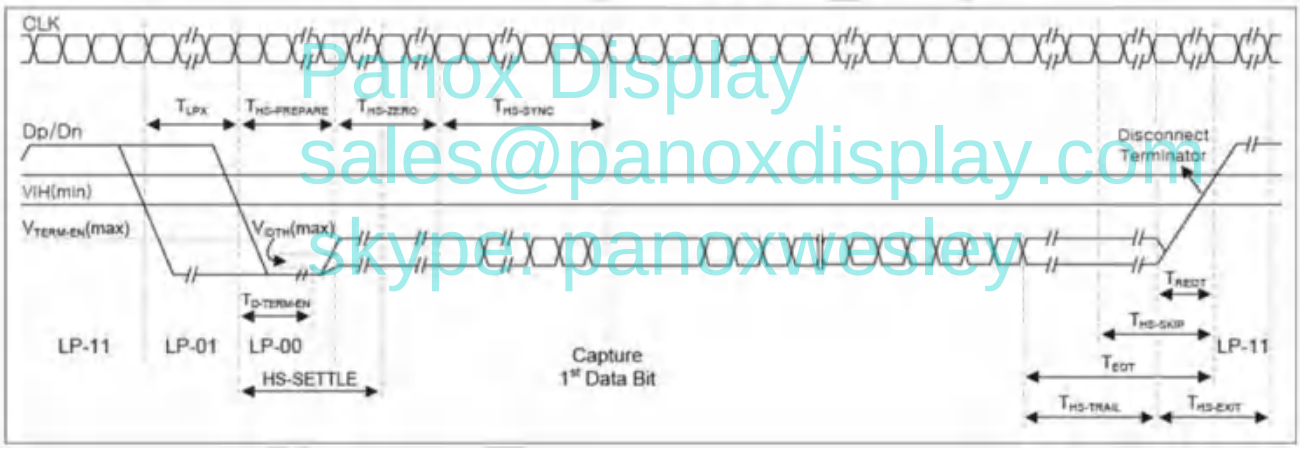
12-2-3. Clock Lane Flow Diagram



12-2-4. High Speed Data Transmission



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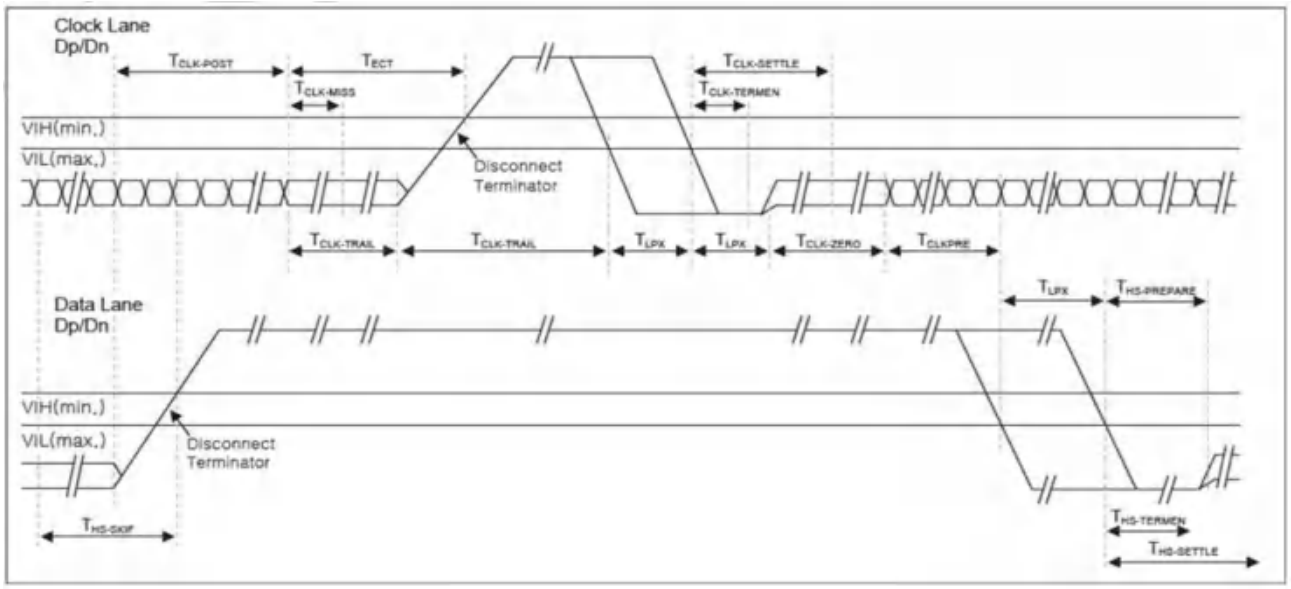
12-2-5. High Speed Clock Transmission



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12-2-6. Escape Mode

Escape Mode is a special mode of operation for Data Lanes using Low-Power states. With this mode some additional functionality becomes available. Though Escape Mode operation is optional in D-PHY, the host processor and peripheral in which Command Mode operation is supported shall implement reverse-direction Escape Mode as well as forward direction Escape Mode.

A Data Lane shall enter Escape Mode via an Escape Mode Entry procedure (LP-11,LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape Mode in Space state (LP-00). If an LP-10 is detected after the first Bridge state or an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape Mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

Once Escape Mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. ***Table 12-1*** lists all currently available Escape Mode commands and actions. All unassigned commands are reserved for future expansion

Table 12-1 MIPI Escape Mode Entry Code

Escape Mode Action	Command Type	Entry Command Pattern (First Bit Transmitted to Last Bit Transmitted)	S6E3HA3X92	
			LP-RX	LP-TX
Low-Power Data Transmission	mode	11100001	O	O
Ultra-Low Power State	mode	00011110	O	-
Undefined-1	mode	10011111	-	-
Undefined-2	mode	11011110	-	-
Reset-Trigger[Remote Application]	Trigger	01100010	O	-
Unknown-3 [TE Trigger]	Trigger	01011101	-	O
Unknown-4 [Acknowledge Trigger]	Trigger	00100001	-	O
Unknown-5	Trigger	10100000	-	-

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12-2-7. Lower Power Data Lane Operation

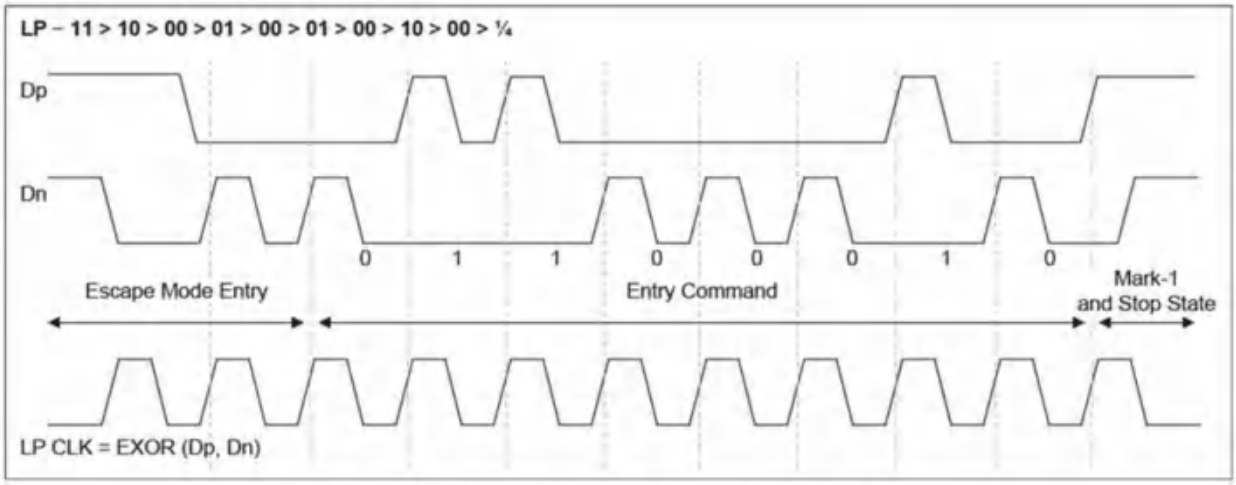

Figure 12-1 **Trigger-Reset Command in Escape Mode**

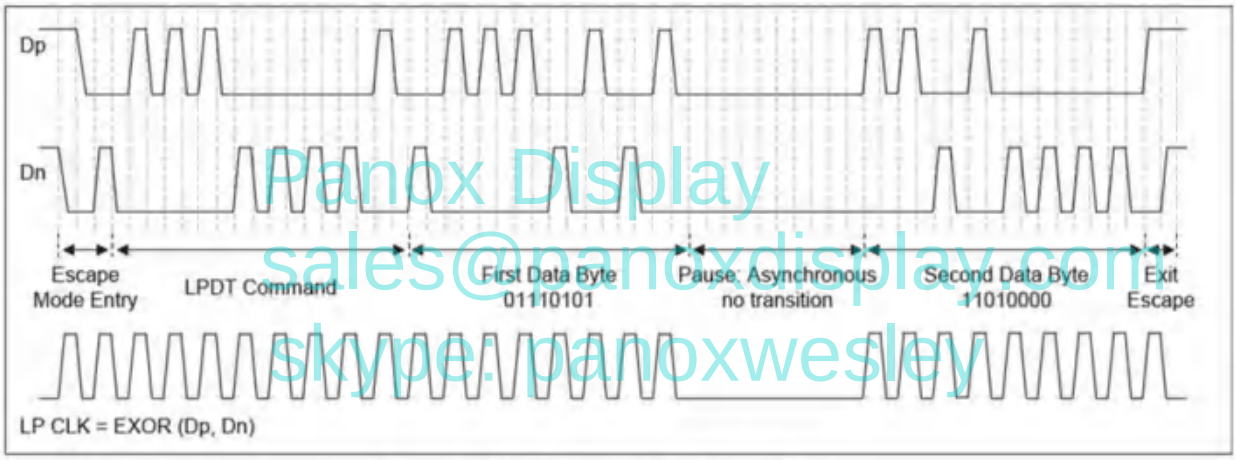

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Figure 3-7 Low Power Data Transmission

12-2-8. Ultra-low Power State

If the Ultra Low Power Entry Command is sent after an Escape Mode Entry command, the Lane shall enter the Ultra Low Power State (ULP). This Command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra Low Power State is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop State. *Figure 3-8* shows an Ultra Low Power Entry and Exit example.

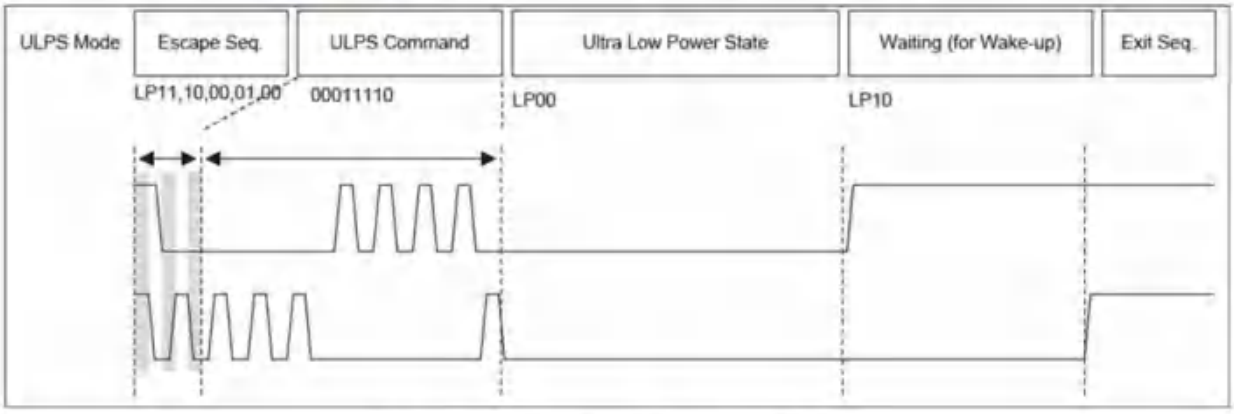

Figure 12-3 **Ultra Low Power State Mode**

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The Host processor provides LP10 state before Exit to wait for the MIPI SLAVE's stabilization. ULPS packet turn off the PHY_IO HS_RX. The ULPS turn off the bias current of HS_RX. The LP10 wakeup state is a trigger to turn on the HS_RX before normal STOP state.

12-2-9. Remote Application Reset

Remote Application Reset Command is used in case of transmission from the host processor to the peripheral. If the Entry Command Pattern matches the Remote Application Reset Command a Trigger is flagged to the protocol at the peripheral side via the logical PPI.

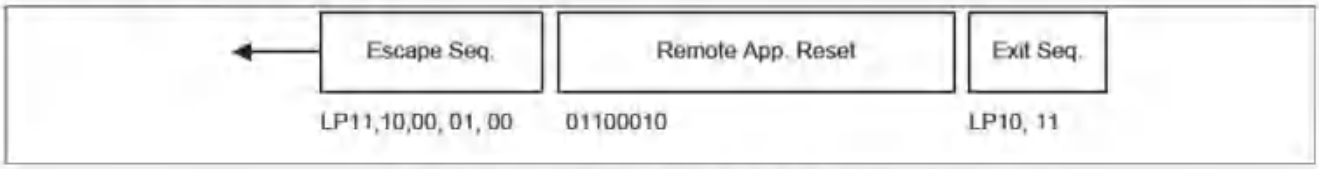

Figure 12-4 **Remote Application Reset Packet**

Figure 12-4 shows MIPI remote application reset packet using LP mode. The host processor can send software reset trigger by Remote Application Reset Packet

12-2-10. Remote Application Reset

A Command Mode display module has its own timings controller and local frame buffer for display refresh. In some cases the host processor needs to be notified of timing events on the display module, e.g. the start of vertical blanking or similar timing information. In a traditional parallel-bus interface like DBI-2, a dedicated signal wire labeled TE (Tearing Effect) is provided to convey such timing information to the host processor. In a DSI system, the same information, with reasonably low latency, shall be transmitted from the display module to the host processor when requested, using the bi-directional Data Lane.

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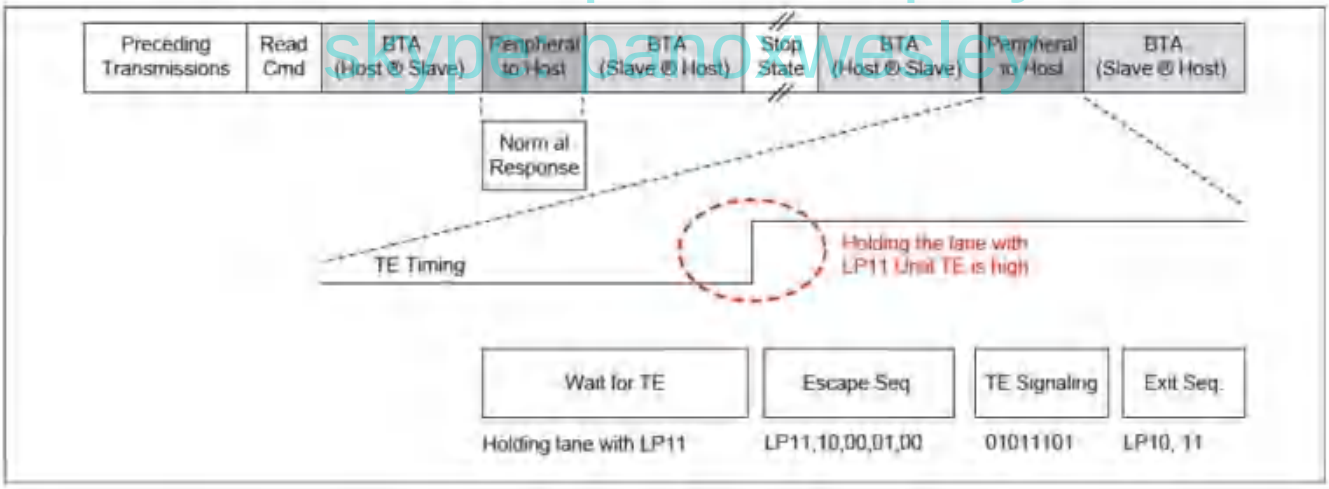

Figure 3-10 BTA Mode - TE Signaling

The PHY for DSI has no inherent interrupt capability from peripheral to host processor so the host processor shall give bus ownership to the peripheral for extended periods, as it does not know when the peripheral will send the TE message.

Since the timing of a TE event is, by definition, unknown to the host processor, the host processor shall give bus possession to the display module and then wait up to one video frame period for the TE response. During this time, the host processor cannot send new commands, or request to the display module, because it does not have bus possession. *Figure 12-5* shows the TE signaling Response procedure.

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The TE Signaling function is enabled and disabled by three DCS commands to the display module's controller: set_tear_on, set_tear_off. After sending set_tear_on to enable this function, the host processor ends the transmission with BTA asserted, giving bus possession to the display module. Since the display module's DSI protocol layer does not interpret DCS commands, but only passes them through to the display controller, it responds with normal Acknowledge and returns bus possession to the host processor. In this state, the display module cannot report TE events to the host processor since it does not have bus possession. To enable TE Reporting, the host processor shall give bus possession to the display module without an accompanying DSI command transmission after TE Signaling has been enabled. This is accomplished by the host processor's protocol logic asserting (internal) BTA signal to its PHY functional block. The PHY layer will then initiate a BTA sequence in LP mode, which gives bus possession to the display module.

Caution: When a state of the display module is in sleep in mode or the TE mode is turned off, the acknowledge Trigger instead of the TE Trigger is responded

12-2-11. Bi-Directional Data Lane Turnaround

The transmission direction of a bi-directional Data Lane can be swapped by means of a Link Turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from Forward-to-Reverse direction or Reverse-to-Forward direction. *Figure 3-11* shows the BTA procedure graphically.

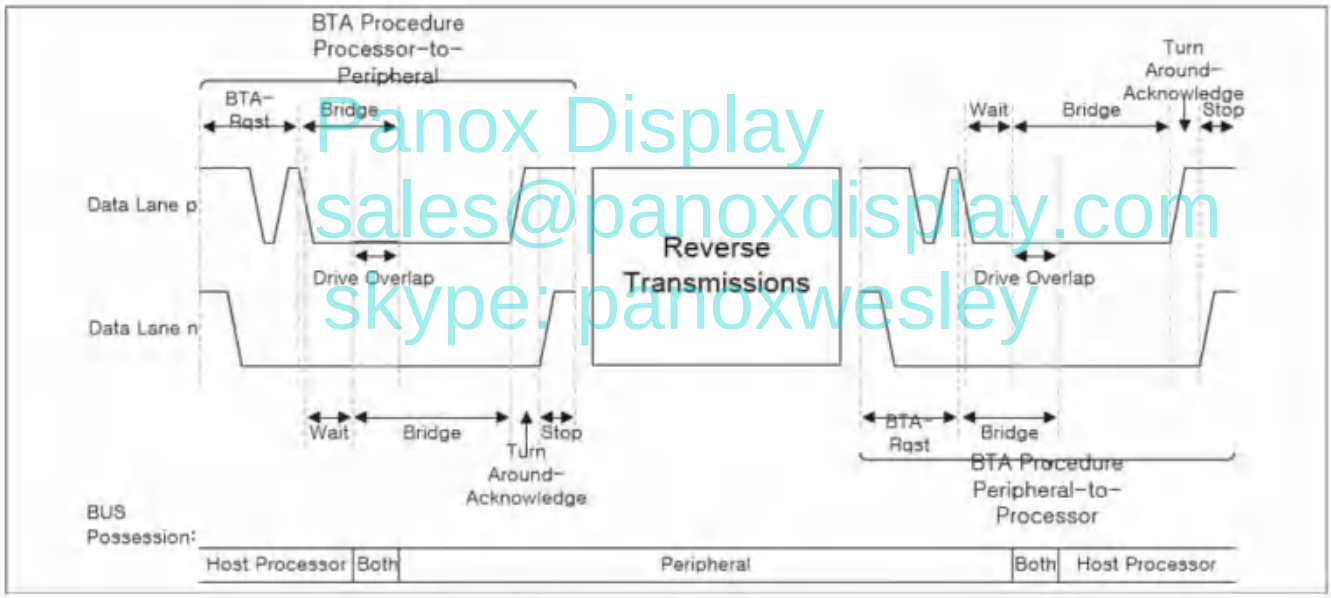

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Figure 3-11 Bus Turn Around Mode

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The low power clock timing for both sides of the Link does not have to be the same, but may differ. However, the ratio between the Low Power State Periods, T_{LPX} is constrained to ensure proper Turnaround behavior. The T_{LPX} (master)/ T_{LPX} (slave) shall be between 2/3 (0.667) and 3/2 (1.50). The handshake process for BTA allows only limited mismatch of Escape Mode clock frequencies between a host processor and a peripheral.

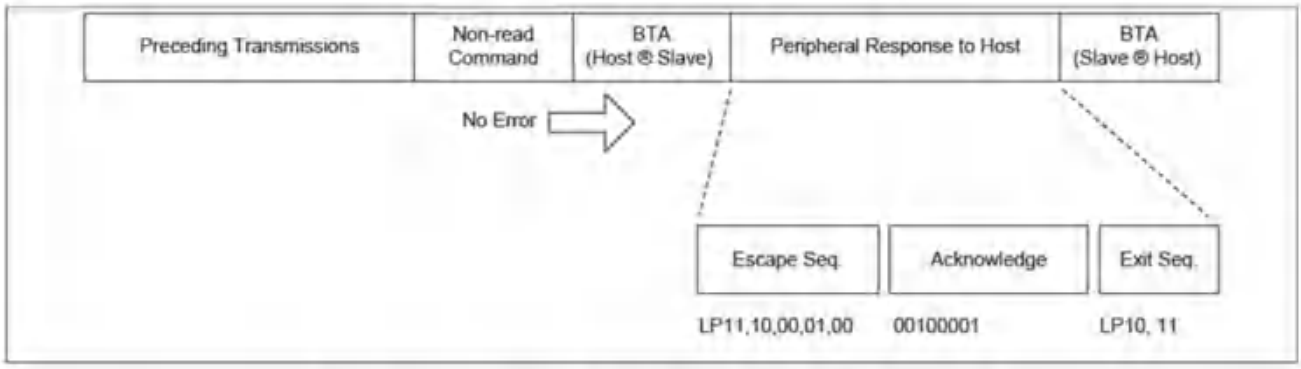

Figure 12-7 **BTA Mode - no error after non-read command**

Figure 12-7 shows an example of BTA after non-read command. The SLAVE get the lane controllability by BTA procedure to send the acknowledge packet on the successful data reception.

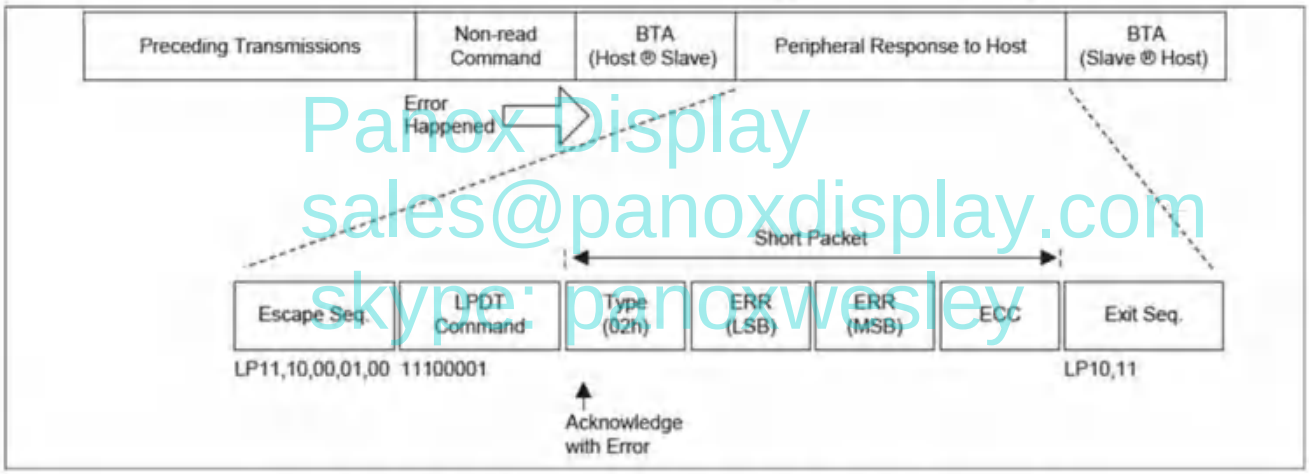

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Figure 12-8 **BTA Mode-Error Happened After Non-read Command**

Figure 3-13 shows an example of BTA after non-read command. The SLAVE gets the lane controllability by BTA procedure to send the acknowledge with error packet on the data reception error.

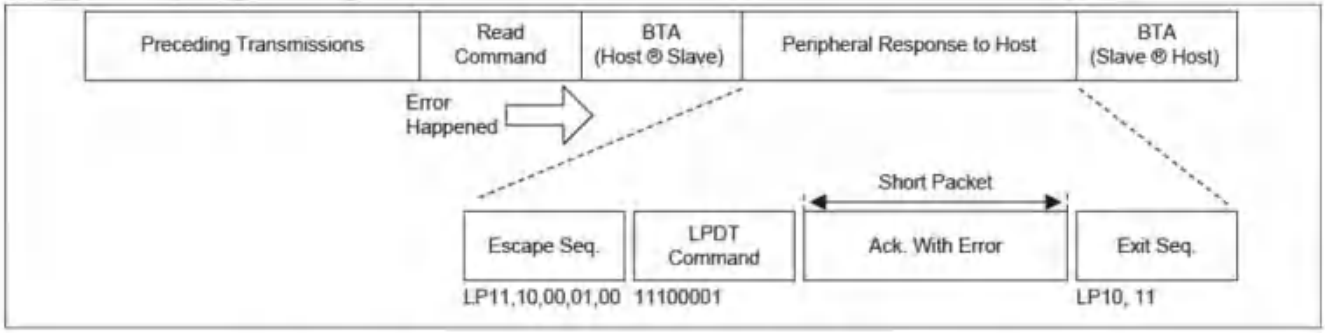

Figure 12-9 **BTA Mode-Error Happened After Read Command**

Figure 12-9 shows an example of BTA after-read command. The SLAVE gets the lane controllability by BTA procedure to send the acknowledge with error packet on the data reception error.

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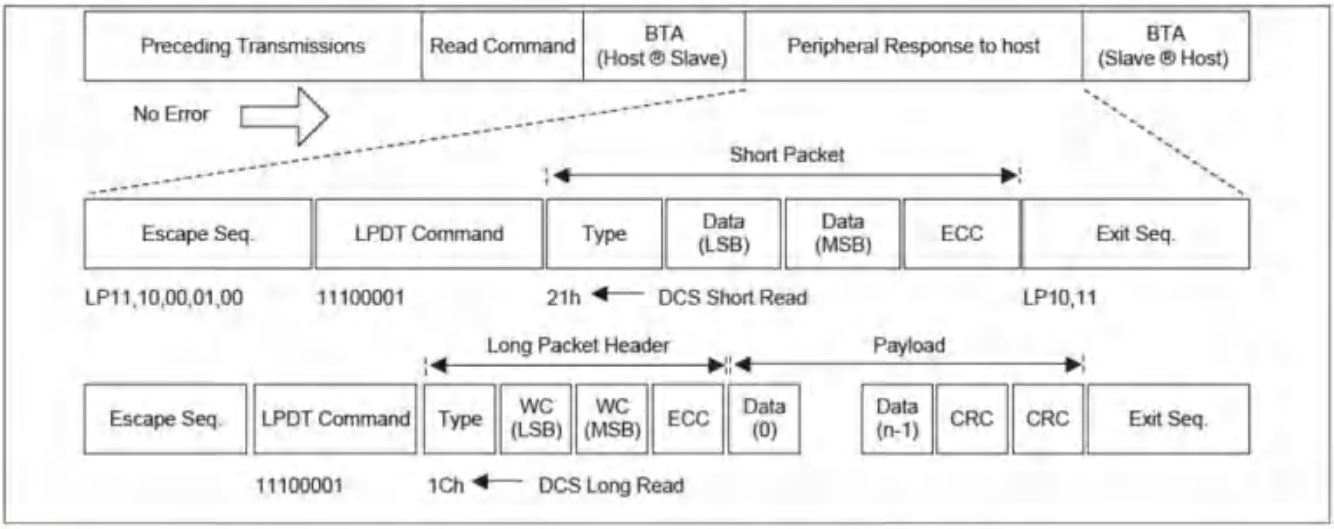

Figure 12-10 **BTA Mode-No Error After Read Command**

Figure 12-10 shows an example of BTA after read command. The SLAVE gets the lane controllability by BTA procedure to send readed data packet on the successful data reception.

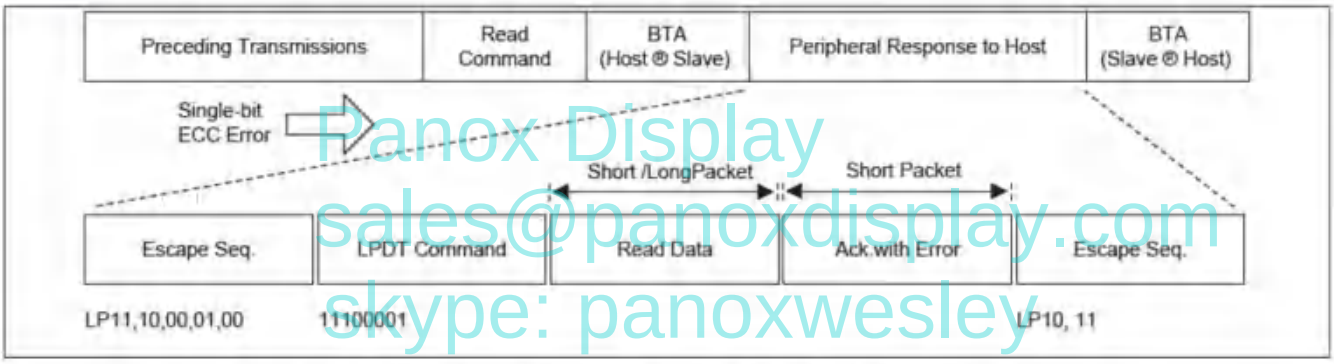

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Figure 12-11 **BTA Mode-One Bit Error After Read Command**

Figure 12-11 shows an example of BTA after read command. The SLAVE gets the lane controllability by BTA procedure to send readed data packet and acknowledge with error on the one bit error.

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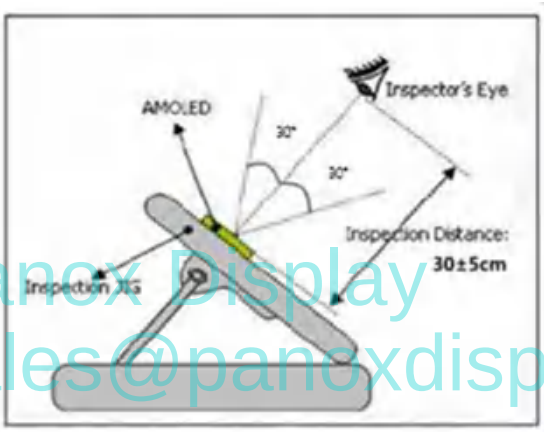
13. Quality Level

13-1. Environmental conditions

Item	Test Condition
Ambient light intensity	Function :0~200 Lux / Appearance : 800~1200 Lux
Viewing angle(tolerance)	90° ± 30°(Up/Down/Left/Right) ---------- note1
Viewing Distance	30 ± 5cm ---------- note1
Temperature	22 ± 3℃
Humidity	65 ± 20%RH
Light source	D65, Fluorescent lamp

[note1] : Viewing angle and distance



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13-2. Sampling Plan for each item's acceptance table

Defect type	Sampling Procedures	AQL
Major Defect	MIL-STD-105D Inspection level Ⅰ normal inspection single sample inspection	0.65
Minor Defect	MIL-STD-105D Inspection level Ⅰ normal inspection single sample inspection	1.0

① Major defect

: A major defect refers to a defect which may substantially degrade usability for product applications.

② Minor defect

: A minor defects refers to a defect which is not considered to substantially degrade product application, or a defect which deviates from existing standards almost unrelated to the effective use of the product or its operation.

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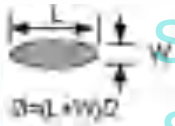
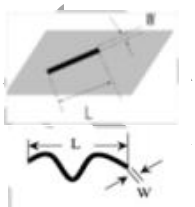
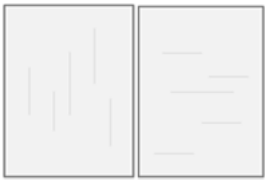
13-3. Function Inspection

: The following defect items are inspected with a display on.

<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>1</td><td>No display</td><td>Not allowable</td><td>Major</td></tr>
<tr><td>2</td><td>Abnormal display</td><td>Not allowable</td><td>Major</td></tr>
<tr><td>3</td><td>Line Defect</td><td>Not allowable
(Vertical line/ Horizontal line)</td><td>Major</td></tr>
<tr><td>4</td><td>Dot Defect
(Bright Dot,
Dark Dot)</td><td>
<table>
<tr><th>Defect</th><th>Acceptable number</th></tr>
<tr><td>Bright dot</td><td>0</td></tr>
<tr><td>Dark dot</td><td>4</td></tr>
</table>
distance between each dot: > 5mm
* Bright dot
Judgment condition : Black pattern & 35G white patt
* Dark dot : dot of 0% brightness
Judgment condition : 255G white & R/G/B pattern
</td><td></td></tr>
<tr><td>5</td><td>Foreign Material
Circular type
  </td><td>
<table>
<tr><th>Size (mm)</th><th>Acceptable number</th></tr>
<tr><td>Ø ≤ 0.1</td><td>Ignore</td></tr>
<tr><td>0.10 <</td><td>0</td></tr>
</table>
If the foreign material is removed with a soft cloth, it is allowable
Inspection performed in quality area
</td><td>Minor</td></tr>
<tr><td>6</td><td>Foreign Material
Linear type
  </td><td>
<table>
<tr><th>Width (㎜)</th><th>Length (㎜)</th><th>Acceptable number</th></tr>
<tr><td>0.02</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td rowspan="2">0.02 < W ≤ 0.04</td><td>L ≤ 2.0</td><td>Ignore</td></tr>
<tr><td>2.0 < L ≤ 5.0</td><td>2</td></tr>
<tr><td rowspan="2">0.04 < W ≤ 0.08</td><td>L ≤ 2.0</td><td>1</td></tr>
<tr><td>2.0 < L</td><td>0</td></tr>
<tr><td>0.08 < W</td><td colspan="2">considered as spot particle</td></tr>
</table>
※ If the foreign material is removed with a soft cloth, it is allowable.
</td><td>Minor</td></tr>
<tr><td>7</td><td>ELA Stain
  </td><td>Follow the SDC internal standard.
(Judgment condition : 87Gray)</td><td>Minor</td></tr>
</table>

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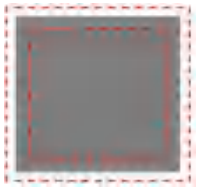
8	Uneven color stain 	Follow the SDC internal standard. (Judgment condition : 87Gray)	Minor
9	Random Mura	Follow the SDC internal standard. (Judgment condition : 87Gray)	Minor
10	WAD	Ignore ------- Note 1	Minor

[Note 1] WAD (White Angular Dependency)

: Luminance and color coordination variation according to viewing angle in full white pattern

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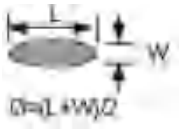
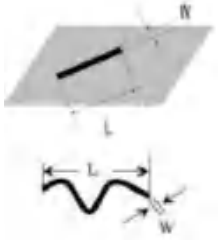
13-4. Appearance Inspection

: The following defect items are inspected with a display off.

<table>
<tr><th>No.</th><th>Item</th><th>Criterion of Defect</th><th>Type</th></tr>
<tr><td>1</td><td>Foreign Material
Circular type
 
</td><td>
<table>
<tr><th>Size Ø (mm)</th><th>Acceptable number</th></tr>
<tr><td>Ø ≤ 0.1</td><td>Ignore</td></tr>
<tr><td>0.10 < Ø</td><td>0</td></tr>
</table>
※ If the foreign material is removed with a soft cloth, it is allowable.
</td><td>Minor</td></tr>
<tr><td>2</td><td>Foreign Material/Scratch
Linear type
 
</td><td>
<table>
<tr><th>Width (㎜)</th><th>Length (㎜)</th><th>Acceptable number</th></tr>
<tr><td>W ≤ 0.02</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td rowspan="2">0.02 < W ≤ 0.04</td><td>L ≤ 2.0</td><td>Ignore</td></tr>
<tr><td>2.0 < L ≤ 5.0</td><td>2</td></tr>
<tr><td rowspan="2">0.04 < W ≤ 0.08</td><td>L ≤ 2.0</td><td>1</td></tr>
<tr><td>2.0 < L</td><td>0</td></tr>
<tr><td>0.08 < W</td><td colspan="2">Foreign Material : considered as spot particle
Scratch : Refer to Dent/Bubble Spec.</td></tr>
</table>
※ If the foreign material is removed with a soft cloth, it is allowable.
</td><td>Minor</td></tr>
<tr><td>3</td><td>Dent</td><td>
<table>
<tr><th>Size Ø (mm)</th><th>Acceptable number</th></tr>
<tr><td>Ø ≤ 0.10</td><td>Ignore (DS>5mm)</td></tr>
<tr><td>0.10 < Ø ≤ 0.20</td><td>2 (DS>5mm)</td></tr>
<tr><td>0.20 < Ø</td><td>0</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>4</td><td>Bubble</td><td>
<table>
<tr><th>Size Ø (mm)</th><th>Acceptable number</th></tr>
<tr><td>Ø ≤ 0.1</td><td>Ignore</td></tr>
<tr><td>0.10 < Ø ≤ 0.2</td><td>2</td></tr>
<tr><td>0.2 < Ø</td><td>0</td></tr>
</table>
- Ignore if cleaned by soft cloth .
- Ignore the bubble between glass and protection film.
</td><td>Minor</td></tr>
<tr><td>5</td><td>Cover-IC Tape
/Tuffy</td><td>IC cover tape and tuffy shall not overlap the active area and can cover encap glass. IC cover tape shall cover fully D-IC.</td><td>Minor</td></tr>
</table>

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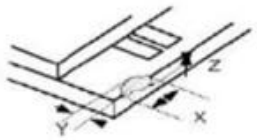
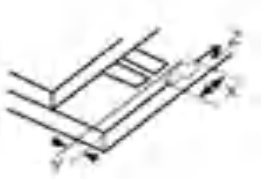
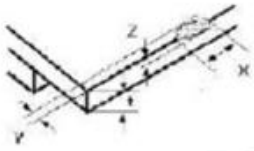
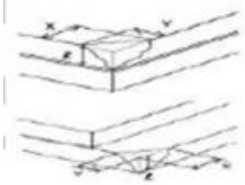
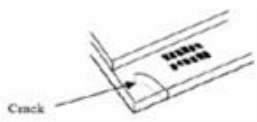
6	Panel PAD Chipping (No pattern area)	 Z ≤ t; X ≤ 5.0mm; Y ≤ 0.6mm	Minor
7	Panel PAD Chipping (pattern area)	 Z ≤ t; X ≤ 5.0mm; Y 0.6mm	Minor
8	Panel PAD Chipping (PAD rear side)	 Z ≤ t; X ≤ 5.0mm; Y ≤ 0.6mm	Minor
9	Panel Chipping (No pad area)	 Z ≤ t; X ≤ 5.0mm; Y ≤ 0.6mm	Minor
10	Panel Chipping (Corners)	 Z ≤ t; X ≤ 1.0mm; Y ≤ 1.0mm; a No pad area Z ≤ t; X ≤ 2.0mm; Y ≤ 1.2mm; a Pad area	Minor
11	Panel Crack	 Not allowable	Minor

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12	Surface Contamination	Ignore if defect is cleaned by soft cloth .	Minor
13	Cushion/Back Tape (Bubble, Dent, lifting, Scratch, Wrinkle, etc.)	Ignore if defect is not visible at the viewing area of front side.	Minor
14	ETC	Ignore if defects that are not listed in Standard Spec is not seen at operating condition	Minor

14. Reliability

No	Item		Condition	Qt'y	Remark
1	High Temperature Operating Life test		70℃, 120hr	5	
2	Low Temperature Operating Life test		-20 , 120hr	5	
3	High Temperature High Humidity Operating Life test		60℃/93%RH, 120hr	5	
4	High Temperature Storage test		75℃, 120hr	5	
5	Low Temperature Storage test		-30℃, 120hr	5	
6	High Temperature High Humidity Storage test		60℃/ 93%RH, 120hr	5	
7	Thermal Cycle Storage test		-30℃ ~ 70℃, 50 Cycles	5	
8	Electrical Static Discharge	Contact	±4kV(1Center, 4Corner), 150pF/330Ω	5	
		Air	±6kV(1Center, 4Corner), 150pF/330Ω	5	
9	Box Vibration / Drop		Random Vibration (6~200Hz, 1.047Grms, 1hr/XYZ axis) 1 corner, 3 Edges, 6 Surfaces	1box	

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15. Handling Precautions

15-1. Mounting Method

The AMOLED panel of SAMSUNG Display CO.,LTD. module consists of two slim glasses which can easily get damaged. Extreme care should be used when handling the AMOLED modules.

15-2. Caution of AMOLED Handling and Cleaning

When cleaning the display surface, use soft cloth solvent as recommended below and wipe gently.

◎ Isopropyl alcohol
◎ Ethyl alcohol
◎ Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the glass surface.
Do not use the following solvent.

◎ Water
◎ Ketone
◎ Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns.
Do not use the following solvent on the pad and prevent it from being contaminated.

◎ HCFC (Other area except ITO pad can use the HCFC for cleaning process)
◎ Soldering flux
◎ Chlorine(Cl), Sulfur(S)
◎ Spittle, Fingerprint

If the product is not wrapped with a desiccant added pad, ITO pattern can be damaged by corrosion. SAMSUNG Display CO,.LDT. suggests wrapping a product with a desiccant unless customers particularly indicate that they do not want it. In case ITO pattern corrodes due to the usage of chlorine, sulfur or customer's mishandling of the product, the responsibility lies with the customer.

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15-3. Caution Against Static Charge

For AMOLED module, use C-MOS LSI drivers, therefore we recommend that you ;
Connect any unused input terminal to VCI or VSS, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity. It could occur static electricity when taping off the film which protects AMOLED.
Against static charge, you should make sure that the product is safe or not by experiment in

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15-4. Packing

◎ The packing principle is that AMOLED module should keep its packing condition at the time of delivery.

◎ For safety & avoiding the module damage, Carton box must stack the below 4 boxes. When storing the AMOLED after unpacking, note the followings.

◎ AMOLED module is consisted of GLASS and assemblies. It should avoid pressure, strong impact, and being dropped from a height.

◎ To prevent modules from degradation, do not operate or store them in a place where they are directly exposed to sunlight or high temperature/humidity.

15-5. Caution for Operation

◎ If you do not follow normal POWER ON , OFF sequence or abnormal operating, then AMOLED module can be damaged electro-optically and does no
Do not change software without Samsung Display conf

◎ Response time may extremely delay at a temperature lower than operating range, AMOLED does not normally operate at a high temperature. But this may recover at a proper temperature.

◎ When you set optimal operating voltage to AMOLED module, you can see the optimal contrast of AMOLED. So, add voltage controllable function at

◎ AMOLED module may not display normally when twisting power or pressing power is added. Therefore you should secure AMOLED module maximum thickness at set assembly not to have any pressure affect AMOLED module.

◎ Electro-chemical reaction may occur when there is humidity on pad, therefore, you should use AMOLED Module below maximum operating humidity.

◎ AMOLED Module Power Vdd should be designed to protect surge current at SET Module.

◎ You should not damage connector and cable for AMOLED module assembly by force folding or by applying extreme power.

◎ AMOLED may not display normally when it is interfered by surrounding elements, therefore you should consider setting design not to damage AMOLED module by surrounding elements.

◎ To satisfy EMI standards, you should plan your design after considering emitting energy.

◎ We can not guarantee display characteristics outside viewing area, therefore your set window should be fixed into viewing area.

◎ Image-sticking may occur if AMOLED displays same image for a long time, so you need to make a change for AMOLED.

◎ When remove the glass protective film, Necessarily need to apply as a way to prevent Cushion and conductive tape delamination.

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15-6. Storage

◎ Place in a dark place where neither exposure to direct sunlight or any fluorescent light is permitted and keep at room temperature & room humidity.

◎ Store with no contact with glass surface.
[It is recommended to store them as they have been contained in the inner container when we delivered them.]

15-7. Safety Precautions

◎ Disassembly or modification may cause electric shock, damages to sensitive part inside of the AMOLED module, dust adhesion, or scratches on the display part.

◎ In the event that the contents of AMOLED module are on skin, wipe them with a paper towel or gauge and wash the part well, and receive medical attention if necessary.

◎ Do not use the AMOLED module for the special purpose besides display units.

◎ Be careful of the glass chips that may cause injury to fingers of skin, when the display part is broken.

◎ For keeping safe quality from outer exposure or contamination, modules should be consumed within 2 months after unpacking.

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15-8. Precautions before Use

You should discuss the following case with SAMSUNG

◎ in case of any questions about contents of this "Specification For Approval".

◎ in case of occurring new problems not mentioned at this "Specification For Approval".

◎ in case of your request about income inspection specification change.

◎ in case of occurring new problem at your driving test.

※ If SAMSUNG Display CO., LTD has to change the conditions specified in the specification, previously the negotiation shall be held and decided.

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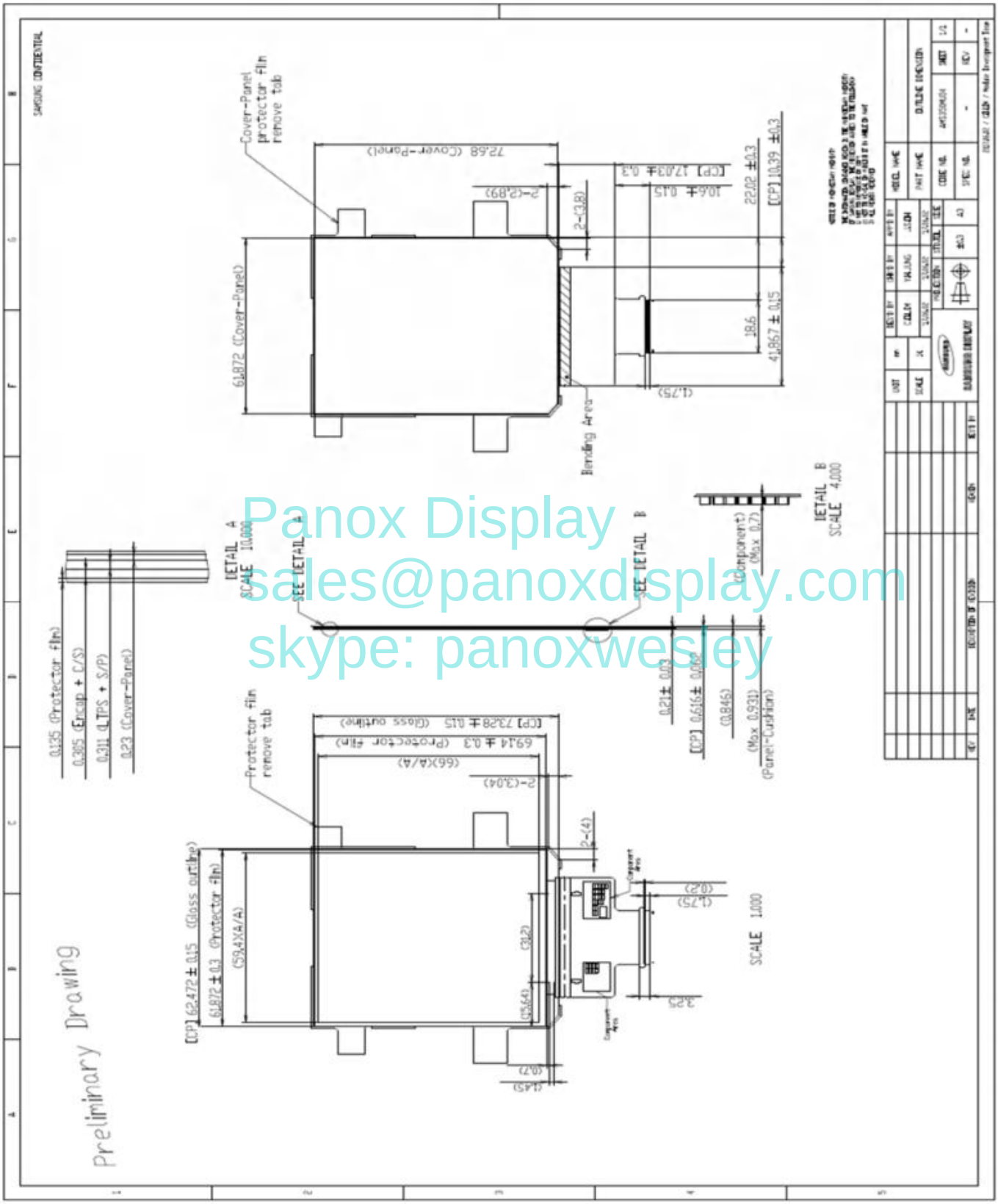
16. Drawings

16-1. Product Drawing



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16-2. MAIN FPC SCHEMATIC

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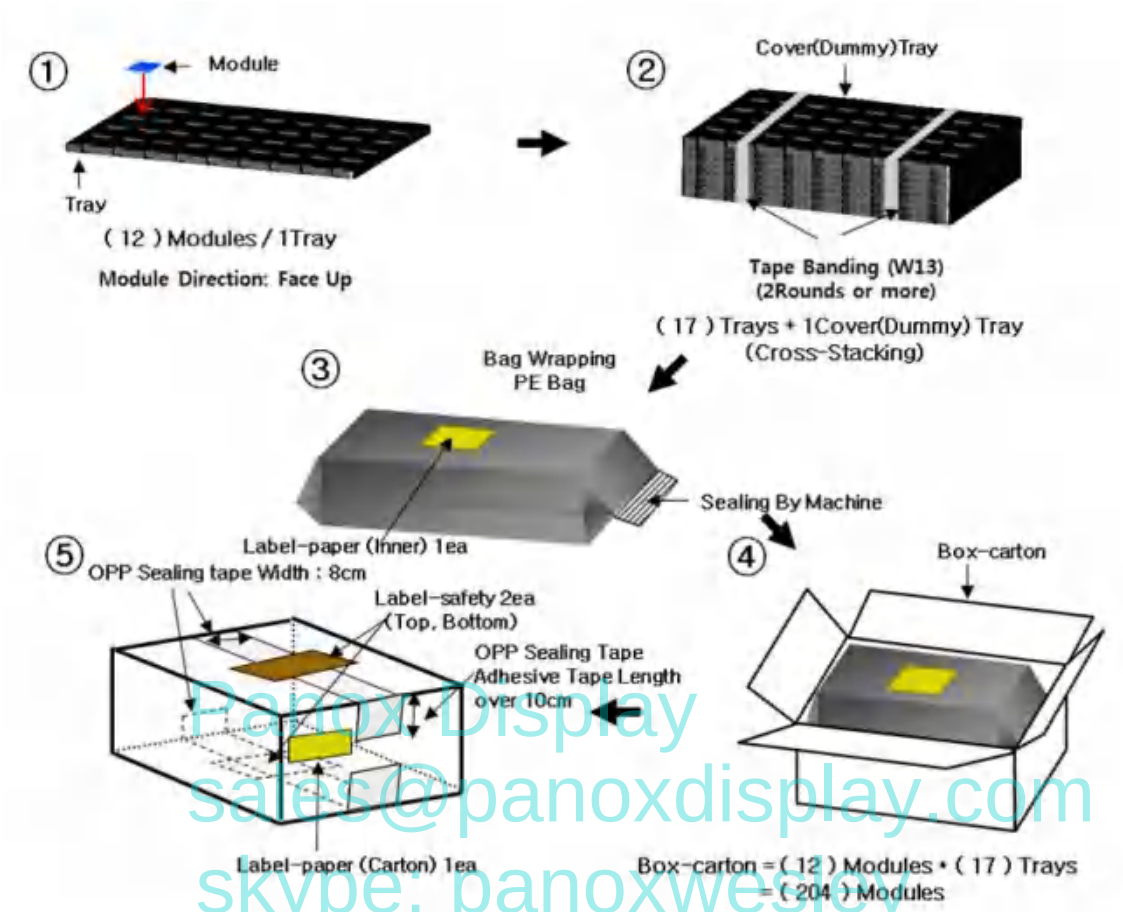
17. Packing Specification

17.1 Box Pack



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Note

(1) Total :Box-carton approx. : Max (13)kg

(2) Size : 583(L) x 388(W) x 210(H)

(3) Place the Module in the tray facing the active area direction.

(4) Stack the trays and cover (dummy) tray.

(5) Resistance of tray surface : 1x105 ~ 1x1 Ω

* Measure Point (Ref. Tray Drawing)

Top direction : In pocket, area of placed Module)

Bottom direction : In pocket, The nearest “11” shape Stopper with Module)

(6) Triboelectric Charge of tray surface : Max 100V

* Measure Point In Pocket (Top / Bottom) , 2kgf over 10 times with Clean Wiper

* Measurement condition : 22±3℃/50±5%, measure on antistatic mats)

(7) Wrap the PE bag by packing machine and affix the Label-Paper on Bag.

(8) Put the bag in the Box-carton .

(9) Seal the Box-carton and affix the Label-safety & Label-paper.

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TRAY Tape Banding (A TYPE TRAY)

(1) TRAY Tape Banding Position : 2nd and 7th groove

(2) The number of TAPE Banding : More than 2 times

[Tape position : 2nd groove] [Tape position : 7th groove]

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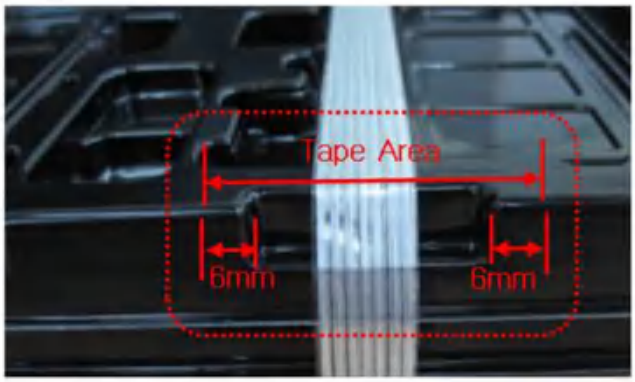

[Tape position]

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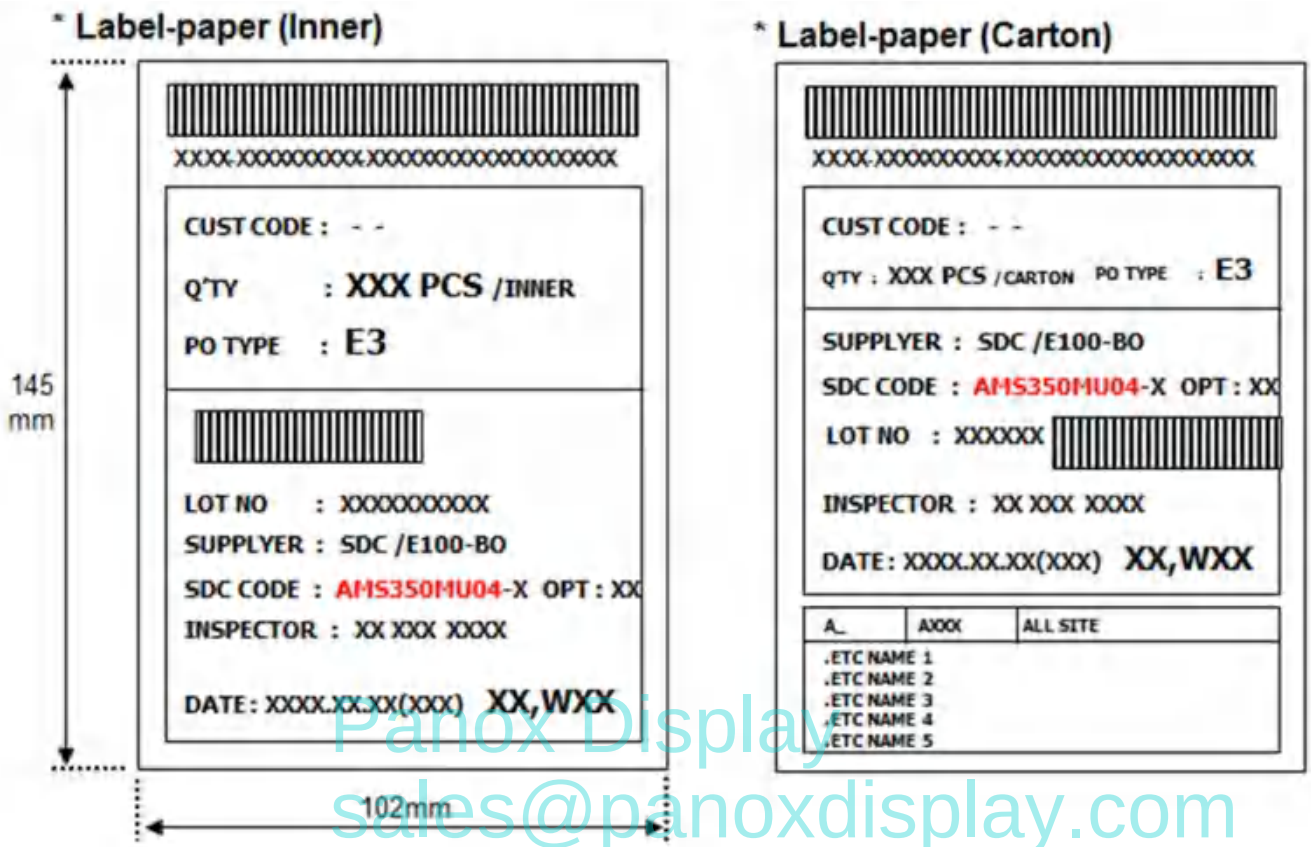
3054015046636O3

17.2 Label



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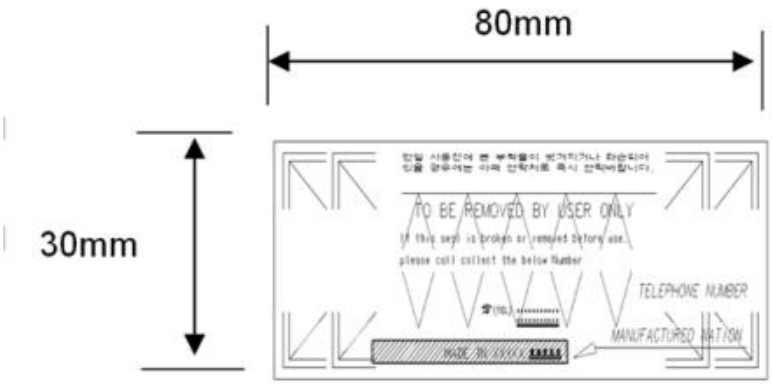
Label Safety



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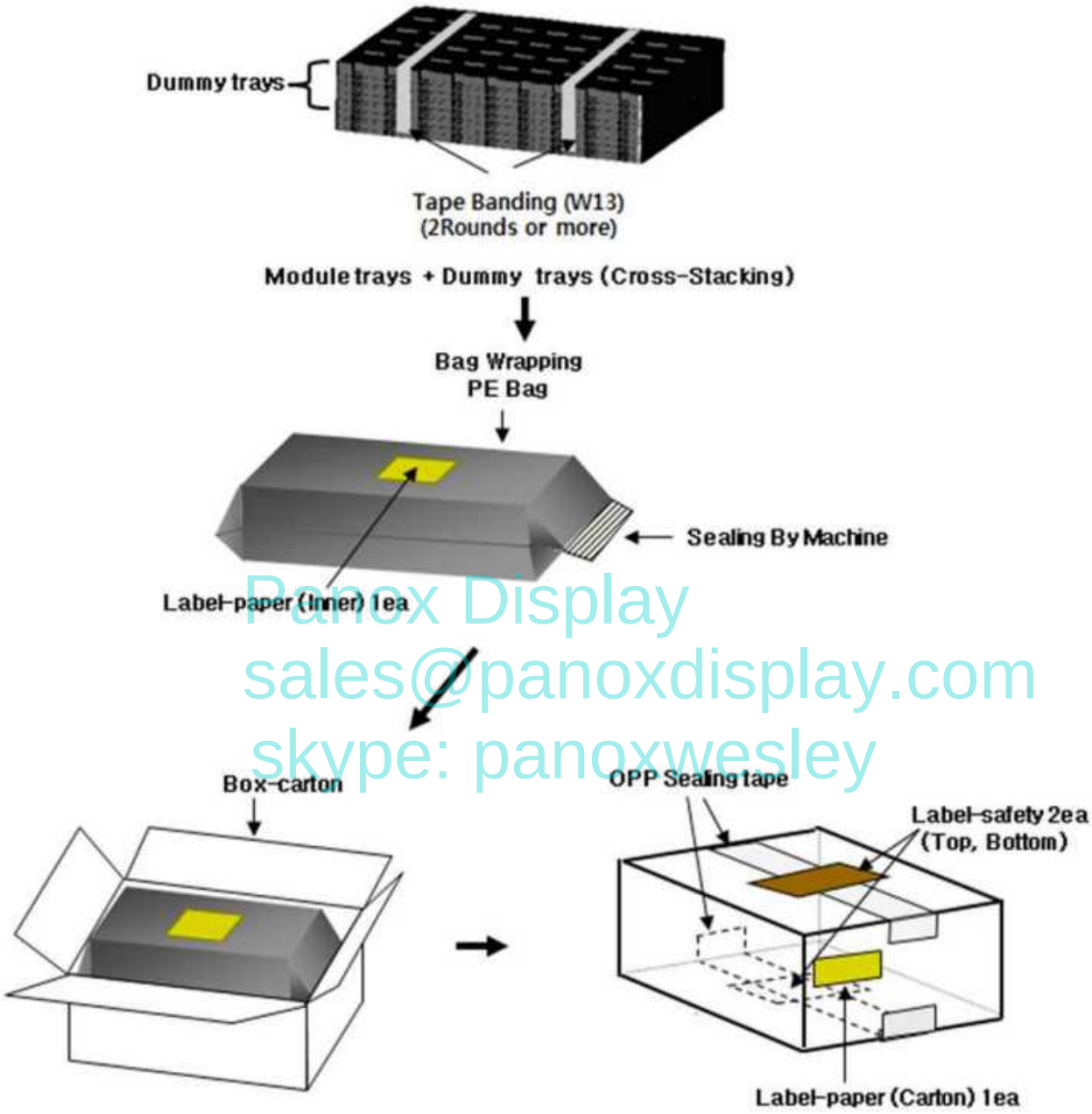
305401504663603

17.3 Packing for Small Quantities



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Note

When package quantity is small, Modules containing trays are stacked the bottom,
and dummy trays are stacked at the top of package,
then wrap the PE bag by packing machine and affix the Label-Paper on Bag.
Put the Bag in the Box-carton.
Seal the Box-carton and affix the Label-safety & Label-Paper.

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17.4 Over Pack

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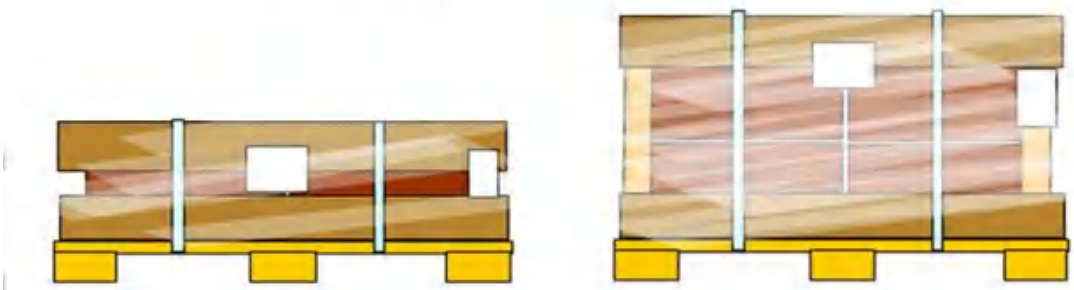
17.5 Packing for Small Quantities



1 step
[Carton Box : 1~4 Box]

2 step
[Carton Box : 5~8 Box]

-. Small Quantities (1step ,2 step) must stack on the Top.

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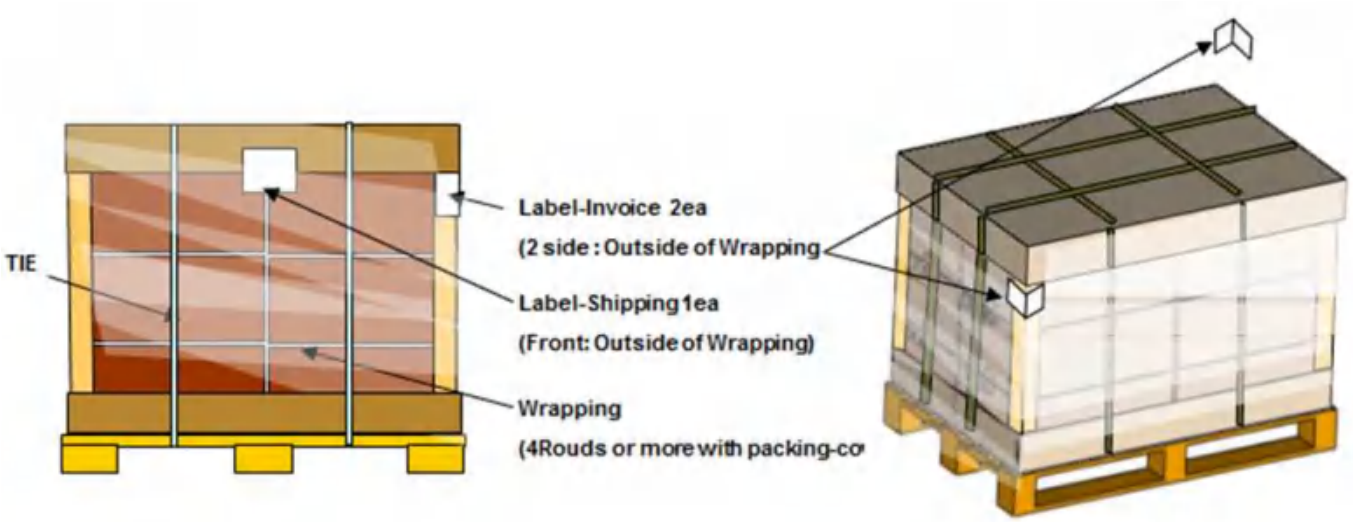
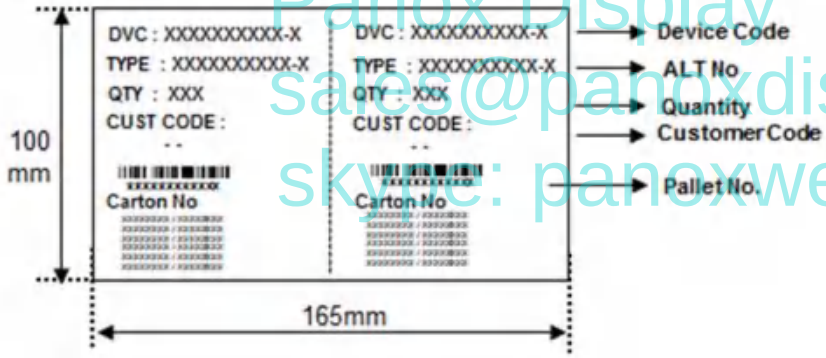
17.6 Over Pack Attach



* Label-invoice



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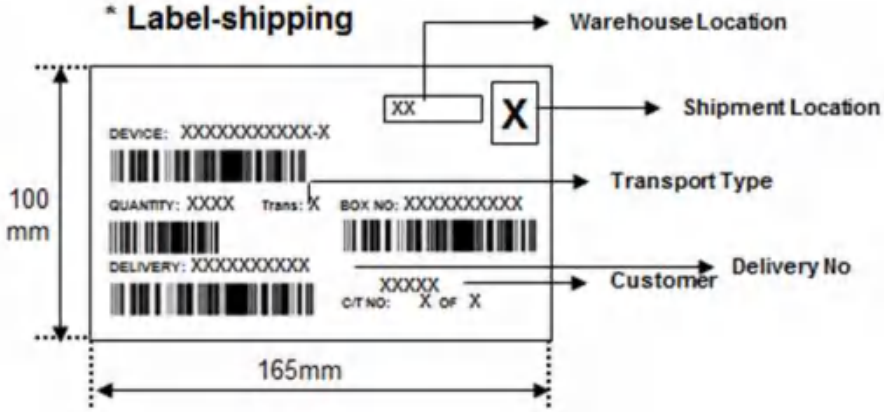
* Label-shipping



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*** Reference Image (Except Label and Wrap)**

Carton Box		
Pallet		

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Caution

For keeping safe quality from outer exposure of contamination, modules should be consumed within 2 months after unpacking