



MODEL NO. : TA068FJWK03-00

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- Preliminary Specification**
 Final Product Specification

Customer :

Approved by	Notes

SHANGHAI TIANMA Confirmed :

Prepared by	Checked by	Approved by
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This technical specification is subjected to change without notice

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Record of Revision

Rev	Issued Date	Description	Editor
1.0	2023-02-18	Preliminary Product Specification	Hui Wang

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1 General Specifications

Item	Specification	Unit
Substrate Thickness	0.15(TPF)+0.0412(panel)+0.088(BP)+0.06(BP 保护膜)	mm
Panel Outline Dimension	72.6768*166.574	mm
Size	6.78	Inch
Active Area	70.6968*157.104	mm
Resolution	1080*2400	pixel
Pixel Size	65.46*65.46	um
Pixel Configuration	Windmill	/
Viewing Direction	ALL	o'clock
Pixel Driving Element	LTPS	/
Suggested driver IC(LCD)	NT37705	
Display Mode	OLED	
Technology Type	TPOT	

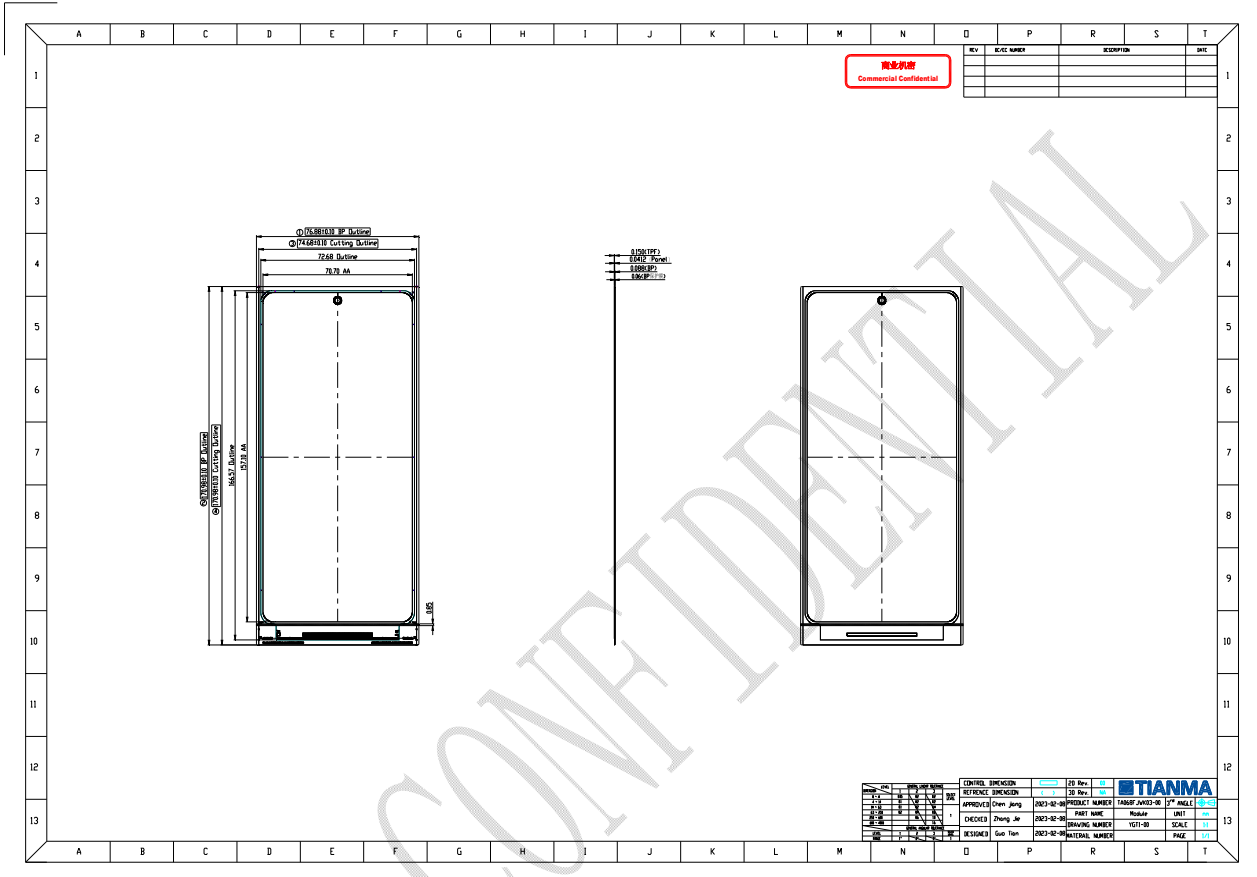
Note 1: Viewing direction for best image quality is different from TFT definition; there is a 180 degree shift.

Note 2: Requirements on Environmental Protection: RoHS+HF



2 Dimension

2.1 Outline Dimension





3 FPC PIN Assignment

3.1 COP Pin Definition (NT37705)


 panel 两侧FPC
 pin定义-202205101

4 Electrical Specification

(DDIC 若为 NT37705 , 数据仅供参考)

4.1 DC characteristics

Item	Symbol	Condition	Specification			Unit	
			Min.	Typ.	Max.		
Supply Voltage (Display)	Analog Voltage	VCI	Operation Voltage	2.8	3.0	3.2	V
	Logic Voltage	VDDI	I/O supply voltage	1.7	1.8	1.9	V
	Digital voltage	DVDDP	Operation Voltage	1.2	1.2	1.4	V
	Source Voltage	VLIN (AVDD)		7.2	7.2	7.6	V
	OLED positive voltage	ELVDD	500nit White	4.5	4.6	4.7	V
	OLED negative voltage	ELVSS	500nit White	-2.8	-2.5	-2.2	V
Supply Voltage (TSP)	Analog Voltage	TP_AVDD	Operation Voltage	2.8	3.0	3.6	V
	Logic Voltage	TP_DVDD	Operation Voltage	1.7	1.8	1.98	V

Note1: VDDI's current will be increase when DVDD's voltage is drop to 1.0V in DDIC, and DVDD's current would be decrease at the same time.so we define the max current as the sum of VDDI and DVDD.

Note2:The value of supply voltage is on BTB side.



4.2 MIPI Interface Characteristics

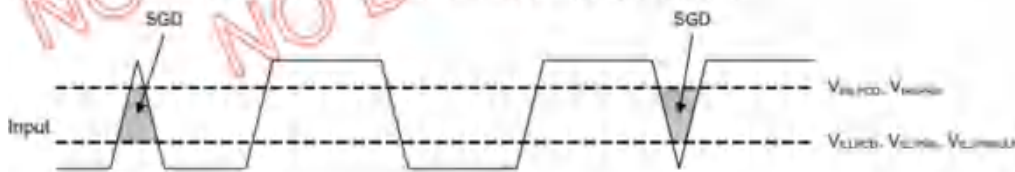
MIPI low-power characteristics

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	$V_{IH,LP,CD}$	LP-CD	450	-	1350	mV
Logic low level input voltage	$V_{LL,LP,CD}$	LP-CD	0	-	200	mV
Logic high level input voltage	$V_{IH,LP,RX}$	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	$V_{LL,LP,RX}$	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{LL,LP,RX,ULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	$V_{OH,LP,TX}$	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	$V_{OL,LP,TX}$	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μ A
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μ A
Input pulse rejection	SGD	DSI2-CLK+/-, DSI2-Dn+/- (Note 3)	-	-	300	Vps

Note 1) $V_{DD1}=1.65\sim 1.95V$, $DVSS=AVSS=AVSS_DC=VSSB=V_{G_HSSI}=0V$, $T_a=-30$ to $70^\circ C$ (to $+85^\circ C$ no damage).

Note 2) DSI2 high speed is off.

Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.



MIPI high-speed characteristics



Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	DSI2-CLK+/-, DSI2-Dn+/- (Note 2, 3)	70	-	330	mV
Input voltage common mode variation (\leq 450MHz)	V_{CMCLK} V_{CMDATA}	DSI2-CLK+/-, DSI2-Dn+/- (Note 4)	-50	-	-50	mV
Input voltage common mode variation (\geq 450MHz)	V_{CMCLKM} $V_{CMDATAM}$	DSI2-CLK+/-, DSI2-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V_{THCLK} V_{THDATA}	DSI2-CLK+/-, DSI2-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V_{THCLK} V_{THDATA}	DSI2-CLK+/-, DSI2-Dn+/-	-	-	70	mV
Single-ended input low voltage	V_{LHS}	DSI2-CLK+/-, DSI2-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V_{HHS}	DSI2-CLK+/-, DSI2-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI2-CLK+/-, DSI2-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI2-CLK+/-, DSI2-Dn+/-	-	-	450	mV
Termination capacitor	C_{TERM}	DSI2-CLK+/-, DSI2-Dn+/-	-	-	14	pF

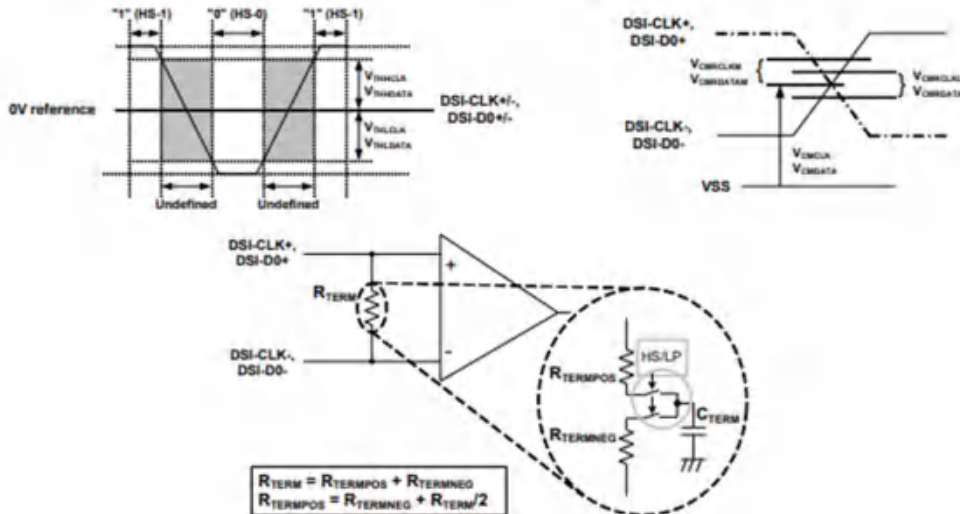
Note 1) $V_{DD1}=1.65\sim 1.95V$, $DVSS=AVSS=AVSS_DC=VSSB=VG_HSSI=0V$, $T_a=-30$ to $70^\circ C$ (to $+85^\circ C$ no damage).

Note 2) Includes 50mV (-50mV to 50mV) ground difference.

Note 3) Without V_{CMCLKM} / $V_{CMDATAM}$

Note 4) Without 50mV (-50mV to 50mV) ground difference.

Note 5) Dn=D0, D1, D2 and D3.



4.3 Reset Input Timing

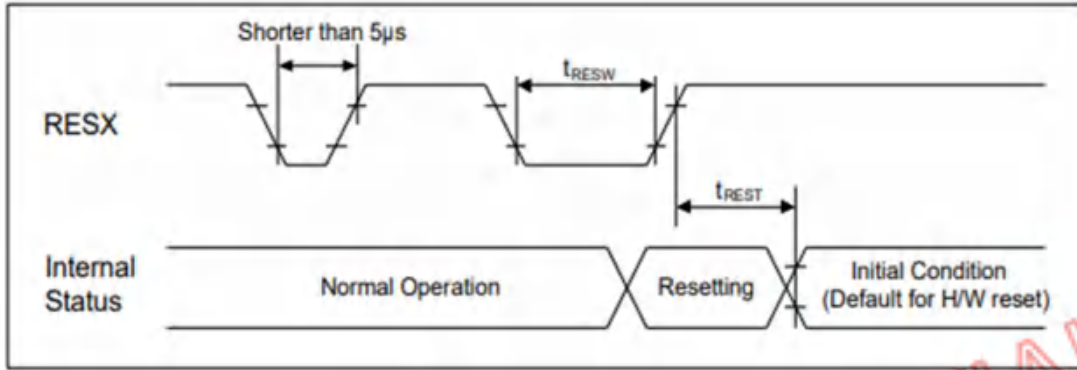


Figure MIPI reset Timing

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t_{RESW}	Reset *L* pulse width (Note 1)	30	-	-	μ s	
	t_{REST}	Reset complete time (Note 2)	-	-	10	ms	When reset applied during Sleep In Mode
					120	ms	When reset applied during Sleep Out Mode and Note 4

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μ s	Reset Rejected
Longer than 30 μ s	Reset
Between 5 μ s and 30 μ s	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In-mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

Table Data to Clock Timing Specifications

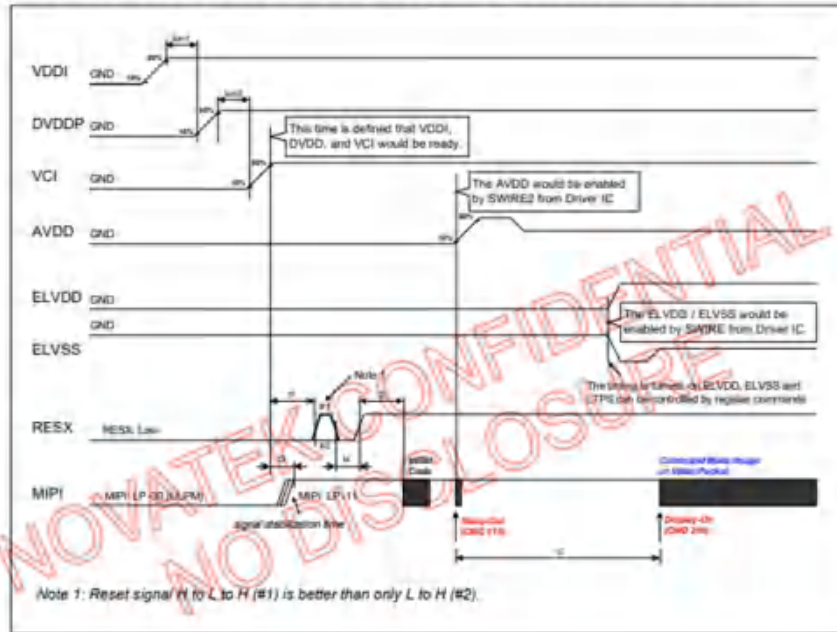


5 Power On/Off Sequence

Power on sequence(4 Power)

- 4 Input Power with independent DVDDP (EXT_DVDD_EN = '0')

VDDI=1.65~1.95V, DVDDP=1.2~1.95V, VCI=2.65~4.5V, AVDD_DC=AVDDB=AVDD=5.0~8.0V

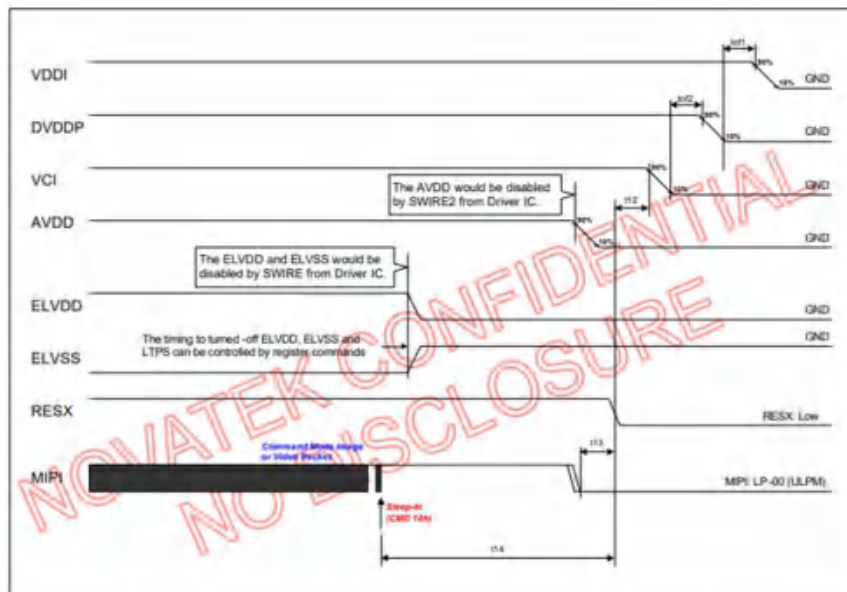


Power off sequence

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	0	-	-	ms	
ton2	0	-	-	ms	
t1	10	-	-	ms	
t2	20	-	-	ms	
t3	0	-	t1	ms	
t4	30	-	-	µs	
t5	120	-	-	ms	

-4 Input Power with independent DVDDP (EXT_DVDD_EN = '0')

VDDI=1.65~1.95V, DVDDP=1.2~1.95V, VCI=2.65~4.5V, AVDD_DC=AVDDB=AVDD=5.0~8.0V



Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
tof1	0	-	-	ms	
tof2	0	-	-	ms	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	-	100	-	ms	

6 INTERFACE TIMING

6.1 High-Speed mode

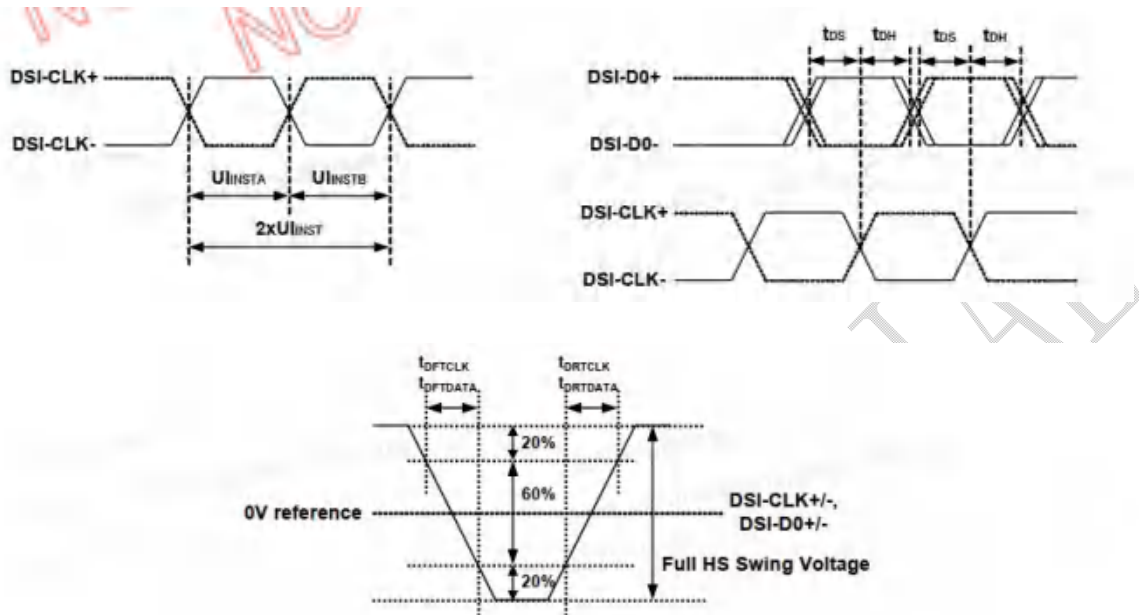


Figure High Speed timing

(DVSS=AVSS=AVSS_DC=VSSB=VG_HSSI=0V, VDDI=1.65V to 1.95V, Ta=-30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI2-CLK+/-	$2 \times UI_{INST}$	Double UI instantaneous	1.334	-	4	ns	4 Lane (Note 2)
DSI2-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halves (UI = UI_{INSTA} = UI_{INSTB})	0.667	-	2	ns	4 Lane (Note 2)
DSI2-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	Note 1, 3
			0.2xUI	-	-	ps	Note 1, 4
DSI2-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	Note 1, 3
			0.2xUI	-	-	ps	Note 1, 4
DSI2-CLK+/- DSI2-Dn+/-	t_{DFTCLK}	Differential rise time for clock	-	-	0.3xUI	ps	Note 1, 5
			-	-	0.35xUI	ps	Note 1, 6
			100			ps	Note 1, 7

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 1.5 Gbps.

Note 3) Total setup and hold window for receiver of $0.3 \times UI_{INST}$ when D-PHY is supporting maximum data rate = 1Gbps.

Note 4) Total setup and hold window for receiver of $0.4 \times UI_{INST}$ when D-PHY is supporting maximum data rate > 1Gbps.

Note 5) Applicable when operating at HS bit rates ≤ 1 Gbps (UI ≥ 1 ns).

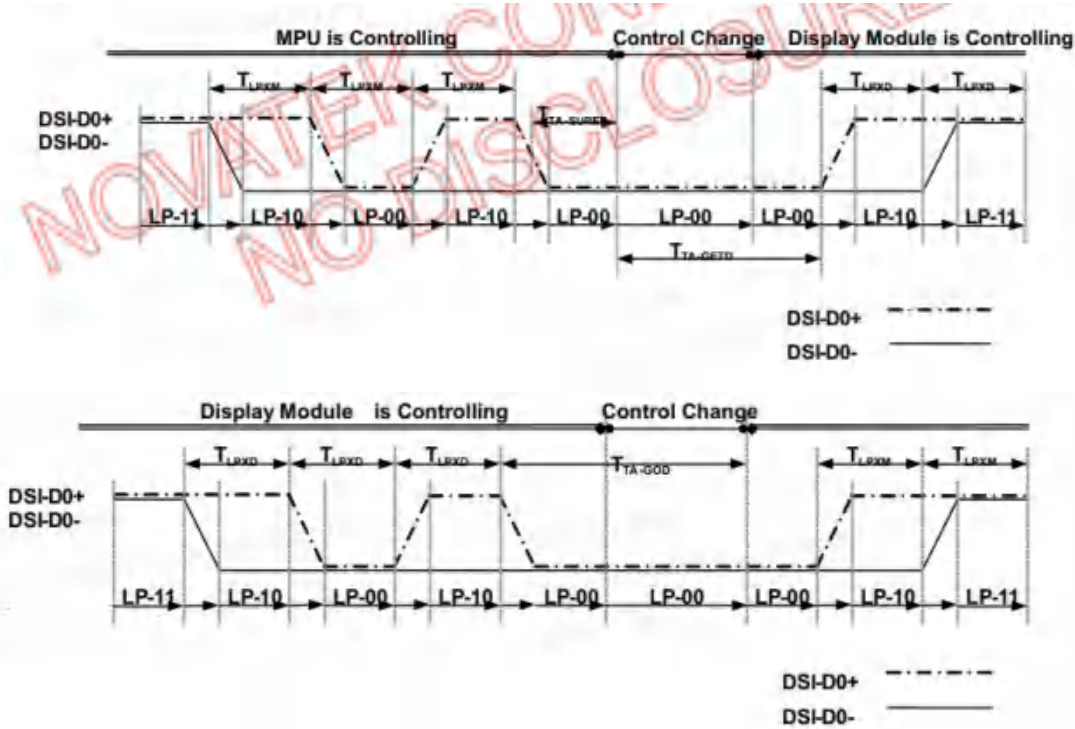
Note 6) Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).

Note 7) Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), should not use values below 150 ps.

Table High Speed mode

6.2 Low-Power Receiver

Input Glitch Rejection of Low Power Receivers as follow.



Figure

Low-Power timing

(DVSS=AVSS=AVSS_DC=VSSB=VG_HSSI=0V, VDDI=1.65V to 1.95V, Ta=-30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI2-D0+/-	T _{LRXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI2-D0+/-	T _{LRXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI2-D0+/-	T _{TA-GLITCH}	Time-out before the MPU start driving	T _{LRXD}	-	2xT _{LRXD}	ns	Output
DSI2-D0+/-	T _{TA-GETD}	Time to drive LP-00 by display module	-	5xT _{LRXD}	-	ns	Input
DSI2-D0+/-	T _{TA-GOOD}	Time to drive LP-00 after turnaround request - MPU	-	4xT _{LRXD}	-	ns	Output

Figure Low-Power mode



7 Optical Characteristics

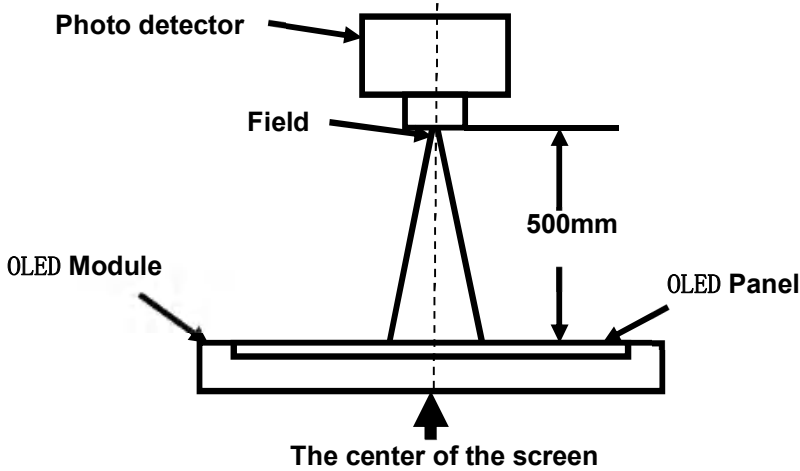
Item	Symbol	Condition	Min	Typ	Max	Unit	Remark
Contrast Ratio	CR	$\theta=0^\circ$	80000	-	-	-	Note1 Note2 TM module for reference
Response Time	T_{ON}	25°C	-	-	1	ms	Note1 Note3 TM module for reference
	T_{OFF}						
Chromaticity	Red	-	x	0.651	0.681	0.711	Note1 Note4 TM module for reference
			y	0.289	0.319	0.349	
	Green		x	0.204	0.244	0.284	
			y	0.679	0.719	0.759	
	Blue		x	0.109	0.139	0.169	
			y	0.014	0.044	0.074	
Uniformity(9 point)	U	-	75	-	-	%	Note1 Note5 TM module for reference
Crosstalk	Ct	-	-	-	2	%	Note6 TM module for reference
NTSC(CIE1931)	-	/	85	-	-	%	Note4 TM module for reference

Test Conditions:

1. The ambient temperature is 25°C.
2. The test systems refer to Note 1 and Note 2.

Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 minutes operation, the optical properties are measured at the center point of the OLED screen. All input terminals OLED panel must be ground when measuring the center area of the panel.



Item	Photo detector
Contrast Ratio	PR730
Chromaticity	
Lum Uniformity	DMS803
Response Time	

Fig. 1 Optical measurement system

Note 2: Definition of contrast ratio

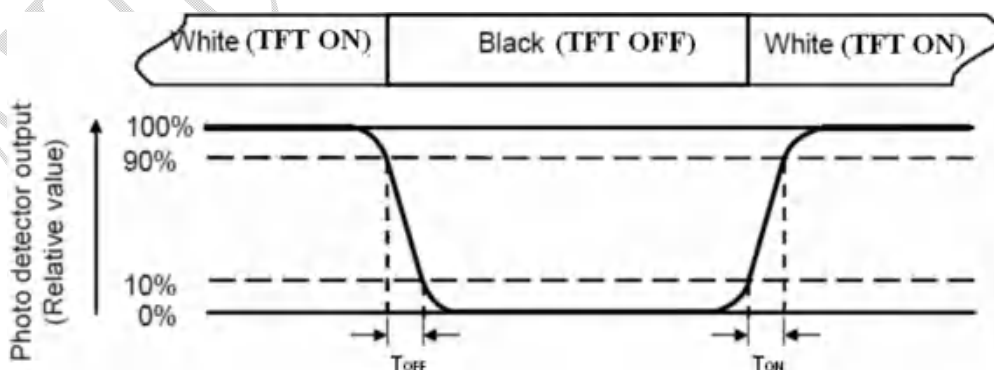
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when OLED is on the "White" state}}{\text{Luminance measured when OLED is on the "Black" state}}$$

“White state”: The state is that the OLED should be driven by V_{white} .

“Black state”: The state is that the OLED should be driven by V_{black} .

Note 3: Definition of Response time

The response time is defined as the OLED optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



to 90%.



Note 4: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of OLED.

Note 5: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 3). Every measuring point is placed at the center of each measuring area.

$$\text{Luminance Uniformity}(U) = L_{\min} / L_{\max}$$

L-----Active area length W----- Active area width

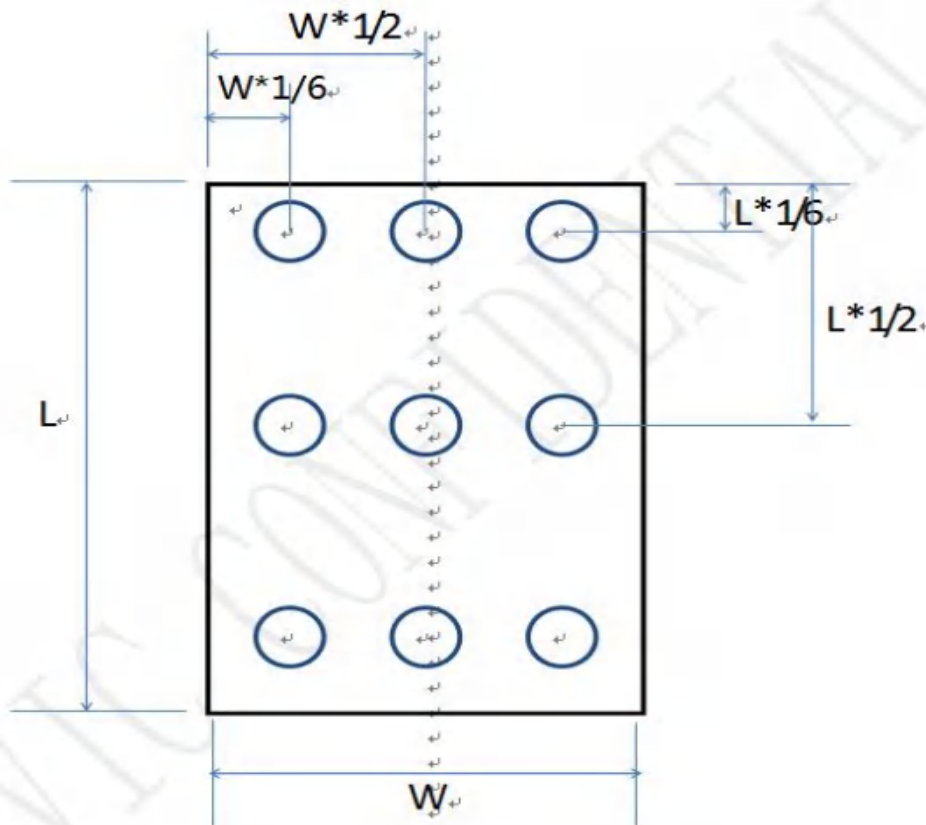


Fig. 2 Definition of uniformity

L_{\max} : The measured maximum luminance of all measurement position.

L_{\min} : The measured minimum luminance of all measurement position.


Note 6: Definition of Crosstalk :

- There should be no visible cross-talk in normal direction of the display when the two "Cross-talk Test Patterns " below are loaded.
- Measurement equipment: CS2000 or similar equipments
- The point should be marked is, the background of Cross-talk Test Pattern-"gray " are defined as middle gray scale . For example, RGB 24bit "gray" defined as below:

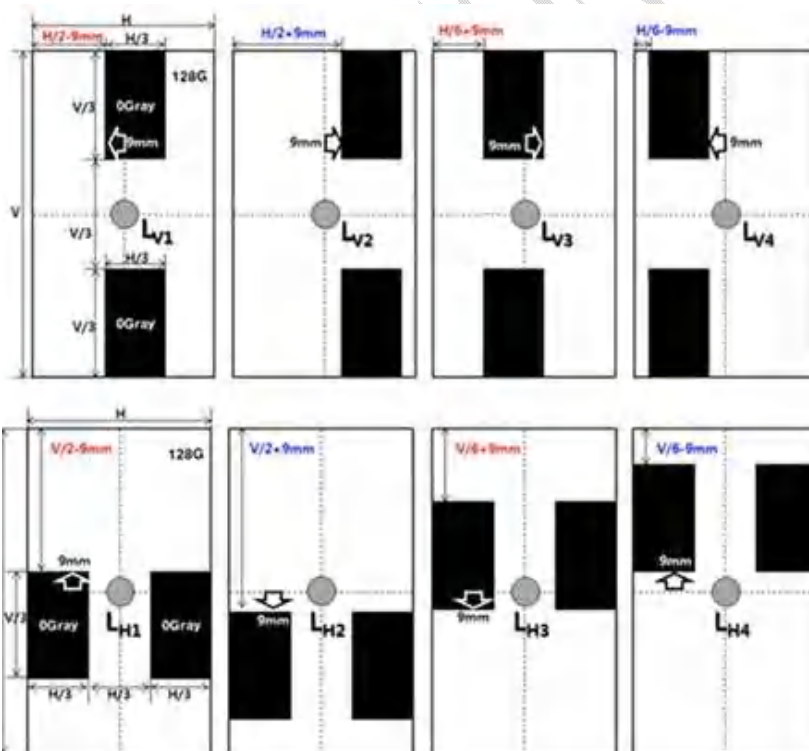
R2	R5	R8	R11	R14	R17	R20	R23	G2	G5	G8	G11	G14	G17	G20	G23	B2	B5	B8	B11	B14	B17	B20	B23
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

- Test pattern follow below picture, the background is middle gray and with two black rectangle parts, each one is 1/9 of the AA size.
- Calculate the crosstalk(V) and crosstalk(H) with the test formula below:

$$Crosstalk(V) = \max \left(\left| \frac{L_{V1} - L_{V2}}{L_{V2}} \right| \times 100, \left| \frac{L_{V3} - L_{V4}}{L_{V4}} \right| \times 100 \right)$$

$$Crosstalk(H) = \max \left(\left| \frac{L_{H1} - L_{H2}}{L_{H2}} \right| \times 100, \left| \frac{L_{H3} - L_{H4}}{L_{H4}} \right| \times 100 \right)$$

- Then use the max value between Crosstalk(V) and Crosstalk(H) as the final crosstalk.





8 Environmental / Reliability Test

No	Test Item	Condition	Remark
1	High Temperature Operation	Ts=+70℃, 120hrs	Note1
2	Low Temperature Operation	Ta=-30℃, 120hrs	
3	High Temperature Storage	Ta=+80℃, 120hrs	
4	Low Temperature Storage	Ta=-40℃, 120hrs	
5	High Temperature & High Humidity Storage	Ta=+60℃, 90% RH 120 hours	Note2
6	Thermal Shock (Non-operation)	-40℃ 30 min~+80℃ 30 min, Change time:3min, 30Cycles	Start with cold temperature, End with high temperature,
7	Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total)(Package condition)	
8	Package Drop Test	Height:80 cm,(When Package weight 10≤M<20 Kg) 1 corner, 3 edges, 6 surfaces	

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

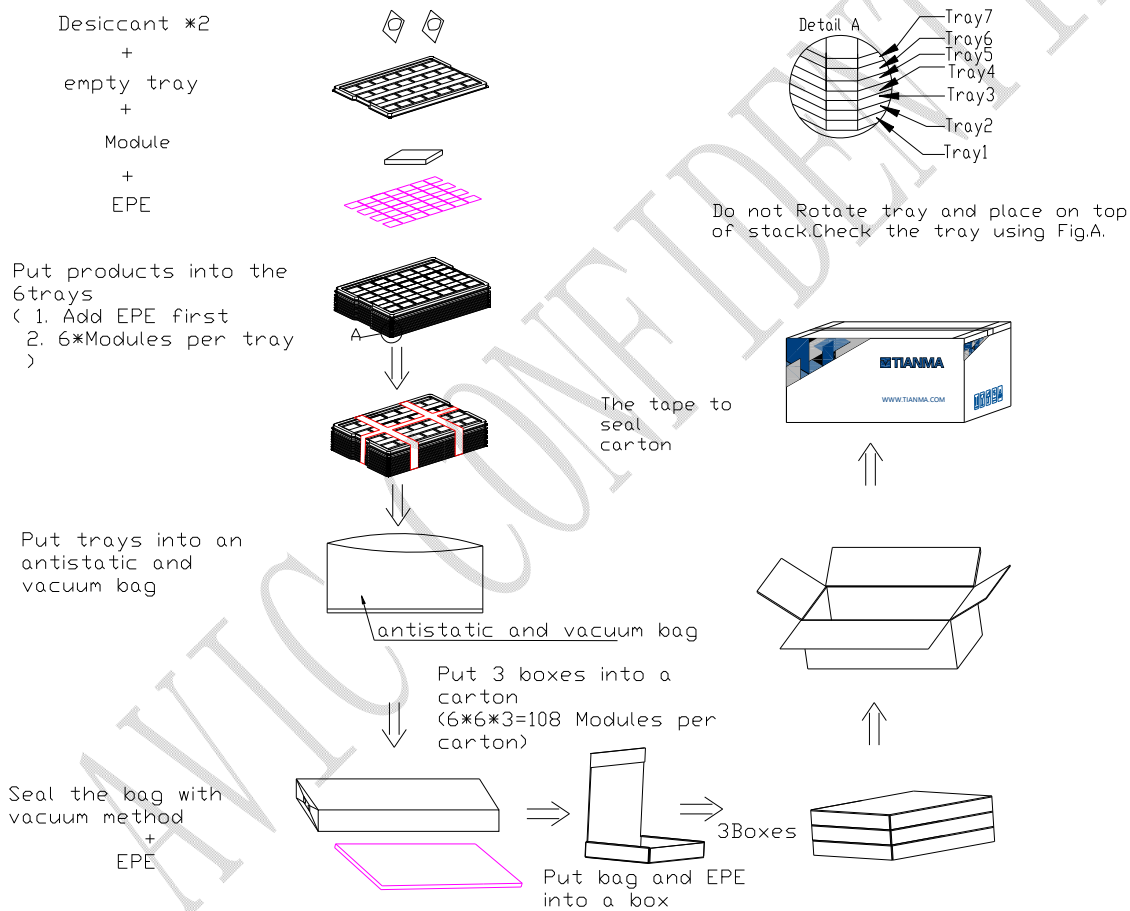


9 Packing Form

Packing Specifications

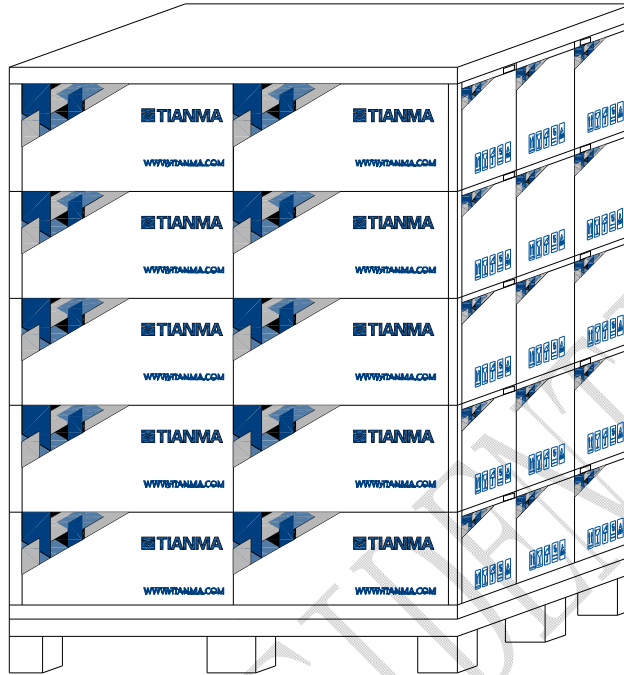
Item	Specification	Remark
Carton(Box) Packing	108pcs	
Carton(Box) Packing Size	544×365×250mm	
Carton(Box) Packing Weight	TBD	For Reference
Pallet Packing	3240 pcs	
Pallet Packing Size	1100x1100x130mm	
Pallet Packing Weight	TBD	For Reference

Packing Method



**Stack:**

纸箱堆叠数按 2*3/每层*共 5 层，栈板尺寸 1100mm*1100mm*130mm，如图所示：





10 Precautions For Use of OLED Modules

10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the Organic Light-Emitting Diode inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The polarizer covering the display surface of the OLED module is soft and easily scratched. Handle this polarizer carefully.

10.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

10.1.6 Do not attempt to disassemble the OLED Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the OLED Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.3 The OLED Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage precautions

10.2.1 When storing the OLED modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The OLED modules should be stored under the storage temperature range. If the OLED modules will be stored for a long time, the recommend condition is:

Temperature : 0°C ~ 40°C Relatively humidity: ≤80%

10.3 The OLED modules should be stored in the room without acid, alkali and harmful gas.

10.3.1 Transportation Precautions

10.3.2 The OLED modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.